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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31cjmn4d

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31C.

Table 1. MCIMX31C and MCIMX31LC Ordering Information[1]

Part Number	Silicon Revision	Operating Temperature Range (°C)	Package[2]
MCIMX31CVMN4C!	2.0	–40 to 85	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LCVMN4C!	2.0	–40 to 85	
MCIMX31CVMN4D!	2.0.1	–40 to 85	
MCIMX31LCVMN4D!	2.0.1	–40 to 85	
MCIMX31CJMN4C	2.0.1	–40 to 85	
MCIMX31LCJMN4D	2.0.1	–40 to 85	
MCIMX31CJMN4D	2.0.1	–40 to 85	

1 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

2 Case 1931 is RoHS compliant, lead-free, MSL = 3.

1.2.1 Feature Differences Between TO2.0 and TO 2.0.1

The following is a summary of the differences between silicon Revision 2.0 and Revision 2.0.1:

- Revision 2.0.1 - iROM updated to support boot from USB HS and SD/MMC.

- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with Hit-Under-Miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector Floating Point co-processor (VFP) for 3D graphics and other floating-point applications hardware acceleration
- ETM™ and JTAG-based debug support

2.1.1 Memory System

The ARM1136JF-S complex includes 16 KB Instruction and 16 KB Data L1 caches. It connects to the MCIMX31C L2 unified cache through 64-bit instruction (read-only), 64-bit data read/write (bi-directional), and 64-bit data write interfaces.

The embedded 16K SRAM can be used for audio streaming data to avoid external memory accesses for the low-power audio playback, for security, or for other applications. There is also a 32-KB ROM for bootstrap code and other frequently-used code and data.

A ROM patch module provides the ability to patch the internal ROM. It can also initiate an external boot by overriding the boot reset sequence by a jump to a configurable address.

Table 2 shows information about the MCIMX31C core in tabular form.

Table 2. MCIMX31C Core

Core Acronym	Core Name	Brief Description	Integrated Memory Includes
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ Platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 x 5 multi-layer AHB crossbar switch (MAX), and a Vector Floating Processor (VFP). The MCIMX31C provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16 Kbyte Instruction Cache • 16 Kbyte Data Cache • 128 Kbyte L2 Cache • 32 Kbyte ROM • 16 Kbyte RAM

The MCIMX31C I/O parameters appear in Table 13 for DDR (Double Data Rate). See Table 7, "Operating Ranges," on page 12 for temperature and supply voltage ranges.

NOTE

NVCC for Table 13 refers to NVCC2, NVCC21, and NVCC22.

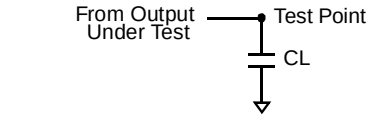
Table 13. DDR (Double Data Rate) I/O DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = –1 mA	NVCC –0.12	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.08	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current	I_{OH}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 –3.6 –7.2 –10.8 –14.4	—	—	mA
Low-level output current	I_{OL}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 3.6 7.2 10.8 14.4	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	NVCC	NVCC+0.3	V
Low-Level DC input voltage	V_{IL}	—	–0.3	0	0.3*NVCC	V
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

1 Use of DDR Drive can result in excessive overshoot and ringing.

4.3.2 AC Electrical Characteristics

Figure 4 depicts the load circuit for outputs. Figure 5 depicts the output transition time waveform. The range of operating conditions appears in Table 14 for slow general I/O, Table 15 for fast general I/O, and Table 16 for DDR I/O (unless otherwise noted).



CL includes package, probe and fixture capacitance

Figure 4. Load Circuit for Output

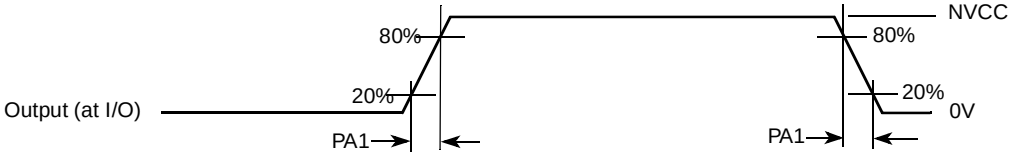


Figure 5. Output Transition Time Waveform

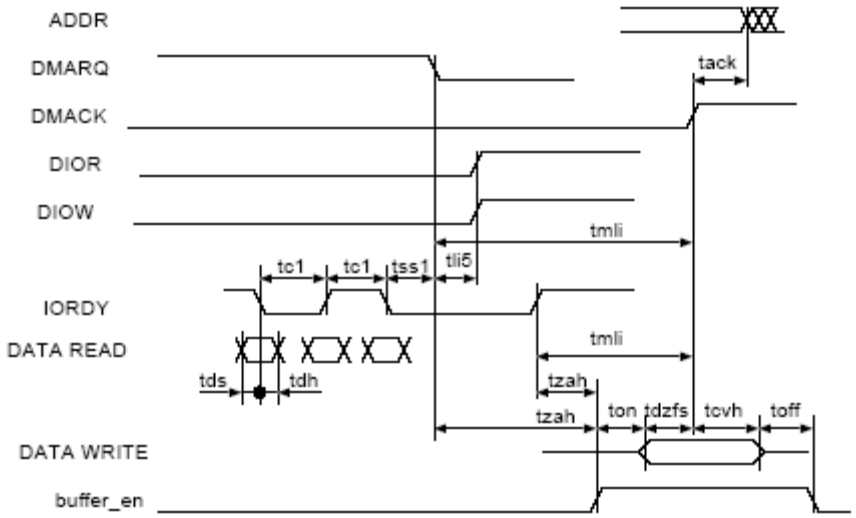


Figure 16. UDMA In Device Terminates Transfer Timing Diagram

Table 25. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 14, Figure 15, Figure 16	Description	Controlling Variable
tack	tack	tack (min) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env * T) – (tskew1 + tskew2) tenv (max) = (time_env * T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp * T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp * T) – (tco + tsu + 3T + 2 *tbuf + 2*tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) * T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) * T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs * T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff big enough to avoid bus contention

Table 28. DPLL Specifications (continued)

Parameter	Min	Typ	Max	Unit	Comments
Phase lock time	—	—	100	µs	In addition to the frequency
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ < 50 kHz
Maximum allowed PLL supply voltage ripple	—	—	20	mV	50 kHz < $F_{modulation}$ < 300 kHz
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ > 300 kHz
PLL output clock phase jitter	—	—	5.2	ns	Measured on CLKO pin
PLL output clock period jitter	—	—	420	ps	Measured on CLKO pin

1 The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

2 The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 22, Figure 23, Figure 24, and Figure 25 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 29 lists the timing parameters.

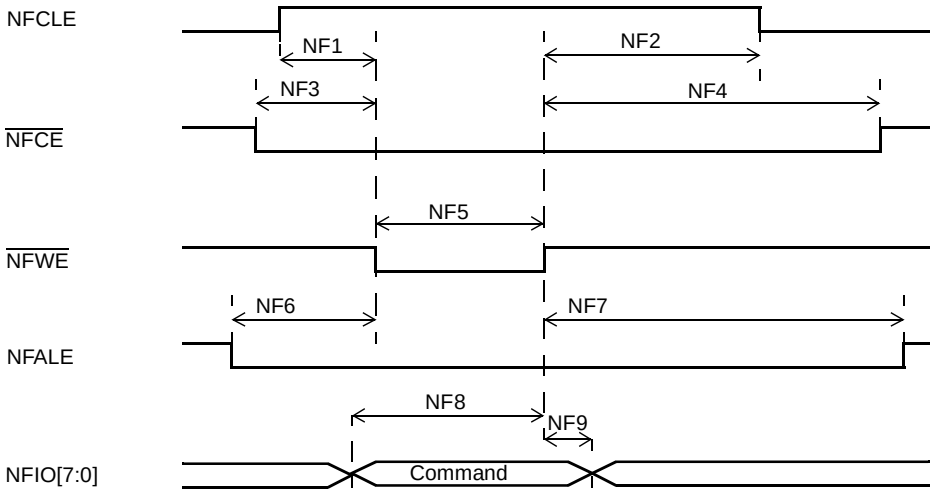


Figure 22. Command Latch Cycle Timing Diagram

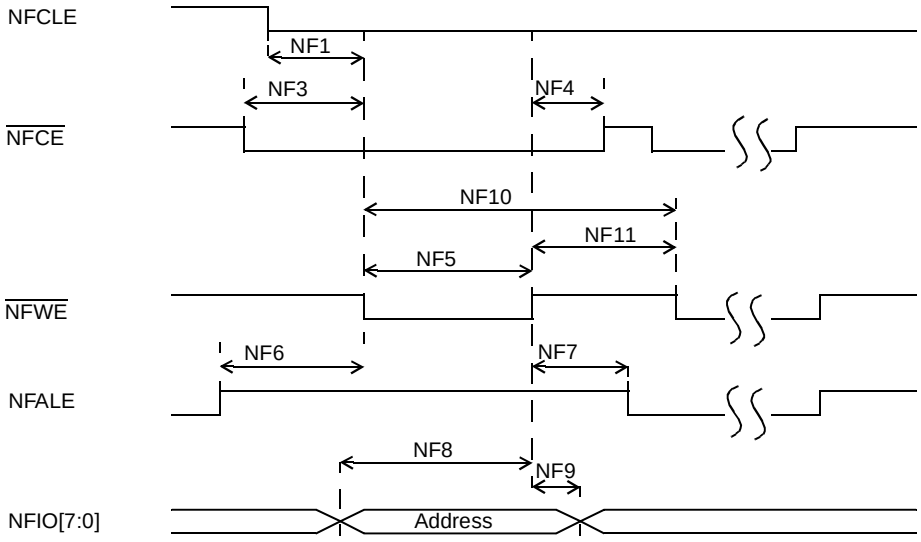


Figure 23. Address Latch Cycle Timing Diagram

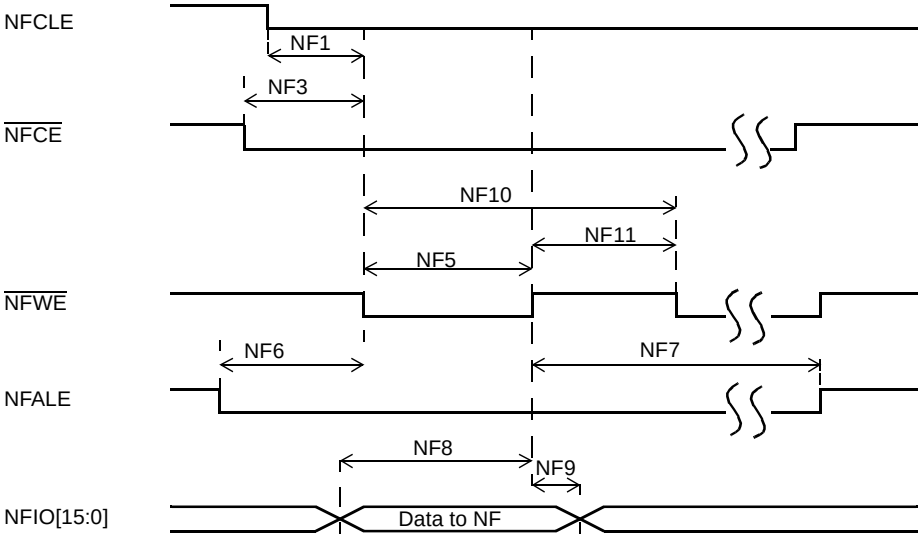


Figure 24. Write Data Latch Cycle Timing Diagram

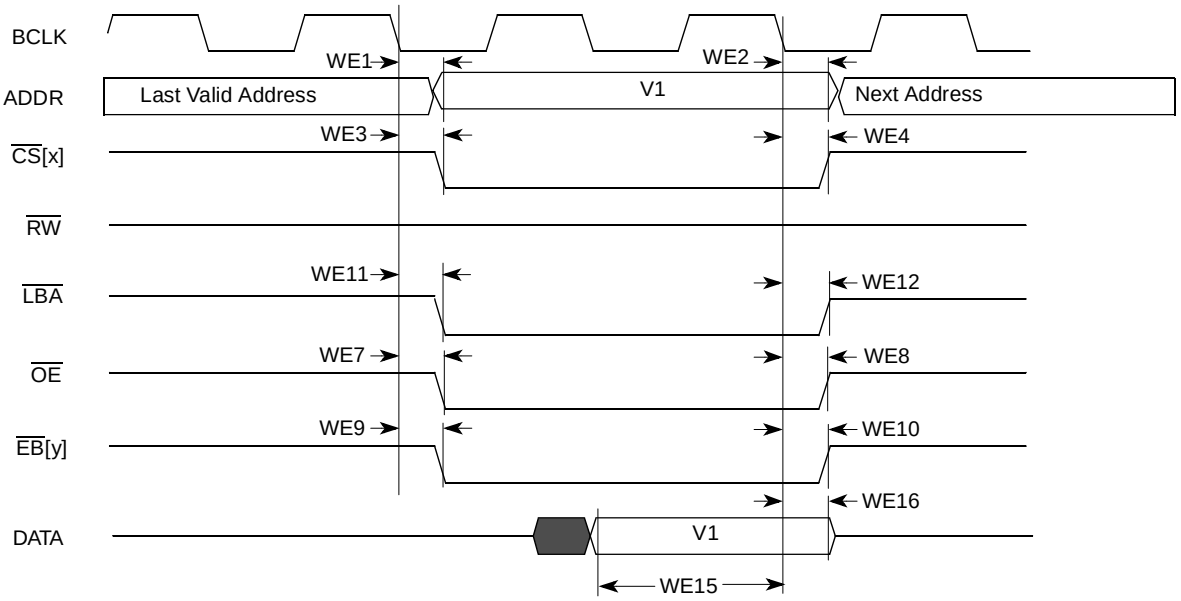


Figure 27. Asynchronous Memory Timing Diagram for Read Access—WSC=1

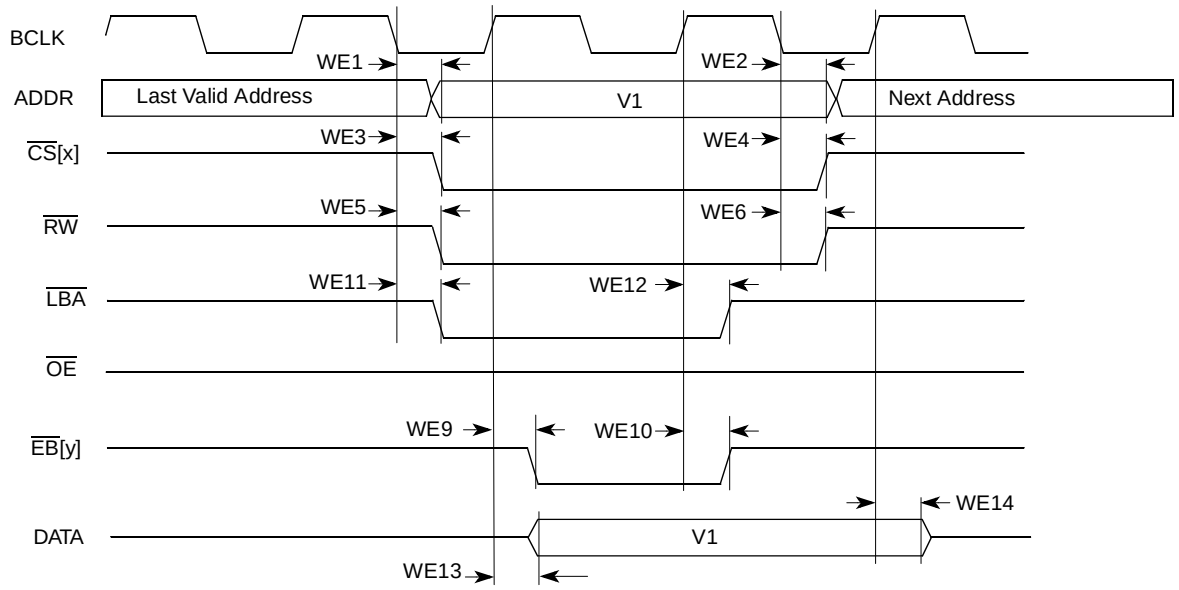


Figure 28. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

Table 31. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD9	Data out hold time[1]	tOH	1.8	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

1 Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 35 and Table 36.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 31 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

Table 33. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

1 SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 33 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

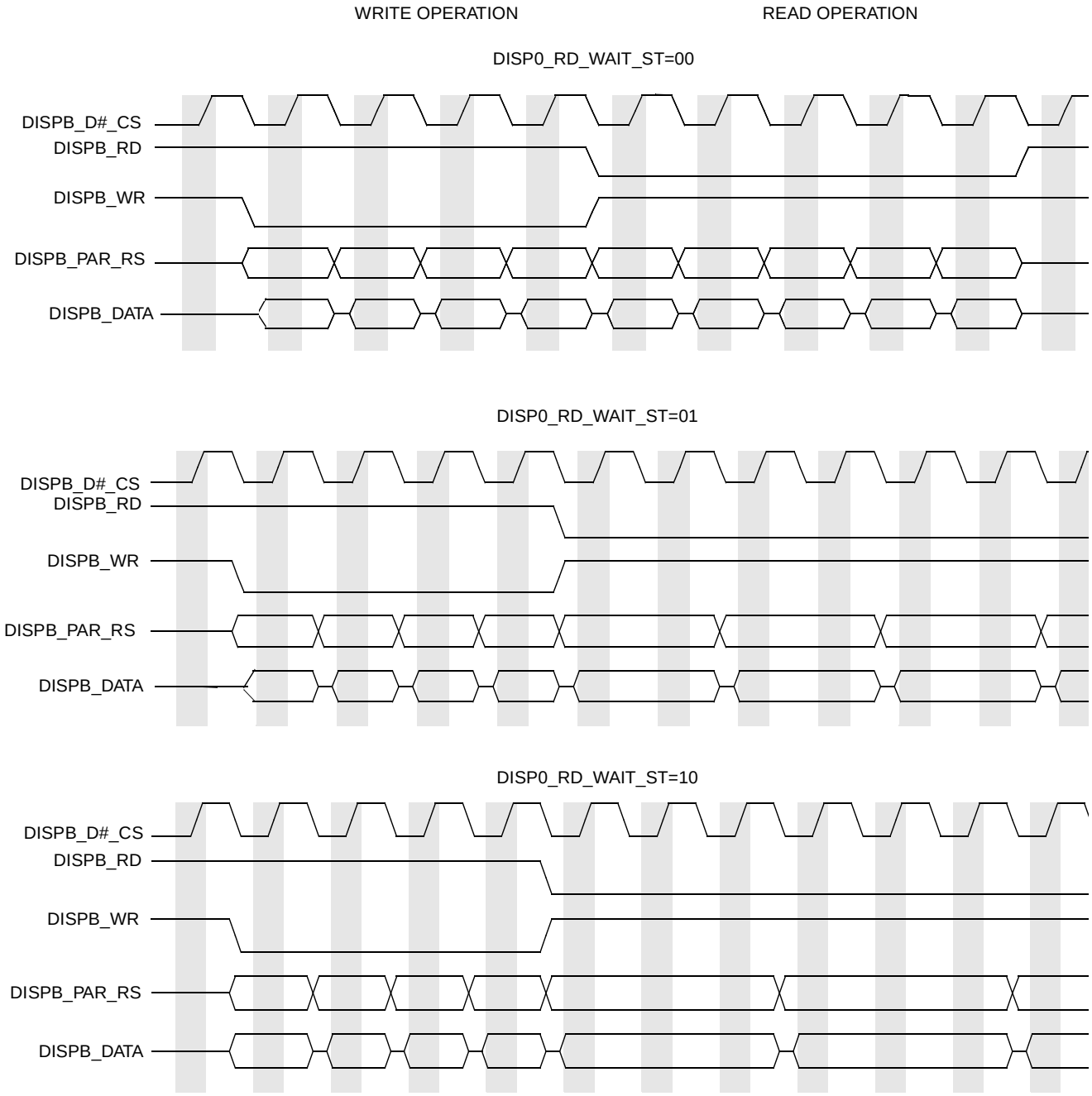


Figure 55. Parallel Interface Timing Diagram—Read Wait States

4.3.15.5.2 Parallel Interfaces, Electrical Characteristics

Figure 56, Figure 58, Figure 57, and Figure 59 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 47 lists the timing parameters at display access level. All timing images are based on active low control signals (signals polarity is controlled via the DI_DISP_SIG_POL Register).

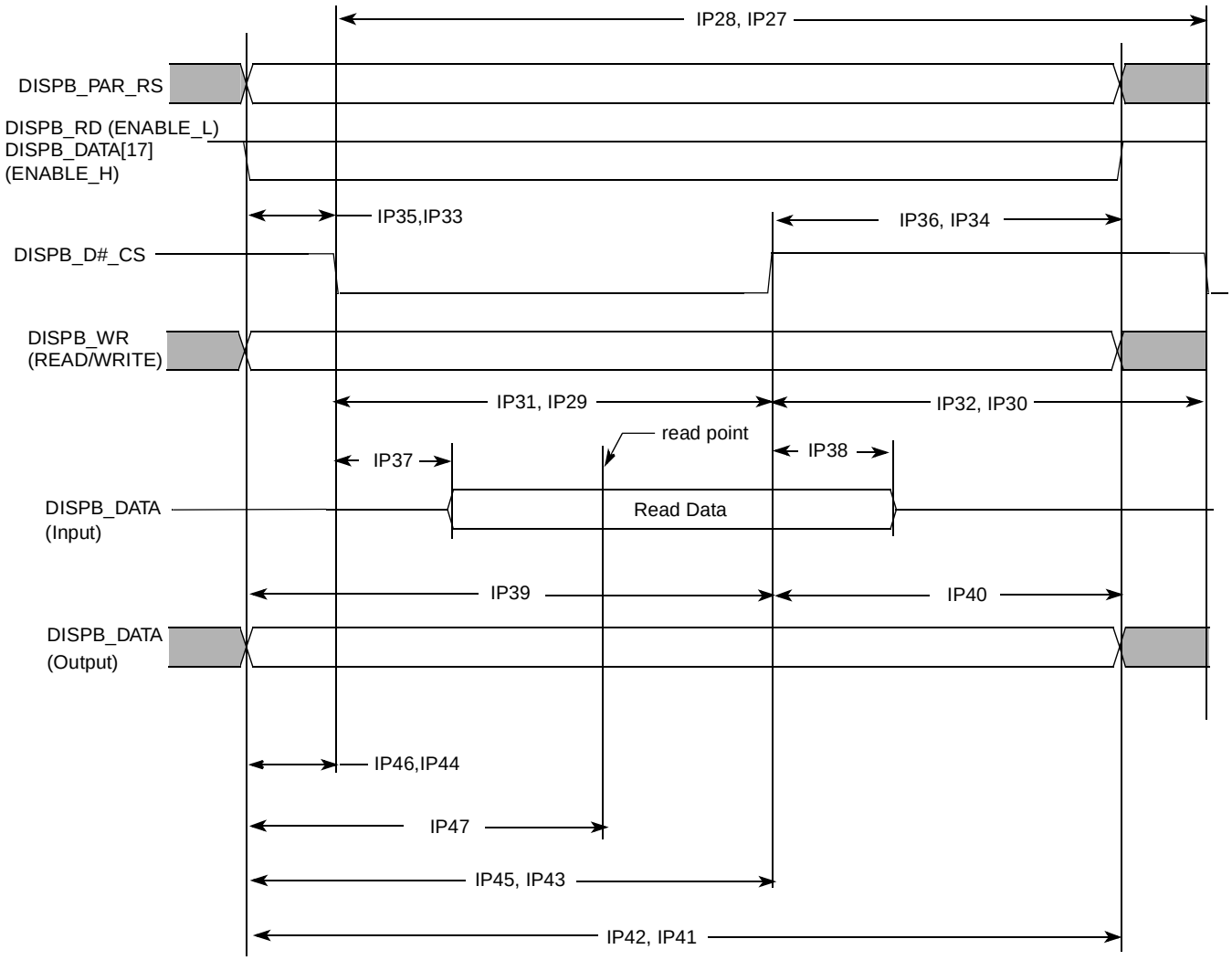


Figure 58. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

4.3.15.5.4 Serial Interfaces, Electrical Characteristics

Figure 64 depicts timing of the serial interface. Table 48 lists the timing parameters at display access level.

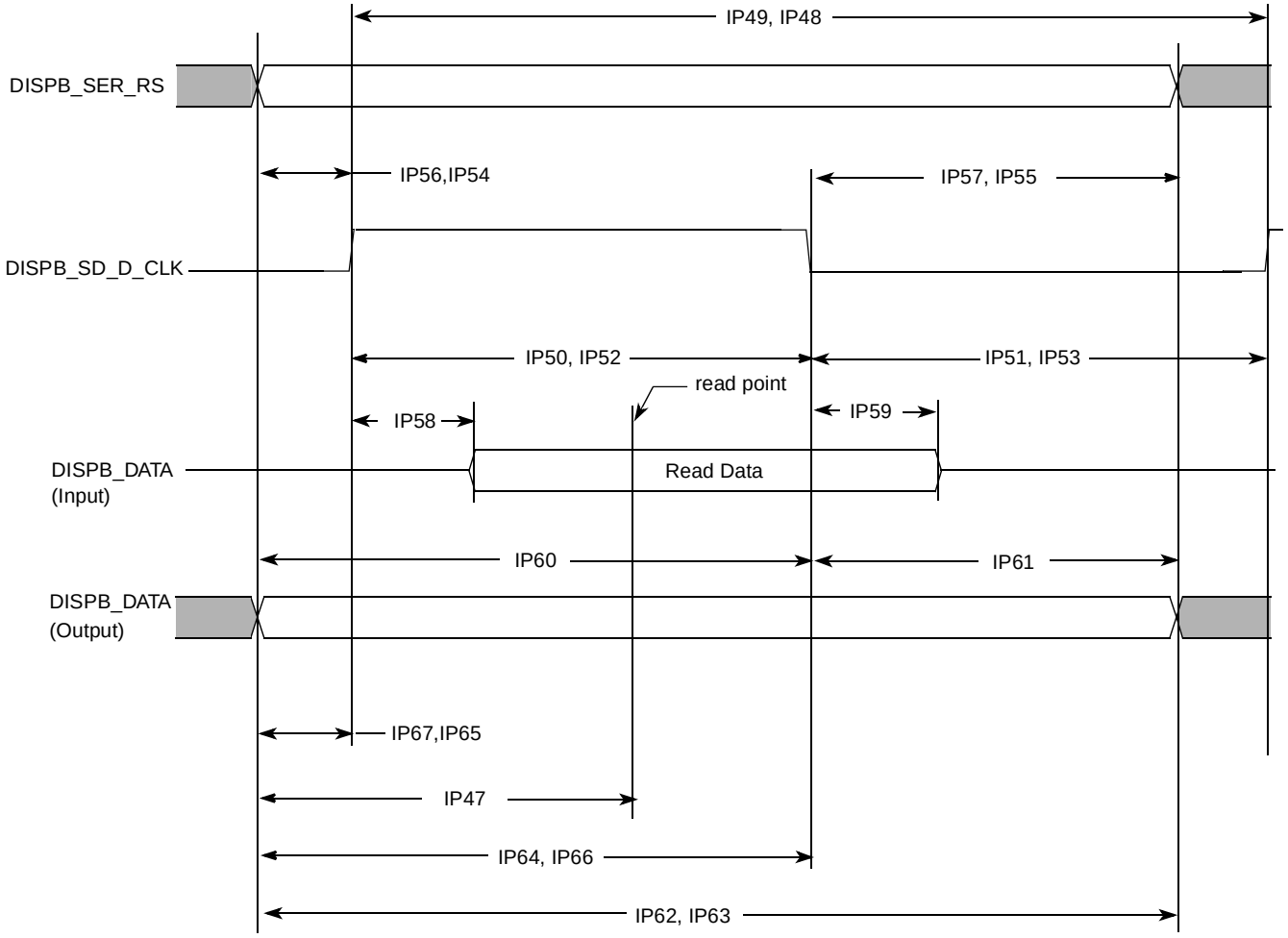


Figure 64. Asynchronous Serial Interface Timing Diagram

Table 48. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns

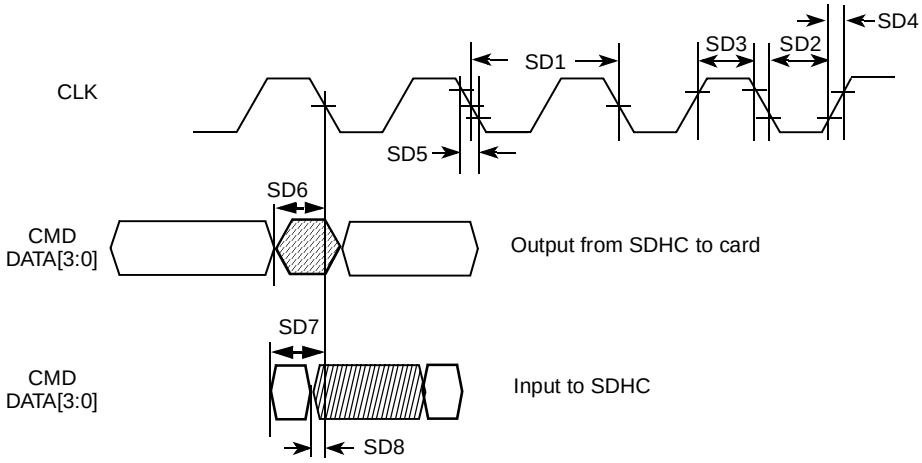


Figure 71. SDHC Timing Diagram

Table 53. SDHC Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	10	—	ns
SD3	Clock High Time	t_{WH}	10	—	ns
SD4	Clock Rise Time	t_{TLH}	—	10	ns
SD5	Clock Fall Time	t_{THL}	—	10	ns
SDHC output / Card inputs CMD, DAT (Reference to CLK)					
SD6	SDHC output delay	t_{ODL}	–6.5	3	ns
SDHC input / Card outputs CMD, DAT (Reference to CLK)					
SD7	SDHC input setup	t_{IS}	—	18.5	ns
SD8	SDHC input hold	t_{IH}	—	–11.5	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 V–3.3 V.
2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 MHz–25 MHz.
3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 MHz–20 MHz.
4 In card identification mode, card clock must be 100 kHz–400 kHz, voltage ranges from 2.7 V–3.3 V.

4.3.20 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (for 2 separate ports of 6 pins each. Mostly one port with 5 pins is used).

4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 75 and Table 55 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

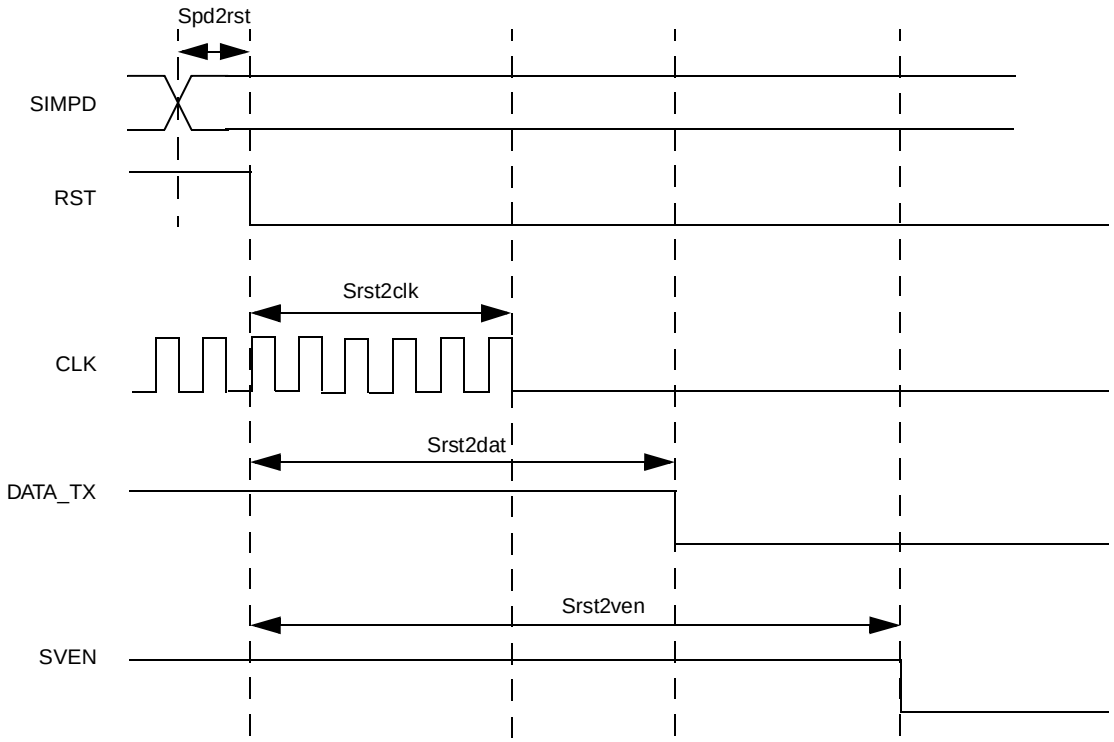


Figure 75. SmartCard Interface Power Down AC Timing

Table 55. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9*1/FCKIL	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8*1/FCKIL	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7*1/FCKIL	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9*1/FCKIL	25	ns

Table 56. SJC Timing Parameters (continued)

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 On cases where SDMA TAP is put in the chain, the max TCK frequency is limited by max ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

2 V_{M} - mid point voltage

4.3.22 SSI Electrical Specifications

This section describes the electrical information of SSI. Note the following pertaining to timing information:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing will be same as that of Tx Data (for example, during AC97 mode of operation).

4.3.22.1 SSI Transmitter Timing with Internal Clock

Figure 80 depicts the SSI transmitter timing with internal clock, and Table 57 lists the timing parameters.

Table 58. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

Table 59. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

4.3.22.4 SSI Receiver Timing with External Clock

Figure 83 depicts the SSI receiver timing with external clock, and Table 60 lists the timing parameters.

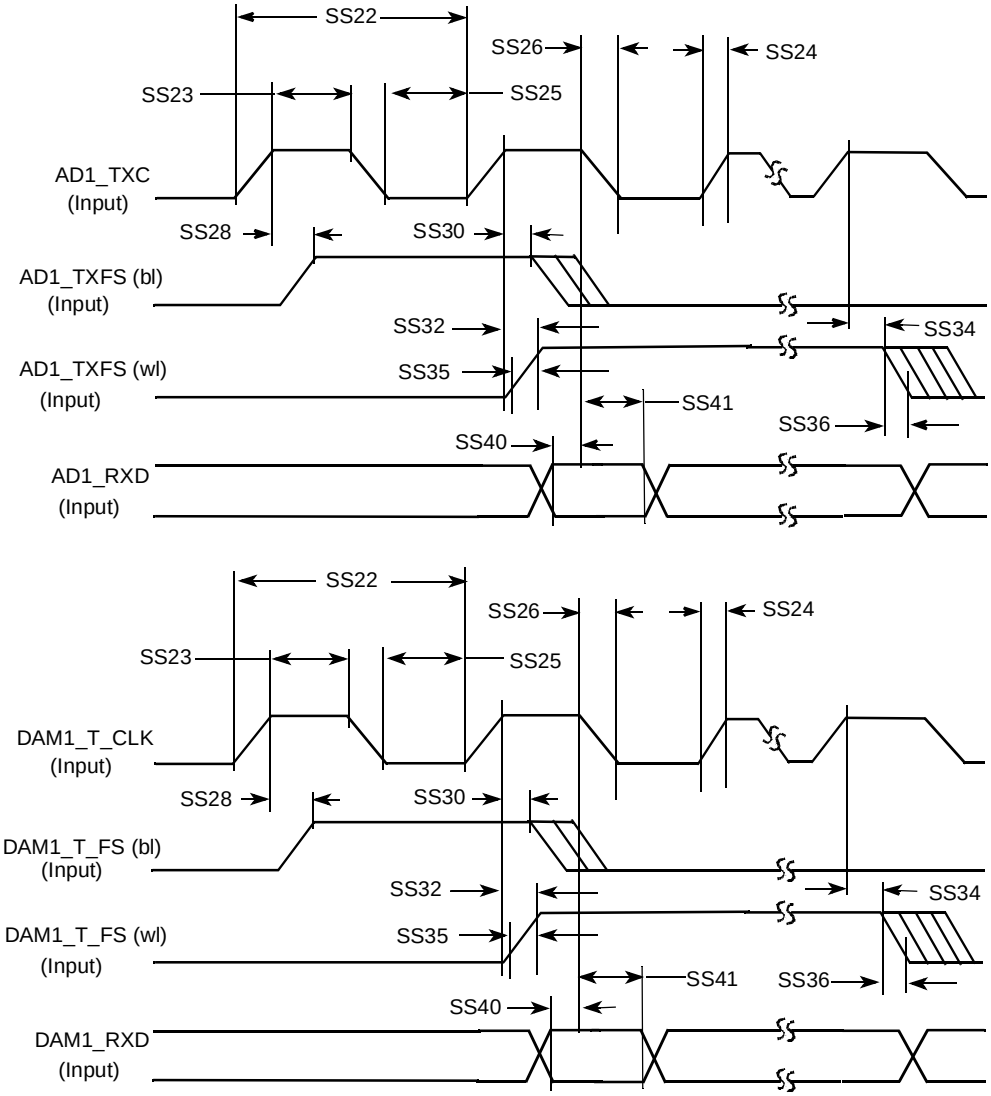


Figure 83. SSI Receiver with External Clock Timing Diagram

Table 60. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns

5 Package Information and Pinout

This section includes the contact assignment information and mechanical package drawing for the MCIMX31C.

5.1.2 MAPBGA Signal Assignment–19 × 19 mm 0.8 mm

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	GND	CSPI2_SS1	USBOTG_DATA6	USBOTG_DATA2	USBOTG_DIR	USB_PWR	CTS1	DTR_DTE1	DSR_DTE1	RXD2	KEY_ROW0	KEY_ROW3	KEY_COL0	KEY_COL5	KEY_COL7	TDI	SRX0	COMPARE	GND	GND	GND	A
B	GND	GND	STXD4	CSPI2_MISO	CSPI2_SCLK	USBOTG_DATA5	USBOTG_NXT	USB_OC	RTS1	DSR_DCE1	RI_DTE1	RTS2	KEY_ROW1	KEY_ROW6	KEY_COL1	KEY_COL6	TDO	SIMPD0	SCLK0	GPIO1_2	WATCHDOG_RST	GND	GND	B
C	GND	GND	SRXD4	SRXD5	CSPI2_SS0	USBOTG_DATA7	USBOTG_DATA1	USB_BYP	RXD1	DCD_DCE1	DTR_DCE2	CTS2	KEY_ROW2	KEY_ROW7	KEY_COL3	TMS	SJC_MOD	SRST0	GPIO1_0	CLKO	BOOT_MODE1	GND	GND	C
D	STXD5	CSPI3_MISO	SFS4	SCK5	CSPI2_MOSI	CSPI2_SPI_RDY	USBOTG_DATA4	USBOTG_CLK	TXD1	RI_DCE1	DCD_DTE1	CE_CONTROL	KEY_ROW5	KEY_COL2	RTCK	$\overline{DE}$	SVEN0	CAPTURE	GPIO1_5	BOOT_MODE2	GPIO1_4	GND	GND	D
E	ATA_CS0	ATA_DMACK	ATA_DIOR	CSPI3_MOSI																BOOT_MODE4	CKIL	DVFS0	DVFS1	E
F	PC_RST	PWMO	$\overline{ATA\_RESET}$	CSPI3_SPI_RDY		BATT_LINE	CSPI2_SS2	USBOTG_DATA3	USBOTG_STP	DTR_DCE1	TXD2	KEY_ROW4	KEY_COL4	TCK	TRSTB	STX0	BOOT_MODE0	BOOT_MODE3		POWER_FAIL	$\overline{POR}$	$\overline{RESET\_IN}$	CKIH	F
G	PC_VS2	PC_BVD1	$\overline{PC\_RW}$	ATA_CS1		SCK4	SFS5	USBOTG_DATA0	NVCC5	NVCC5	NVCC6	NVCC6	NVCC6	NVCC9	NVCC1	NVCC1	GPIO1_1	GPIO1_6		GPIO1_3	VPG0	VPG1	GPIO3_0	G
H	$\overline{PC\_CD2}$	PC_READY	PC_VS1	PC_BVD2		ATA_DIOW	CSPI3_SCLK	NVCC5	NVCC5	NVCC8	NVCC8	NVCC6	QVCC	NVCC4	NVCC7	NVCC1	CLKSS	VSTBY		CSI_MCLK	CSI_VSYNC	CSI_HSYNC	CSI_PIXCLK	H
J	SD1_DATA1	SD1_DATA2	$\overline{PC\_CD1}$	$\overline{PC\_WAIT}$		PC_POE	IOIS16	QVCC1	QVCC1	QVCC1	NVCC8	GND	GND	QVCC	NVCC4	NVCC7	NVCC1	I2C_CLK		CSI_D4	CSI_D5	CSI_D7	CSI_D8	J
K	USBH2_DATA1	SD1_CLK	SD1_CMD	SD1_DATA0		PC_PWRON	NVCC3	NVCC3	QVCC1	GND	GND	GND	GND	GND	NVCC4	NVCC7	GPIO3_1	I2C_DAT		CSI_D9	CSI_D10	CSI_D11	CSI_D12	K
L	USBH2_CLK	USBH2_DIR	USBH2_STP	USBH2_NXT		SD1_DATA3	NVCC3	NVCC3	QVCC4	GND	GND	GND	GND	GND	QVCC	NVCC7	CSI_D6	CSI_D14		CSI_D13	CSI_D15	VSYNC0	HSYNC	L
M	CSPI1_SPI_RDY	CSPI1_SS0	CSPI1_SS2	CSPI1_SCLK		USBH2_DATA0	QVCC4	QVCC4	GND	GND	GND	GND	GND	GND	QVCC	NVCC7	DRDY0	SD_D_IO		SD_D_I	SD_D_CLK	LCS0	FPSHIFT	M
N	CSPI1_MOSI	CSPI1_MISO	SRXD3	STXD3		CSPI1_SS1	NC[1]	QVCC4	QVCC	GND	GND	GND	GND	GND	QVCC	NVCC2	D3_SPL	READ		VSYNC3	CONTRAST	WRITE	LCS1	N
P	SCK3	SFS3	STXD6	SFS6		$\overline{NFWP}$	NC[1]	NVCC10	QVCC	GND	GND	GND	GND	GND	QVCC	NVCC2	UGND	UVCC		D3_CLS	D3_REV	PAR_RS	SER_RS	P
R	SRXD6	SCK6	NFRB	$\overline{NFCE}$		D13	NVCC10	NVCC10	NVCC10	QVCC	QVCC	GND	QVCC	QVCC	NVCC2	NVCC2	LD8	LD11		LD3	LD2	LD1	LD0	R
T	NFCLE	NFALE	$\overline{NFWE}$	$\overline{NFRE}$		D8	D4	IOQVDD	NVCC10	NVCC22	NVCC21	NVCC21	NVCC21	NVCC2	FUSE_VDD	FVCC	M_REQUEST	OE		LD7	LD6	LD5	LD4	T
U	D15	D14	D12	D11		D0	NVCC22	NVCC22	NVCC22	NVCC22	NVCC21	SVCC	SGND	MGND	MVCC	FGND	CS0	M_GRANT		LD12	NC	LD10	LD9	U
V	D10	D9	D6	D3		NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	A22	A20	A18	A16	A10	SDCKE1	LBA	RW		LD16	LD15	LD14	LD13	V
W	D7	D5	D2	D1																BCLK	EB1	EB0	LD17	W
Y	GND	MA10	A13	A8	A4	A0	SDBA1	A25	A24	A23	A21	A19	A17	A15	A14	DQM1	SDCKE0	CS2	CS3	CS4	ECB	CS1	GND	Y
AA	GND	GND	A12	A7	A3	SDBA0	SD30	SD28	SD24	SD20	SD17	SD15	SD12	SD9	SD6	SD4	SD1	DQM2	RAS	CAS	CS5	GND	GND	AA
AB	GND	GND	A11	A6	A2	SDQS3	SD29	SD26	SDQS2	SD21	SD18	SDQS1	SD13	SD10	SD7	SDQS0	SD2	DQM3	DQM0	SDWE	GND	GND	GND	AB
AC	GND	GND	A9	A5	A1	SD31	SD27	SD25	SD23	SD22	SD19	SD16	SD14	SD11	SD8	SD5	SD3	SD0	$\overline{SDCLK}$	SDCLK	GND	GND	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

1 These contacts are not used and must be floated by the user.

Figure 86. Ball Map—0.8 mm Pitch