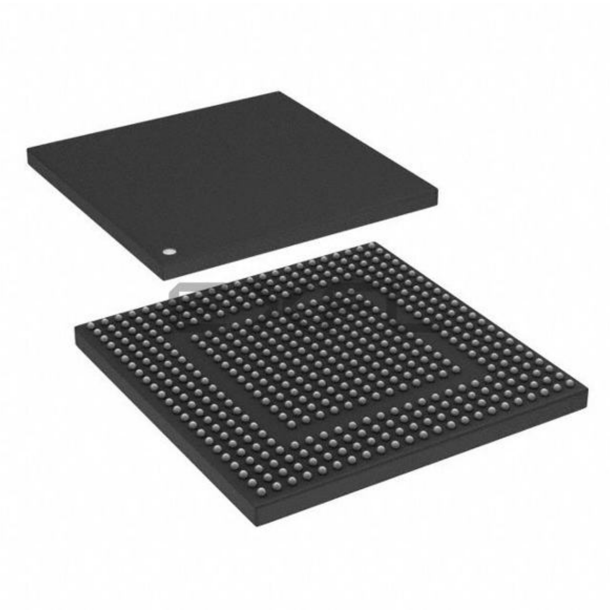

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31cjmn4dr2

The MCIMX31C I/O parameters appear in Table 13 for DDR (Double Data Rate). See Table 7, "Operating Ranges," on page 12 for temperature and supply voltage ranges.

NOTE

NVCC for Table 13 refers to NVCC2, NVCC21, and NVCC22.

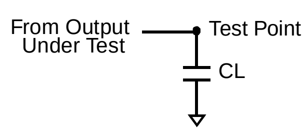
Table 13. DDR (Double Data Rate) I/O DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = –1 mA	NVCC –0.12	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.08	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current	I_{OH}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 –3.6 –7.2 –10.8 –14.4	—	—	mA
Low-level output current	I_{OL}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 3.6 7.2 10.8 14.4	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	NVCC	NVCC+0.3	V
Low-Level DC input voltage	V_{IL}	—	–0.3	0	0.3*NVCC	V
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

[1] Use of DDR Drive can result in excessive overshoot and ringing.

4.3.2 AC Electrical Characteristics

Figure 4 depicts the load circuit for outputs. Figure 5 depicts the output transition time waveform. The range of operating conditions appears in Table 14 for slow general I/O, Table 15 for fast general I/O, and Table 16 for DDR I/O (unless otherwise noted).



CL includes package, probe and fixture capacitance

Figure 4. Load Circuit for Output

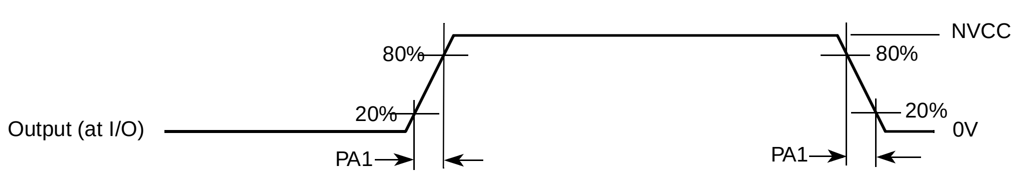


Figure 5. Output Transition Time Waveform

Table 17. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1]– 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

[1] VDD is the supply voltage of CAMP. See reference manual.
[2] This value of the sinusoidal input will be measured through characterization.

4.3.4 1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 18 lists the RPP timing parameters.

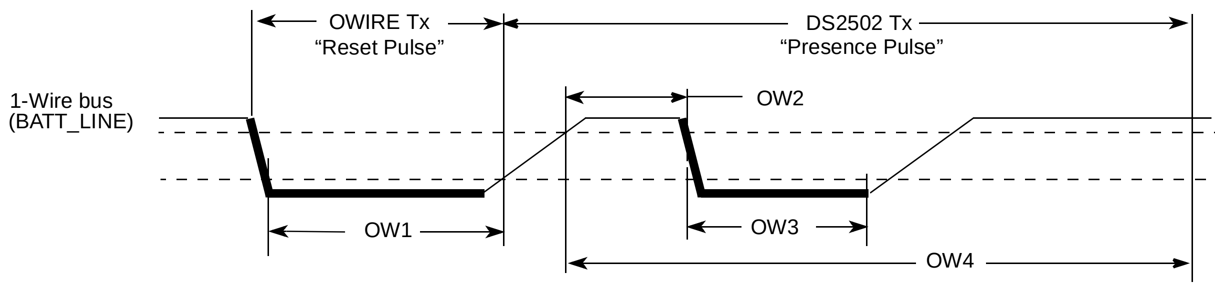


Figure 6. Reset and Presence Pulses (RPP) Timing Diagram

Table 18. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 7 depicts Write 0 Sequence timing, and Table 19 lists the timing parameters.

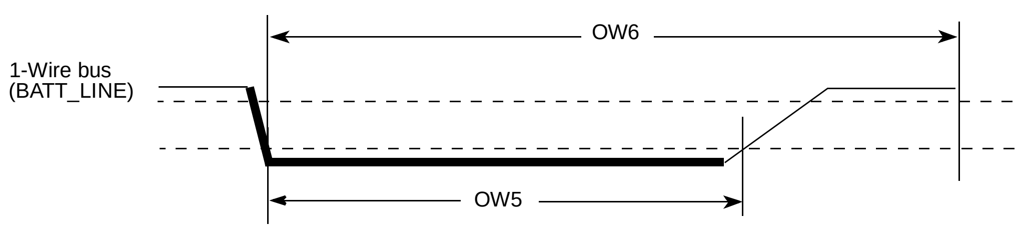


Figure 7. Write 0 Sequence Timing Diagram

Table 21. ATA Timing Parameters (continued)

Name	Description	Value/ Contributing Factor[1]
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	cable

[1] Values provided where applicable.

4.3.5.2 PIO Mode Timing

Figure 10 shows timing for PIO read, and Table 22 lists the timing parameters for PIO read.

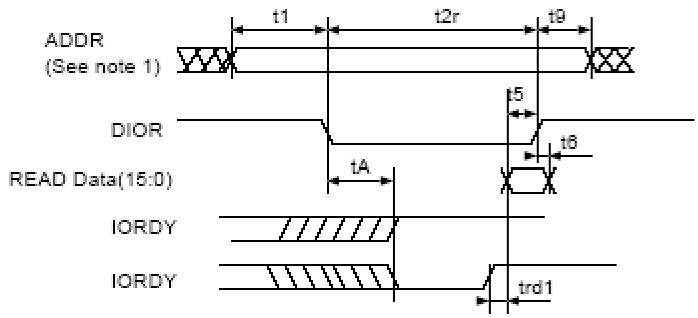


Figure 10. PIO Read Timing Diagram

Table 22. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 10	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 11 shows timing for PIO write, and Table 23 lists the timing parameters for PIO write.

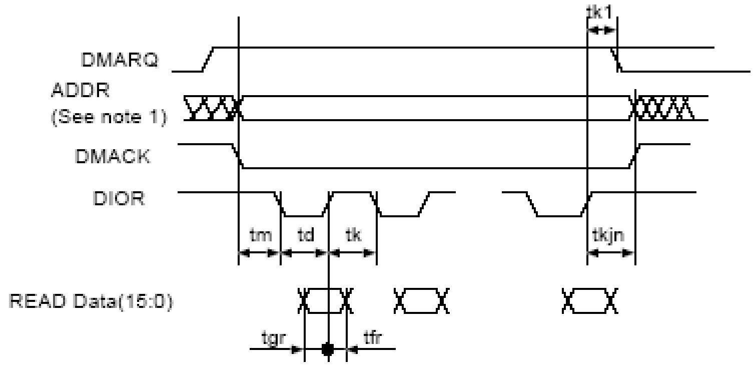


Figure 12. MDMA Read Timing Diagram

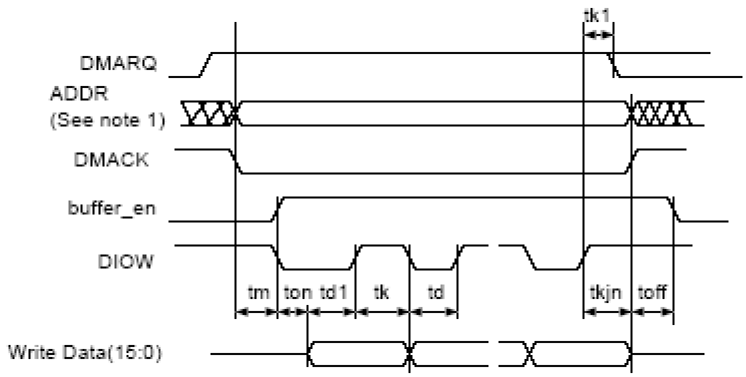


Figure 13. MDMA Write Timing Diagram

Table 24. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 12, Figure 13	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

Table 27. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	30	—	ns
CS3	SCLK Rise or Fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	SSx pulse width	t_{CSLH}	25	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	25	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	25	—	ns
CS7	Data Out Setup Time	t_{Smosi}	5	—	ns
CS8	Data Out Hold Time	t_{Hmosi}	5	—	ns
CS9	Data In Setup Time	t_{Smiso}	6	—	ns
CS10	Data In Hold Time	t_{Hmiso}	5	—	ns
CS11	$\overline{\text{SPI\_RDY}}$ Setup Time[1]	t_{SRDY}	—	—	ns

[1] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31C (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

4.3.8.1 Electrical Specifications

Table 28 lists the DPLL specification.

Table 28. DPLL Specifications

Parameter	Min	Typ	Max	Unit	Comments
CKIH frequency	15	26[1]	75[2]	MHz	—
CKIL frequency (Frequency Pre-multiplier (FPM) enable mode)	—	32; 32.768, 38.4	—	kHz	FPM lock time ≈ 480 µs.
Predivision factor (PD bits)	1	—	16	—	—
PLL reference frequency range after Predivider	15	—	35	MHz	15 ≤ CKIH frequency/PD ≤ 35 MHz 15 ≤ FPM output/PD ≤ 35 MHz
PLL output frequency range: MPLL and SPLL UPLL	 52 190	—	 400 240	MHz	—
Maximum allowed reference clock phase noise.	—	—	± 100	ps	—
Frequency lock time (FOL mode or non-integer MF)	—	—	398	—	Cycles of divided reference clock.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

NOTE

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 26 depicts the timing of the WEIM module, and Table 30 lists the timing parameters.

Table 30. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{\text{OE}}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{\text{EB}}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{\text{EB}}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{\text{LBA}}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{\text{LBA}}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{\text{ECB}}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{\text{ECB}}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{\text{DTACK}}$ setup time[1]	0	—	ns
WE20	$\overline{\text{DTACK}}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing
2 BCLK parameters are being measured from the 50% VDD.
3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 27, Figure 28, Figure 29, Figure 30, Figure 31, and Figure 32 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 30 for specific control parameter settings.

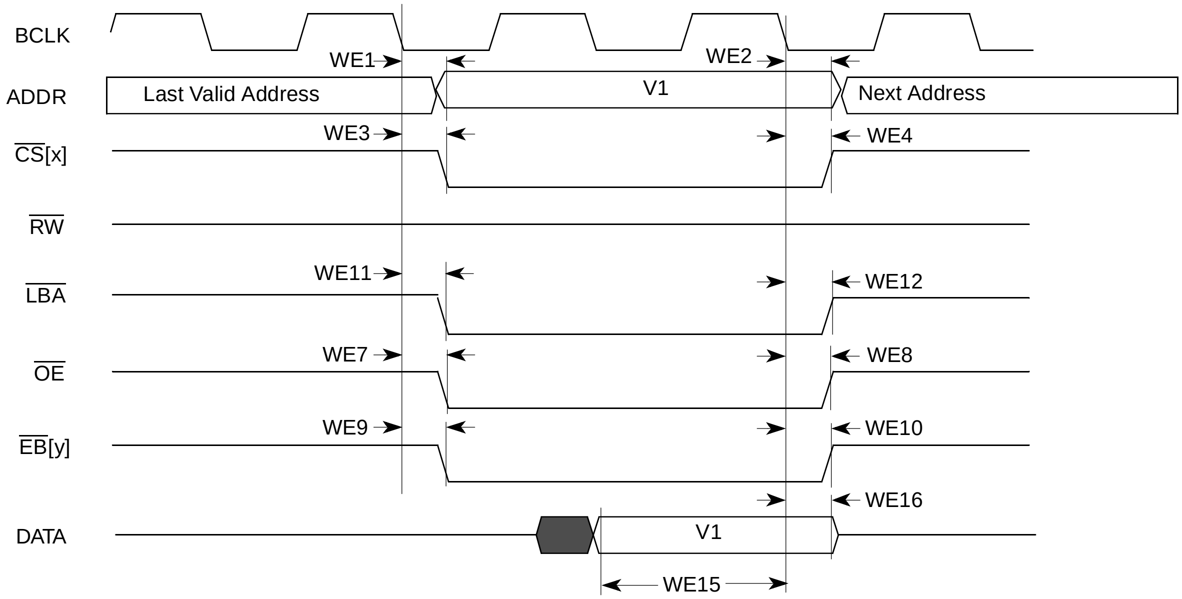


Figure 27. Asynchronous Memory Timing Diagram for Read Access—WSC=1

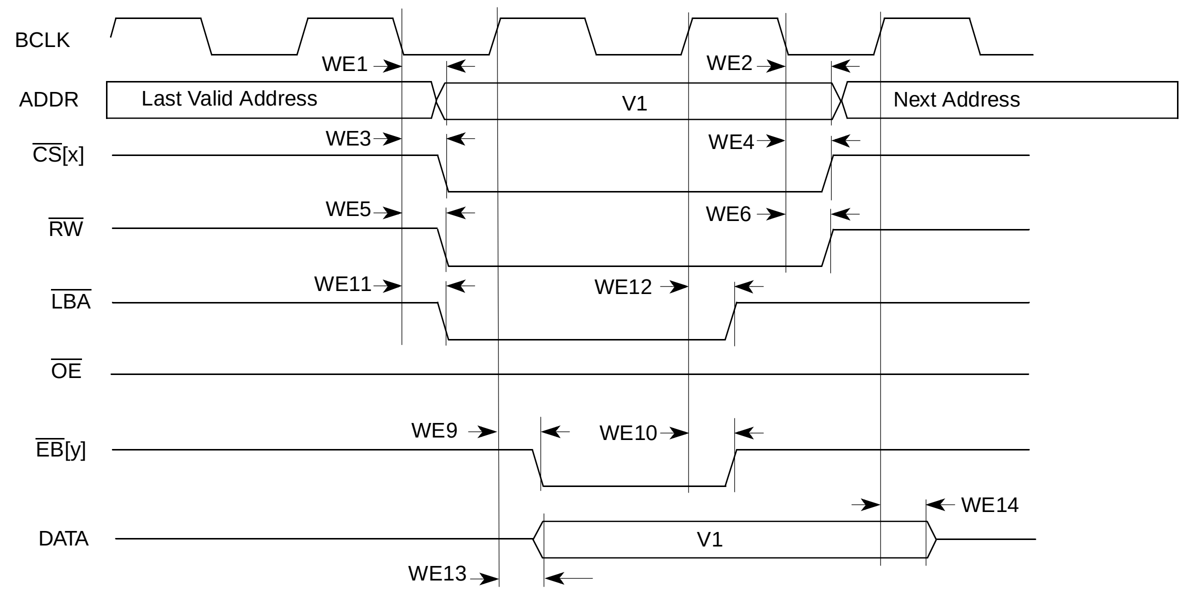


Figure 28. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

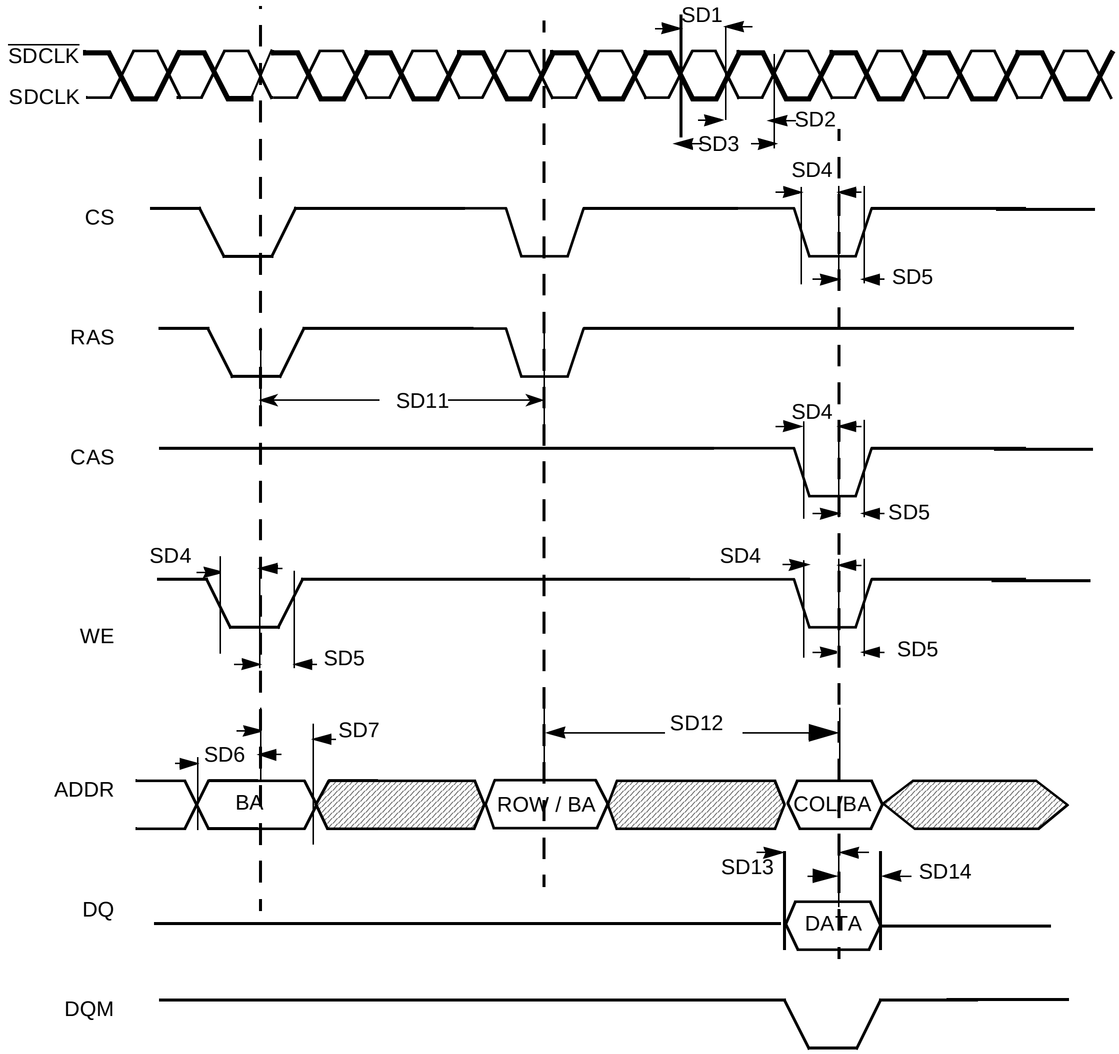


Figure 34. SDR SDRAM Write Cycle Timing Diagram

Table 32. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD11	Precharge cycle period[1]	tRP	1	4	clock
SD12	Active to read/write command delay[1]	tRCD	1	8	clock

4.3.13 I²C Electrical Specifications

This section describes the electrical information of the I²C Module.

4.3.13.1 I²C Module Timing

Figure 41 depicts the timing of I²C module. Table 40 lists the I²C module timing parameters where the I/O supply is 2.7 V. 1

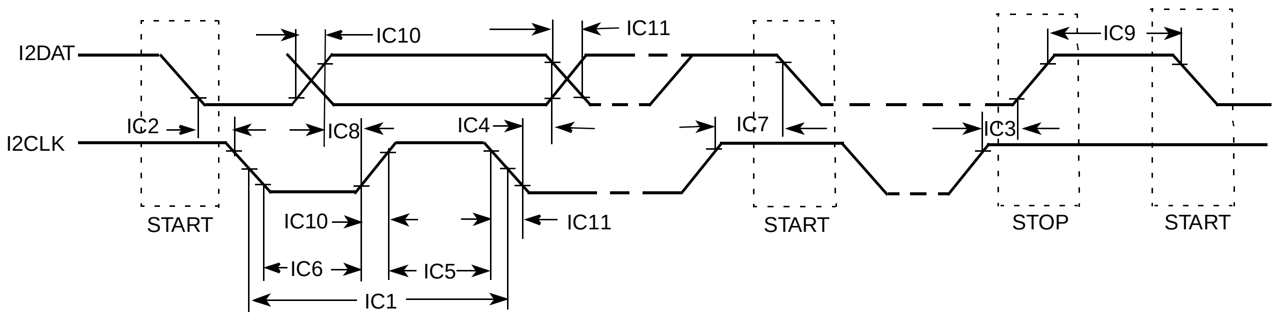


Figure 41. I²C Bus Timing Diagram

Table 40. I²C Module Timing Parameters—I²C Pin I/O Supply=2.7 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

[1] A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

[3] A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

[4] C_b = total capacitance of one bus line in pF.

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 41 lists the known supported camera sensors at the time of publication.

Table 41. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI–SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

4.3.14.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 42.

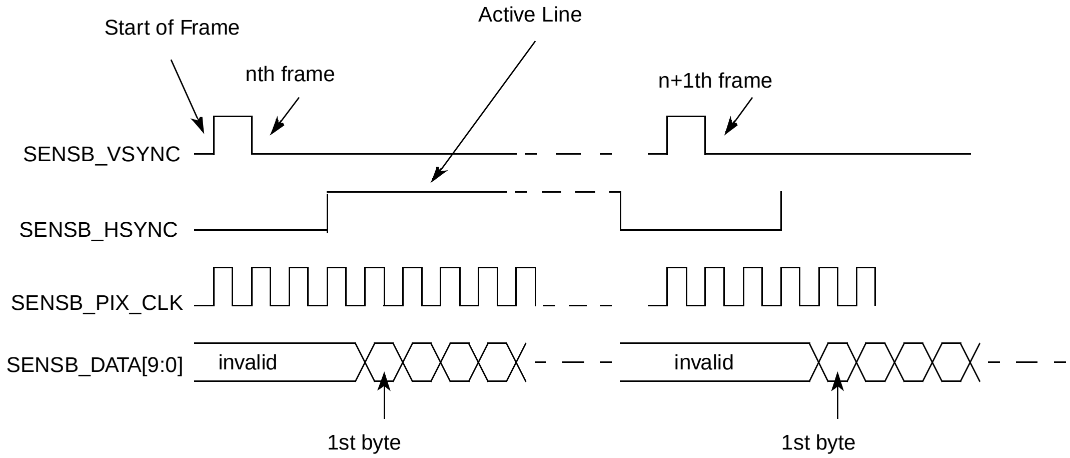


Figure 42. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.3.14.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.3.14.2.2, "Gated Clock Mode," on page 52), except for the SENSB_HSYNC signal, which is not used. See Figure 43. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

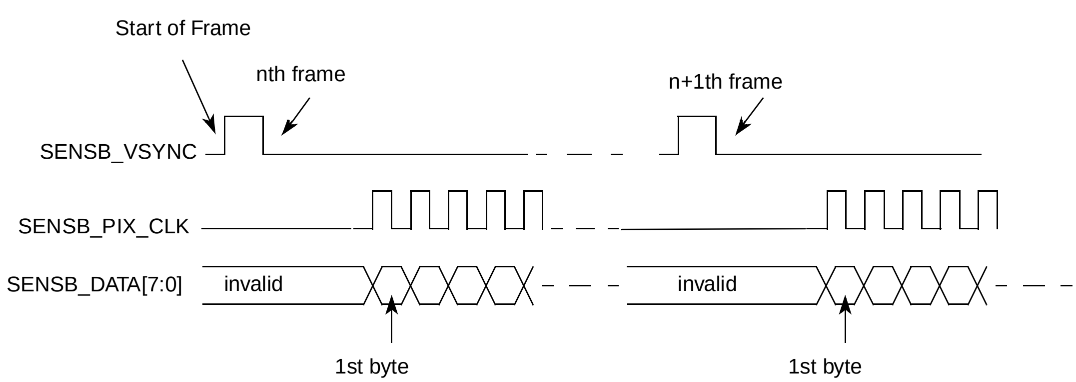


Figure 43. Non-Gated Clock Mode Timing Diagram

- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

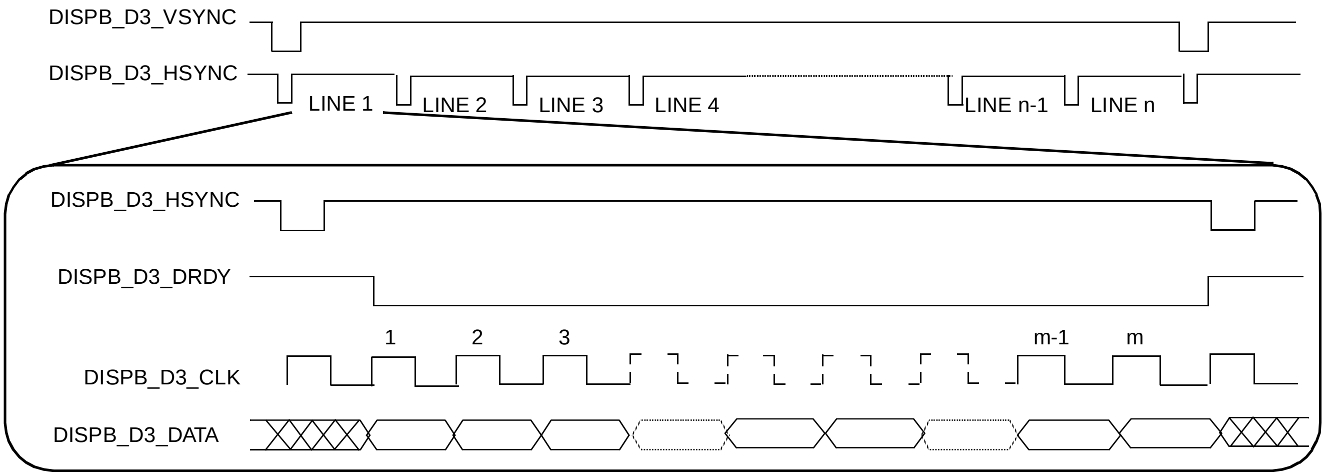


Figure 45. Interface Timing Diagram for TFT (Active Matrix) Panels

4.3.15.2.2 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 46 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

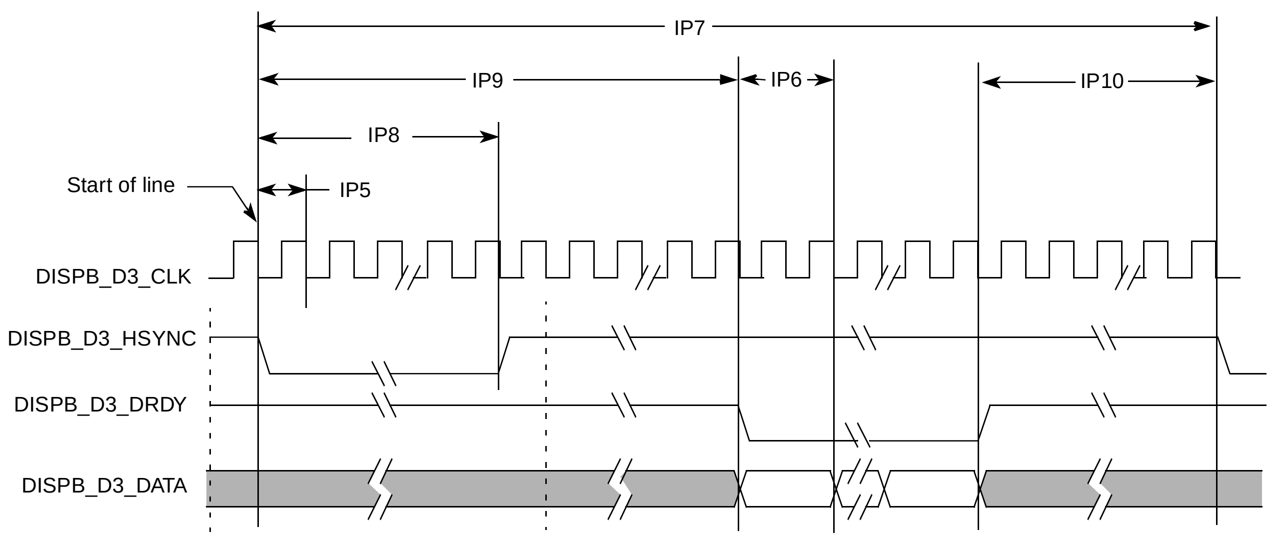


Figure 46. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 47 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

NOTE

HSP_CLK is the High-Speed Port Clock, which is the input to the Image Processing Unit (IPU). Its frequency is controlled by the Clock Control Module (CCM) settings. The HSP_CLK frequency must be greater than or equal to the AHB clock frequency.

The SCREEN_WIDTH, SCREEN_HEIGHT, H_SYNC_WIDTH, V_SYNC_WIDTH, BGXP, BGYP and V_SYNC_WIDTH_L parameters are programmed via the SDC_HOR_CONF, SDC_VER_CONF, SDC_BG_POS Registers. The FW and FH parameters are programmed for the corresponding DMA channel. The DISP3_IF_CLK_PER_WR, HSP_CLK_PERIOD and DISP3_IF_CLK_CNT_D parameters are programmed via the DI_DISP3_TIME_CONF, DI_HSP_CLK_PER and DI_DISP_ACC_CC Registers.

Figure 48 depicts the synchronous display interface timing for access level, and Table 45 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

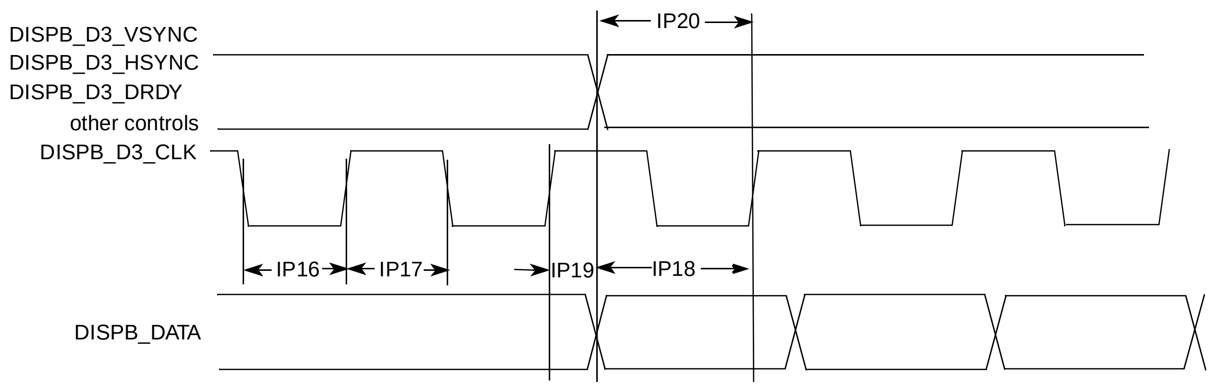


Figure 48. Synchronous Display Interface Timing Diagram—Access Level

Table 45. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min	Typ[1]	Max	Units
IP16	Display interface clock low time	Tckl	Tdicd–Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–3.5	Tdicp–Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd–3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$\mathrm{Tdicd} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP3\_IF\_CLK\_DOWN\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

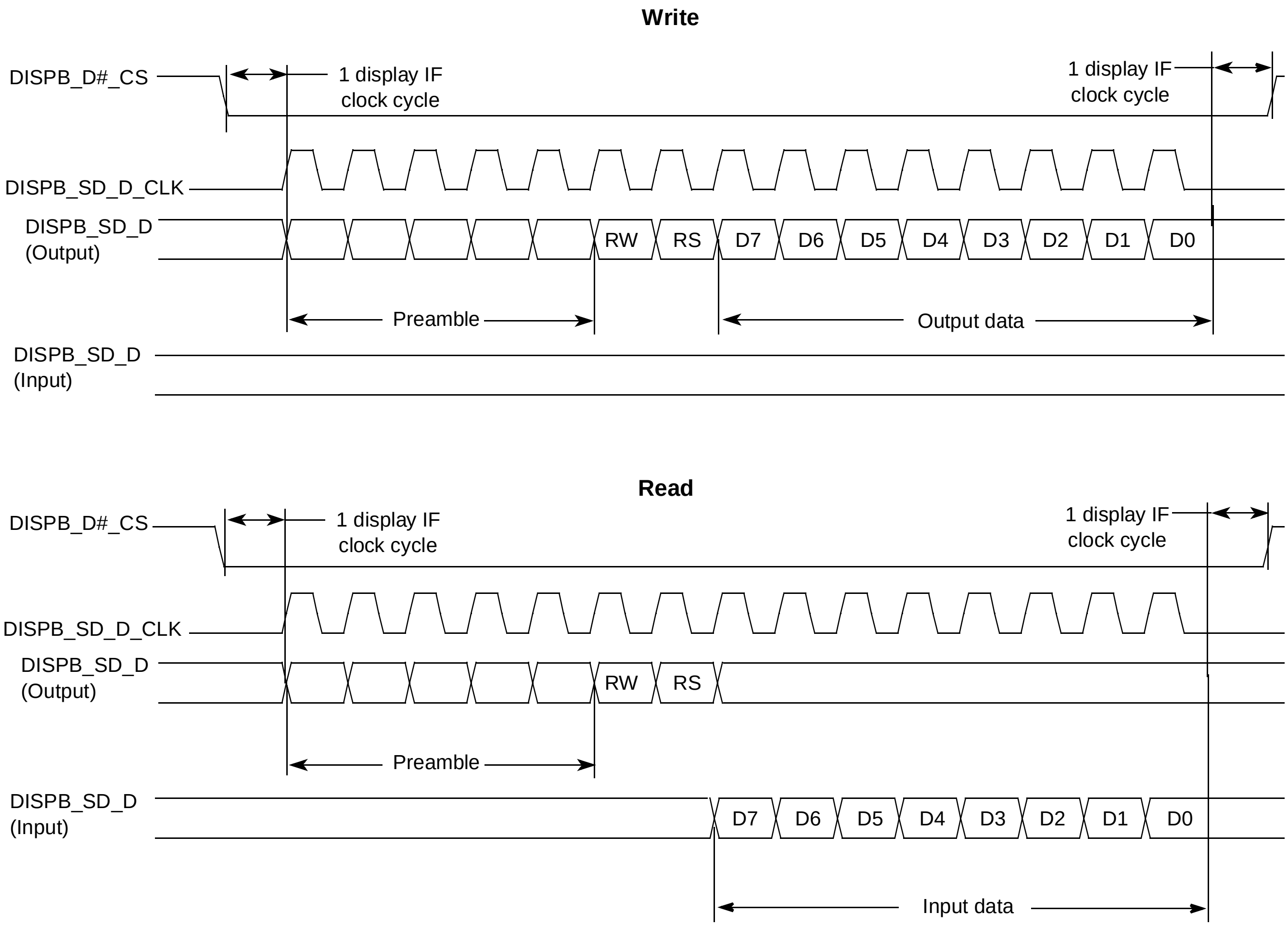


Figure 61. 4-Wire Serial Interface Timing Diagram

Figure 62 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

Table 48. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP56	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]–Tdicur–1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp–Tlbd–Tdicdr+1.5	—	Tdicpr–Tdicdr–1.5	ns
IP60	Write data setup time	Tds	Tdicdw–1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr–1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw–1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr–1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur–1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw–1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw–1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$\text{Tdicpr} = T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{\text{DISP\#\_IF\_CLK\_PER\_RD}}{\text{HSP\_CLK\_PERIOD}}\right]$$

3 Display interface clock period value for write:

$$\text{Tdicpw} = T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{\text{DISP\#\_IF\_CLK\_PER\_WR}}{\text{HSP\_CLK\_PERIOD}}\right]$$

4 Display interface clock down time for read:

$$\text{Tdicdr} = \frac{1}{2}T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{2 \cdot \text{DISP\#\_IF\_CLK\_DOWN\_RD}}{\text{HSP\_CLK\_PERIOD}}\right]$$

5 Display interface clock up time for read:

$$\text{Tdicur} = \frac{1}{2}T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{2 \cdot \text{DISP\#\_IF\_CLK\_UP\_RD}}{\text{HSP\_CLK\_PERIOD}}\right]$$

6 Display interface clock down time for write:

$$\text{Tdicdw} = \frac{1}{2}T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{2 \cdot \text{DISP\#\_IF\_CLK\_DOWN\_WR}}{\text{HSP\_CLK\_PERIOD}}\right]$$

7 Display interface clock up time for write:

$$\text{Tdicuw} = \frac{1}{2}T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{2 \cdot \text{DISP\#\_IF\_CLK\_UP\_WR}}{\text{HSP\_CLK\_PERIOD}}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

9 Data read point:

$$\text{Tdrp} = T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{\text{DISP\#\_READ\_EN}}{\text{HSP\_CLK\_PERIOD}}\right]$$

10 Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

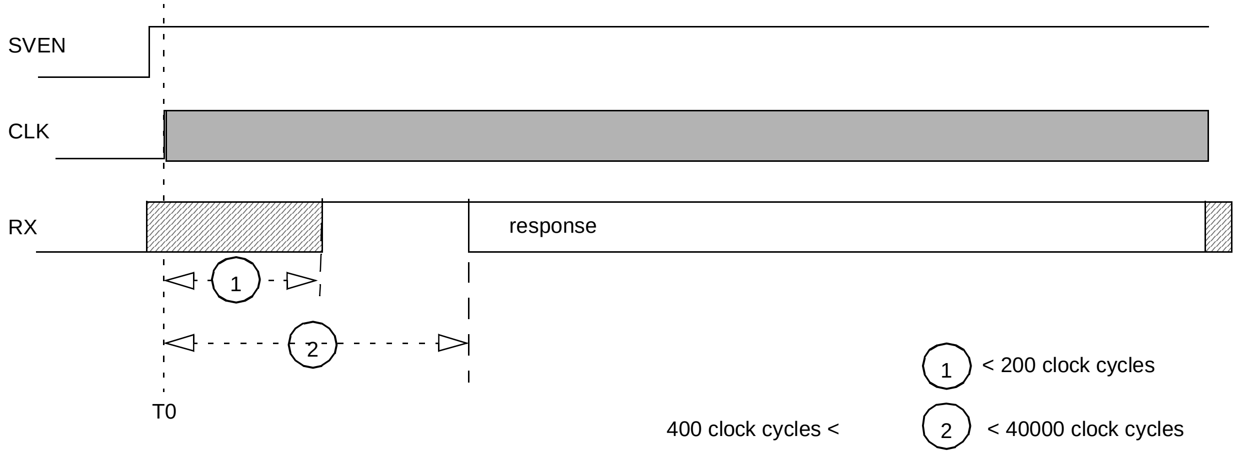


Figure 73. Internal-Reset Card Reset Sequence

4.3.20.2.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 74):

1. After powerup, the clock signal is enabled on CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
4. RST is set High (time T1)
5. RST must remain High for at least 40000 clock cycles after T1 and a response must be received on RX between 400 and 40000 clock cycles after T1.

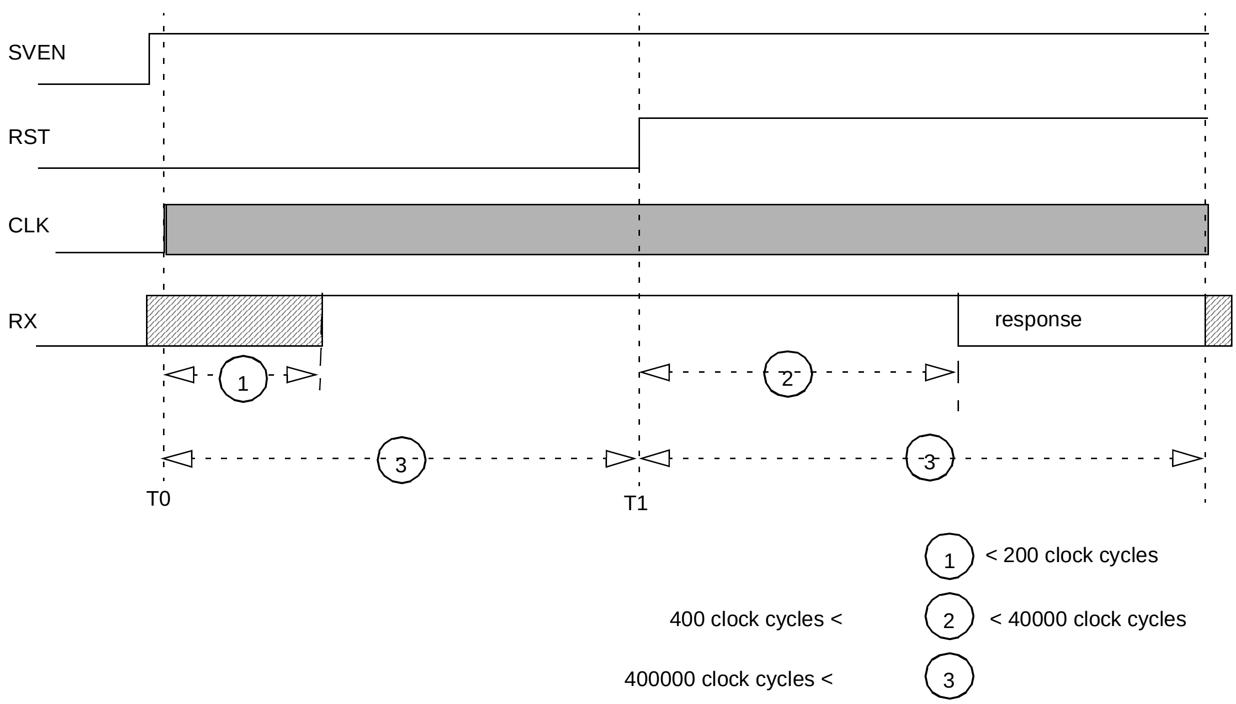


Figure 74. Active-Low-Reset Card Reset Sequence

4.3.22.3 SSI Transmitter Timing with External Clock

Figure 82 depicts the SSI transmitter timing with external clock, and Table 59 lists the timing parameters.

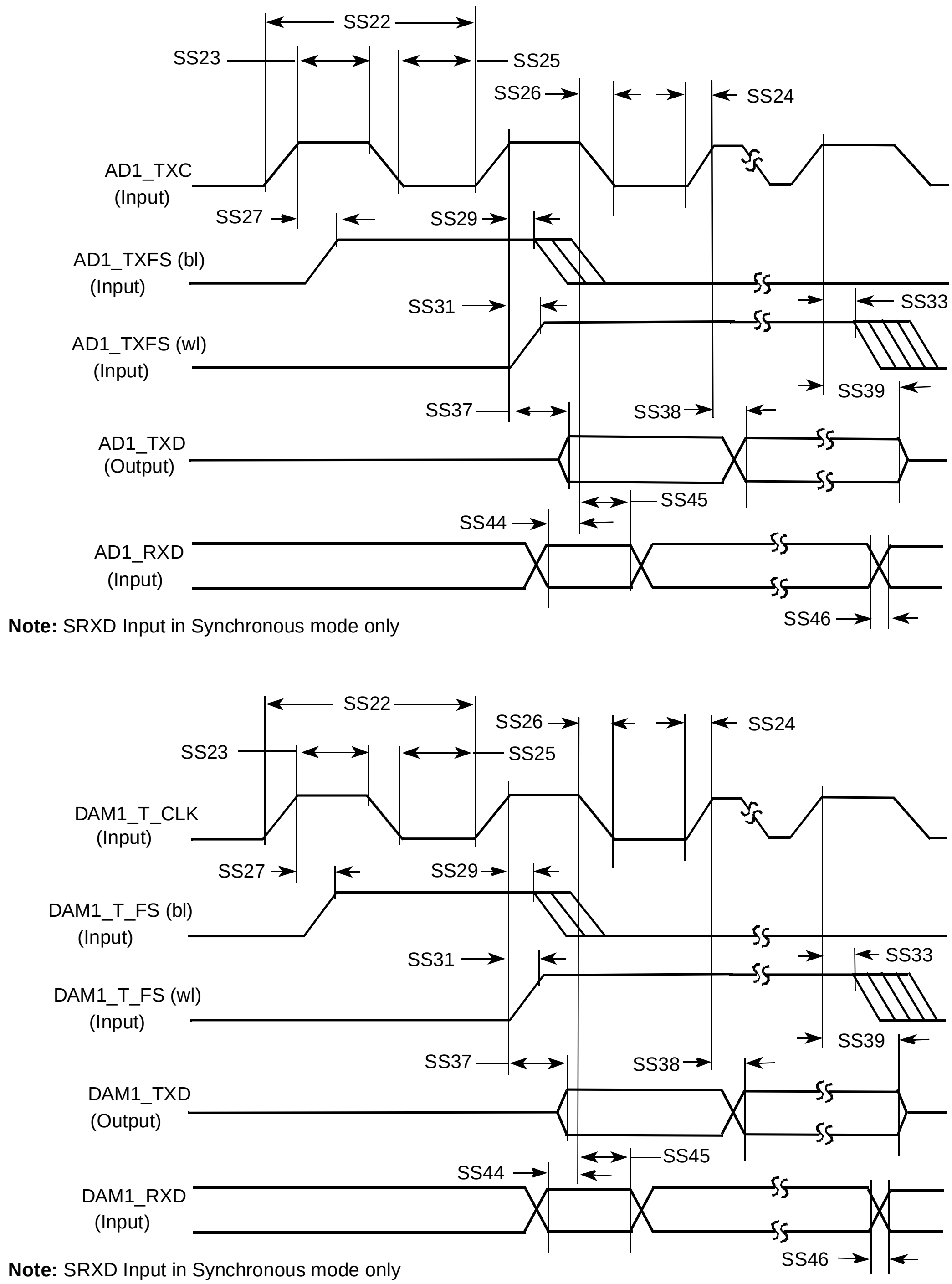


Figure 82. SSI Transmitter with External Clock Timing Diagram

5.1 MAPBGA Production Package 473 19 x 19 mm, 0.8 mm Pitch

This section contains the outline drawing, signal assignment map, and MAPBGA ground/power ID by ball grid location for the 473 19 x 19 mm, 0.8 mm pitch package.

5.1.1 Production Package Outline Drawing–19 x 19 mm 0.8 mm

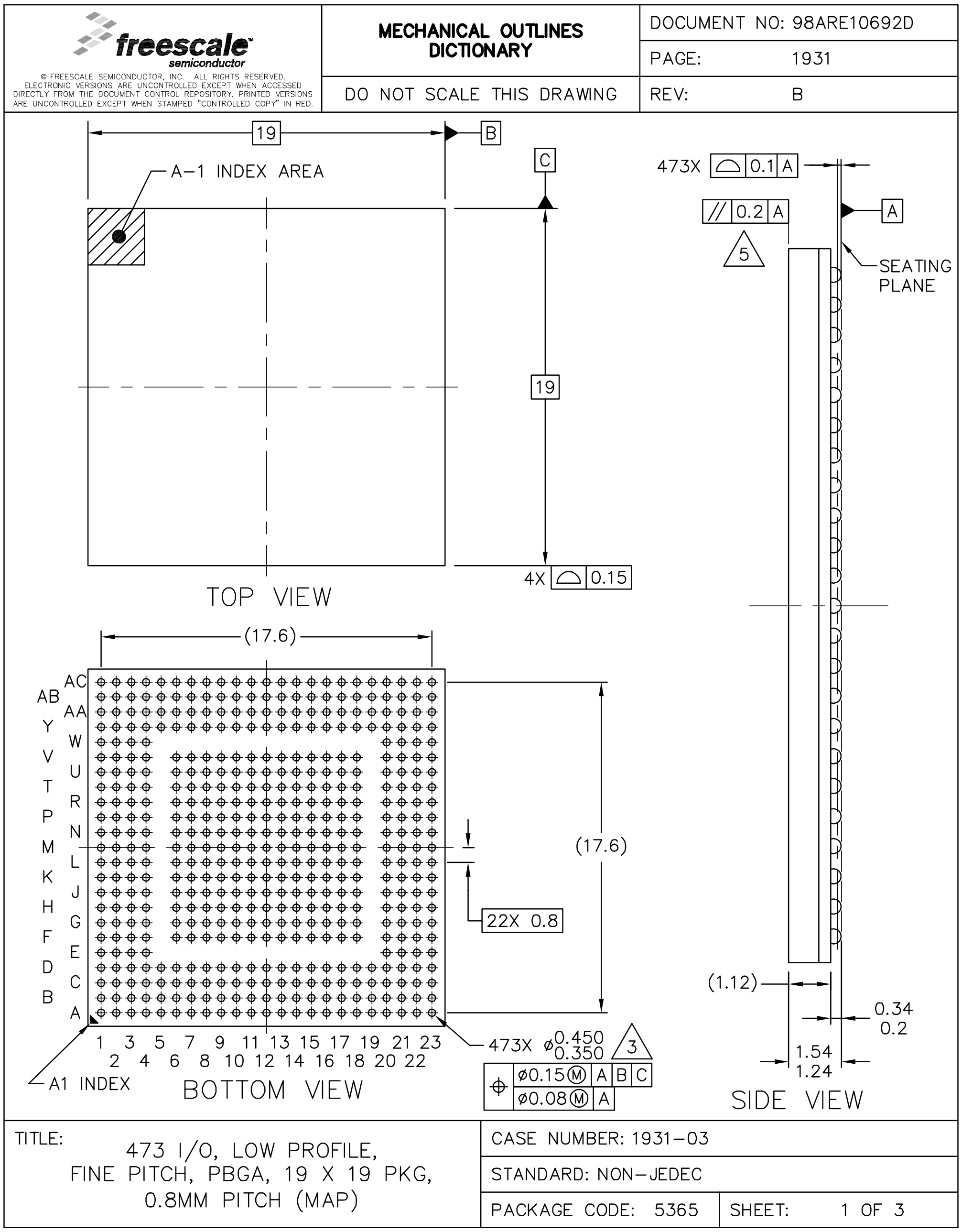


Figure 85. Production Package: Case 1931—0.8 mm Pitch

Table 63. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

[1] These contacts are not used and must be floated by the user.

5.1.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 64. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location	Signal ID	Ball Location
A0	Y6	CKIL	E21
A1	AC5	CLKO	C20
A10	V15	CLKSS	H17
A11	AB3	COMPARE	A20
A12	AA3	CONTRAST	N21
A13	Y3	CS0	U17
A14	Y15	CS1	Y22
A15	Y14	CS2	Y18
A16	V14	CS3	Y19
A17	Y13	CS4	Y20
A18	V13	CS5	AA21
A19	Y12	CSI_D10	K21
A2	AB5	CSI_D11	K22
A20	V12	CSI_D12	K23
A21	Y11	CSI_D13	L20
A22	V11	CSI_D14	L18
A23	Y10	CSI_D15	L21
A24	Y9	CSI_D4	J20
A25	Y8	CSI_D5	J21
A3	AA5	CSI_D6	L17
A4	Y5	CSI_D7	J22
A5	AC4	CSI_D8	J23
A6	AB4	CSI_D9	K20
A7	AA4	CSI_HSYNC	H22
A8	Y4	CSI_MCLK	H20
A9	AC3	CSI_PIXCLK	H23
ATA_CS0	E1	CSI_VSYNC	H21
ATA_CS1	G4	CSPI1_MISO	N2
ATA_DIOR	E3	CSPI1_MOSI	N1
ATA_DIOW	H6	CSPI1_SCLK	M4
ATA_DMACK	E2	CSPI1_SPI_RDY	M1
$\overline{\text{ATA\_RESET}}$	F3	CSPI1_SS0	M2
BATT_LINE	F6	CSPI1_SS1	N6
BCLK	W20	CSPI1_SS2	M3
BOOT_MODE0	F17	CSPI2_MISO	B4
BOOT_MODE1	C21	CSPI2_MOSI	D5