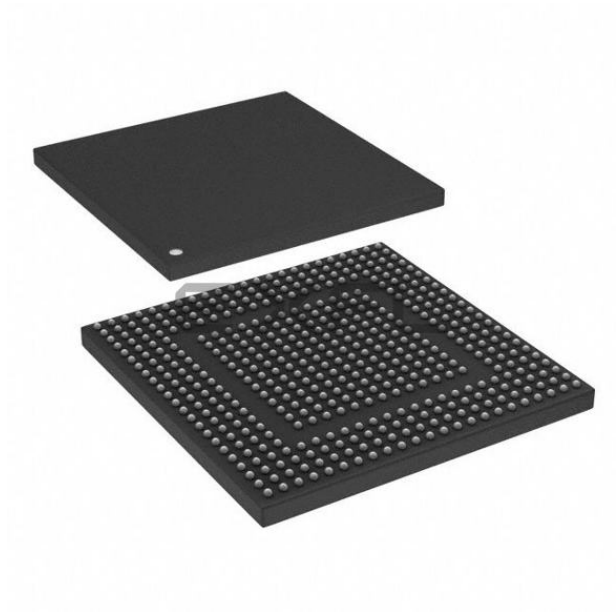

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31cvmn4d

- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with Hit-Under-Miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector Floating Point co-processor (VFP) for 3D graphics and other floating-point applications hardware acceleration
- ETM™ and JTAG-based debug support

2.1.1 Memory System

The ARM1136JF-S complex includes 16 KB Instruction and 16 KB Data L1 caches. It connects to the MCIMX31C L2 unified cache through 64-bit instruction (read-only), 64-bit data read/write (bi-directional), and 64-bit data write interfaces.

The embedded 16K SRAM can be used for audio streaming data to avoid external memory accesses for the low-power audio playback, for security, or for other applications. There is also a 32-KB ROM for bootstrap code and other frequently-used code and data.

A ROM patch module provides the ability to patch the internal ROM. It can also initiate an external boot by overriding the boot reset sequence by a jump to a configurable address.

Table 2 shows information about the MCIMX31C core in tabular form.

Table 2. MCIMX31C Core

Core Acronym	Core Name	Brief Description	Integrated Memory Includes
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ Platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 x 5 multi-layer AHB crossbar switch (MAX), and a Vector Floating Processor (VFP). The MCIMX31C provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16 Kbyte Instruction Cache • 16 Kbyte Data Cache • 128 Kbyte L2 Cache • 32 Kbyte ROM • 16 Kbyte RAM

Table 4. MCIMX31C Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, “Absolute Maximum Ratings”	on page 10
Table 6, “Thermal Resistance Data—19 × 19 mm Package”	on page 10
Table 7, “Operating Ranges”	on page 12
Table 8, “Specific Operating Ranges for Silicon Revision 2.0 and 2.0.1”	on page 12
Table 9, “Interface Frequency”	on page 13
Section 4.1.1, “Supply Current Specifications”	on page 14
Section 4.2, “Supply Power-Up/Power-Down Requirements and Restrictions”	on page 15

CAUTION

Stresses beyond those listed under Table 5, "Absolute Maximum Ratings," on page 10 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 7, "Operating Ranges," on page 12 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	–0.5	1.47	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.1	V
Input Voltage Range	V_{Imax}	–0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	–40	125	^{o}C
ESD Damage Immunity:				
Human Body Model (HBM)	V_{esd}	—	H1C[1]	V
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	C2[2]	
Offset voltage allowed in run mode between core supplies.	V_{core_offset}[3]	—	15	mV

1 HBM ESD classification level according to the AEC-Q100-002-Rev-D standard.

2 Integrated circuit CDM ESD classification level according to the AEC-Q100-011-Rev-B standard.

3 The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 6 provides the thermal resistance data for the 19 × 19 mm, 0.8 mm pitch package.

Table 6. Thermal Resistance Data—19 × 19 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	46	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	29	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	38	°C/W	1, 2, 3

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31C board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power-up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31C (worst-case scenario)

4.2.1 Powering Up

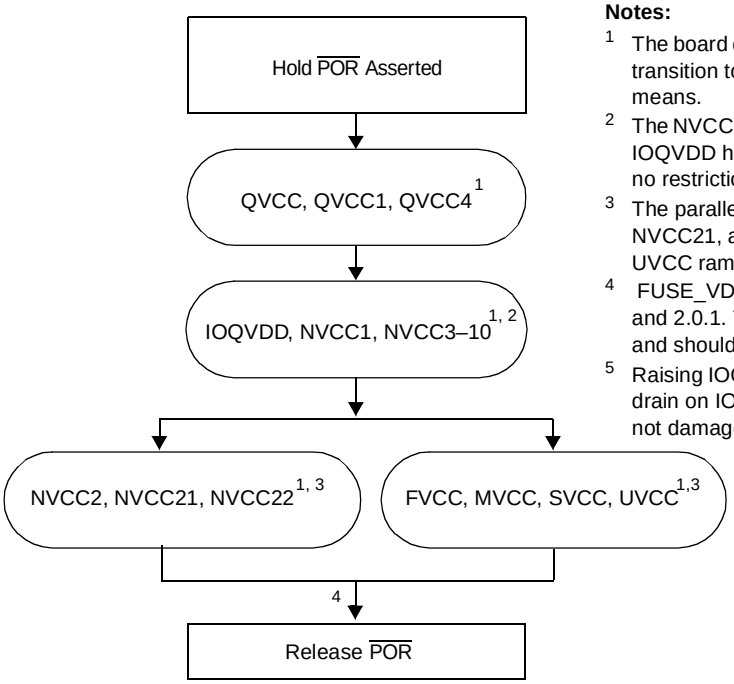
The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power-up sequence. Power-up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 and Figure 3 show two options of the power-up sequence.

NOTE

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.



Notes:

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent.
4. FUSE_VDD should not be driven on power-up for Silicon Revision 2.0 and 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.
5. Raising IOQVDD before NVCC21 produces a slight increase in current drain on IOQVDD of approximately 3–5 mA. The current increase will not damage the IC. Refer to Errata ID TLSbo91750 for details.

Figure 2. Option 1 Power-Up Sequence for Silicon Revision 2.0 and 2.0.1

Table 14. AC Electrical Characteristics of Slow[1] General I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.92 1.5	1.95 2.98	3.17 4.75	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	1.52 2.75	—	4.81 8.42	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	2.79 5.39	—	8.56 16.43	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

Table 15. AC Electrical Characteristics of Fast[1] General I/O [2]

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.68 1.34	1.33 2.6	2.07 4.06	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.91 1.79	1.77 3.47	2.74 5.41	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.36 2.68	2.64 5.19	4.12 8.11	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

2 Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

Table 16. AC Electrical Characteristics of DDR I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (DDR Drive)[1]	tpr	25 pF 50 pF	0.51 0.97	0.82 1.58	1.28 2.46	ns
	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.67 1.29	1.08 2.1	1.69 3.27	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.99 1.93	1.61 3.13	2.51 4.89	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.96 3.82	3.19 6.24	4.99 9.73	ns

1 Use of DDR Drive can result in excessive overshoot and ringing.

4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 17 shows clock amplifier electrical characteristics.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

4.3.5.1 Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 21 shows ATA timing parameters.

Table 21. ATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	peripheral clock frequency
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	transceiver
tbuf	Max buffer propagation delay	transceiver
tcable1	Cable propagation delay for ata_data	cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	cable

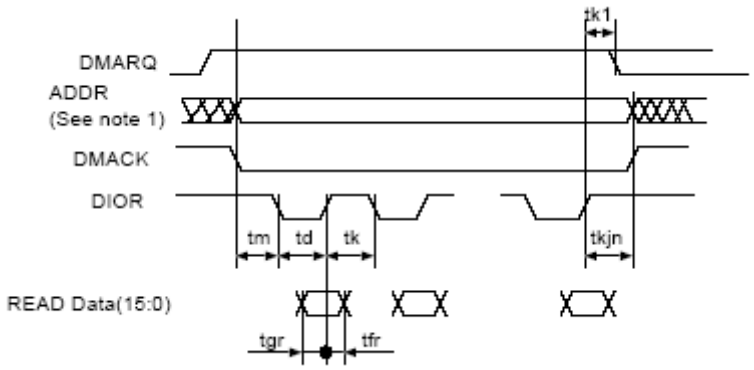


Figure 12. MDMA Read Timing Diagram

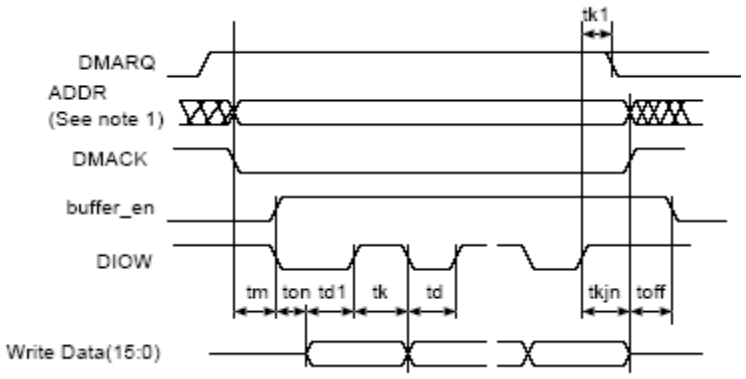


Figure 13. MDMA Write Timing Diagram

Table 24. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 12, Figure 13	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

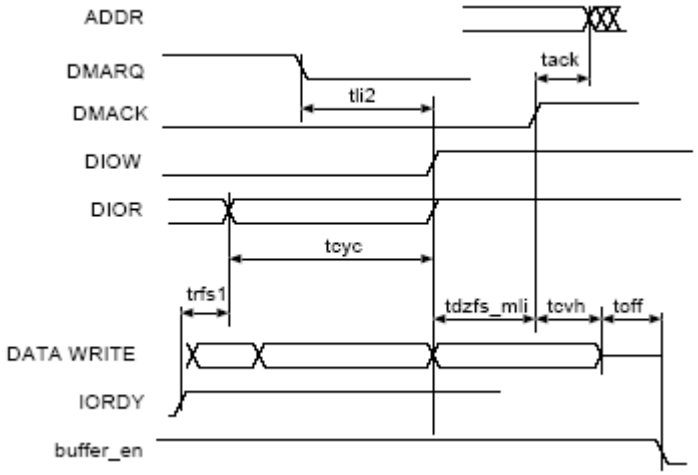


Figure 19. UDMA Out Device Terminates Transfer Timing Diagram

Table 26. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 17, Figure 18, Figure 19	Value	Controlling Variable
tack	tack	tack (min) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env * T) – (tskew1 + tskew2) tenv (max) = (time_env * T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs * T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh * T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc * T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc * 2 * T	time_cyc
trfs1	trfs	trfs = 1.6 * T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs * T – (tskew1)	time_dzfs
tss	tss	tss = time_ss * T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) * T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

4.3.6 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. Please refer to their respective electrical specifications.

4.3.7 CSPI Electrical Specifications

This section describes the electrical information of the CSPI.

4.3.7.1 CSPI Timing

Figure 20 and Figure 21 depict the master mode and slave mode timings of CSPI, and Table 27 lists the timing parameters.

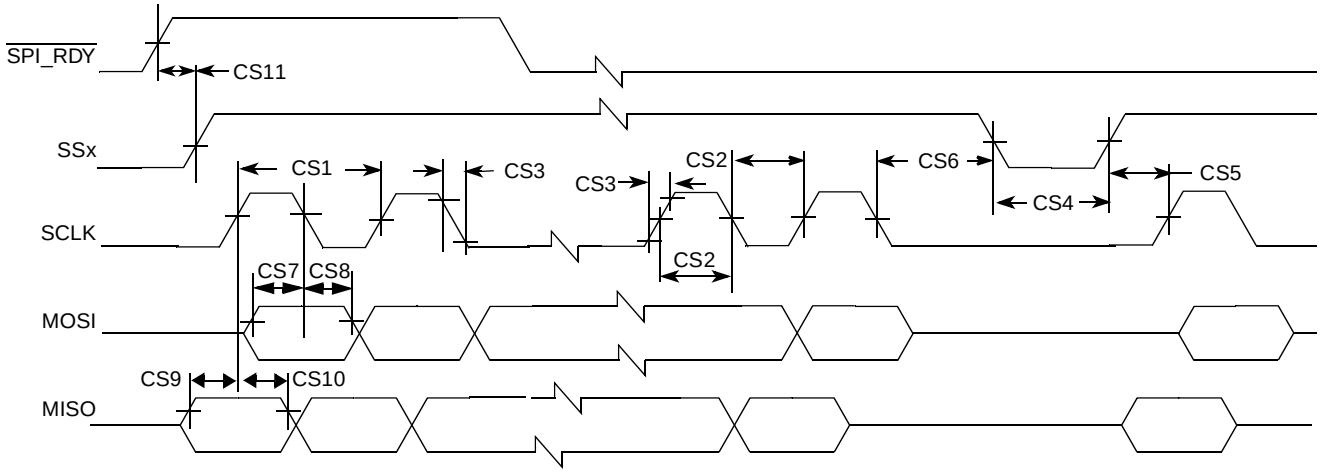


Figure 20. CSPI Master Mode Timing Diagram

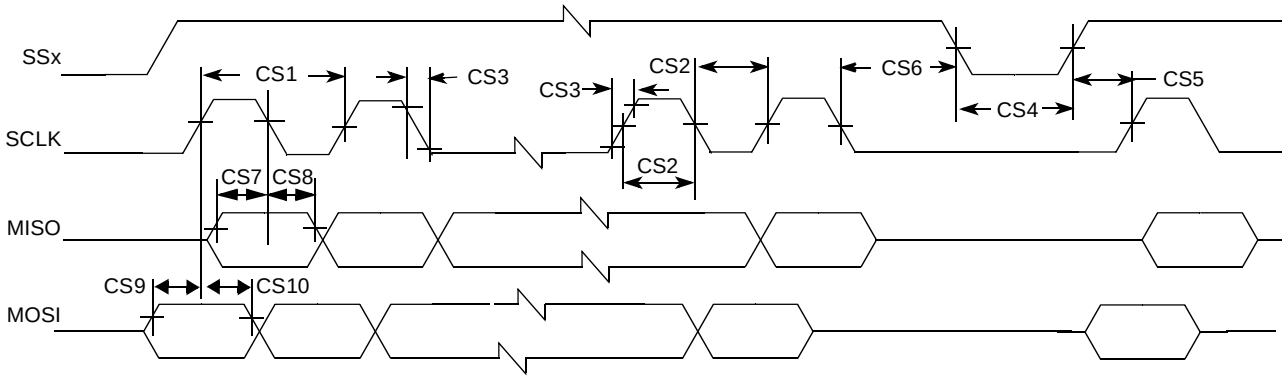


Figure 21. CSPI Slave Mode Timing Diagram

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

NOTE

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 26 depicts the timing of the WEIM module, and Table 30 lists the timing parameters.

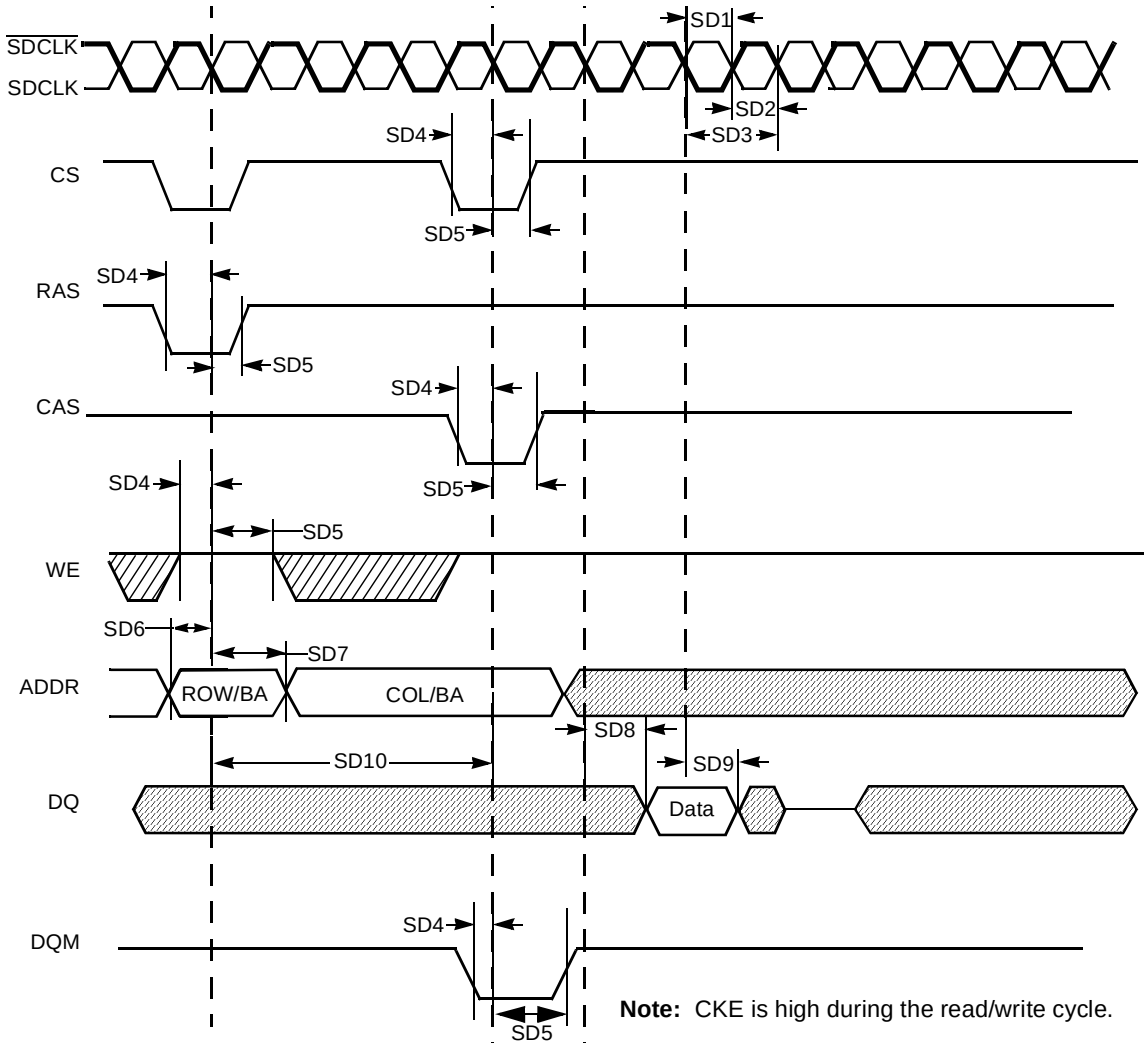


Figure 33. SDRAM Read Cycle Timing Diagram

Table 31. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

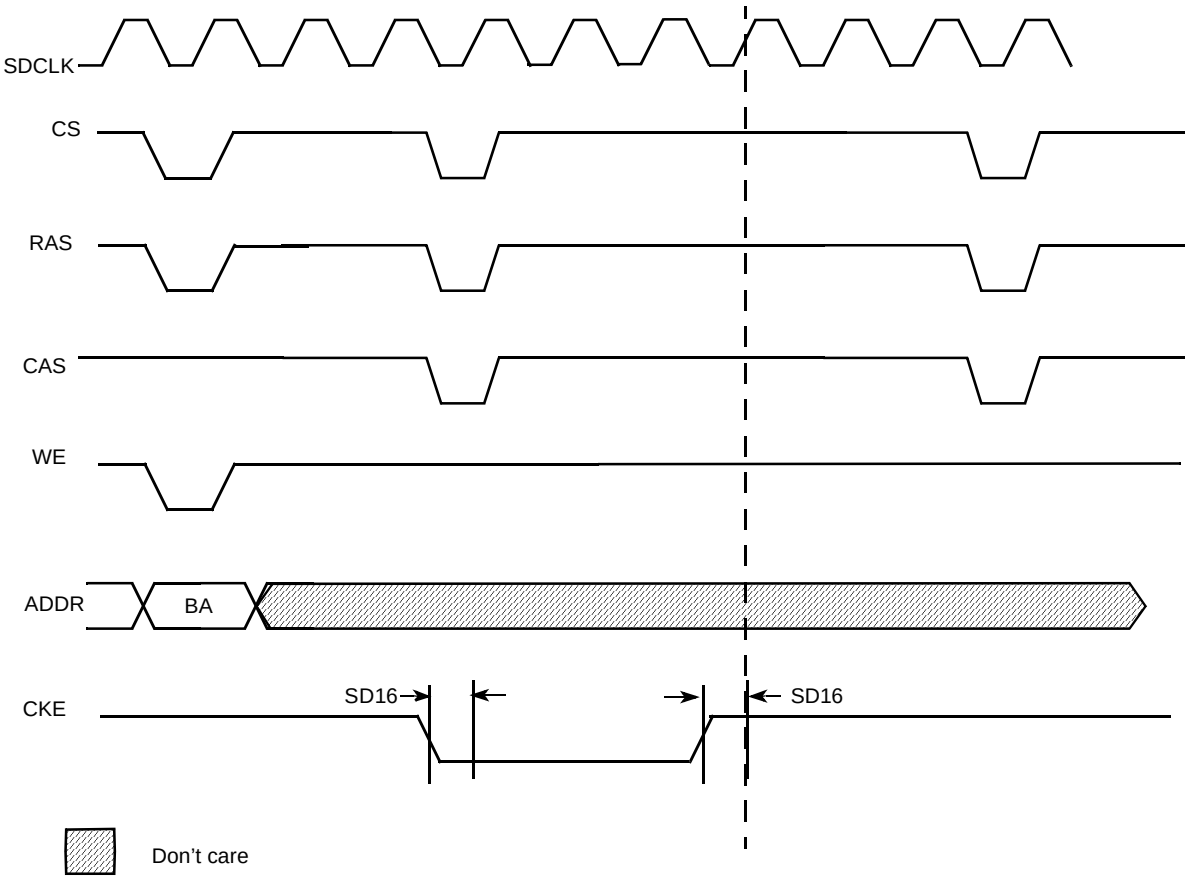


Figure 36. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 34. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

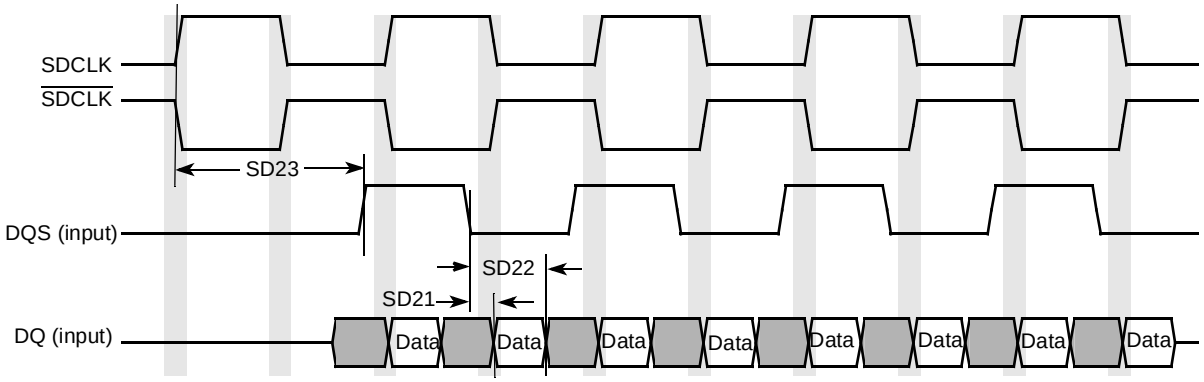


Figure 38. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 36. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 39 depicts the TRACECLK timings of ETM, and Table 37 lists the timing parameters.

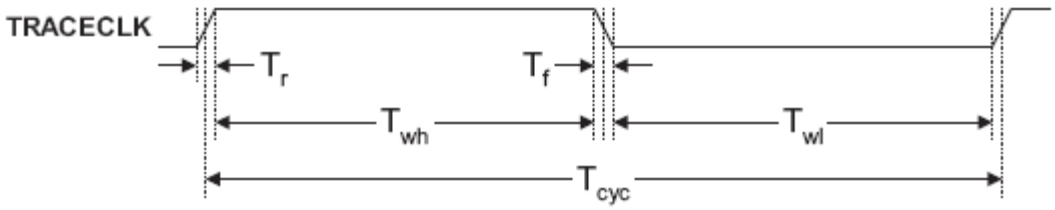


Figure 39. ETM TRACECLK Timing Diagram

NOTE

HSP_CLK is the High-Speed Port Clock, which is the input to the Image Processing Unit (IPU). Its frequency is controlled by the Clock Control Module (CCM) settings. The HSP_CLK frequency must be greater than or equal to the AHB clock frequency.

The SCREEN_WIDTH, SCREEN_HEIGHT, H_SYNC_WIDTH, V_SYNC_WIDTH, BGXP, BGYP and V_SYNC_WIDTH_L parameters are programmed via the SDC_HOR_CONF, SDC_VER_CONF, SDC_BG_POS Registers. The FW and FH parameters are programmed for the corresponding DMA channel. The DISP3_IF_CLK_PER_WR, HSP_CLK_PERIOD and DISP3_IF_CLK_CNT_D parameters are programmed via the DI_DISP3_TIME_CONF, DI_HSP_CLK_PER and DI_DISP_ACC_CC Registers.

Figure 48 depicts the synchronous display interface timing for access level, and Table 45 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

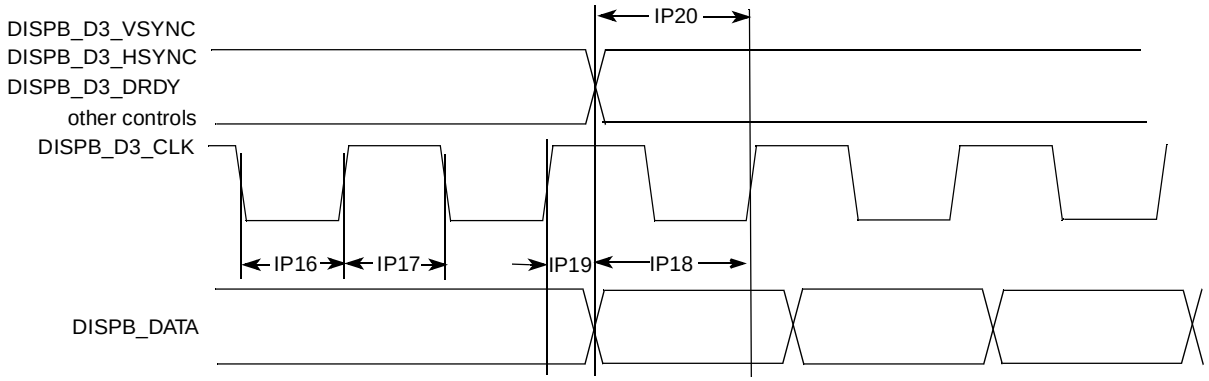


Figure 48. Synchronous Display Interface Timing Diagram—Access Level

Table 45. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min	Typ[1]	Max	Units
IP16	Display interface clock low time	Tckl	Tdicd–Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–3.5	Tdicp–Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd–3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

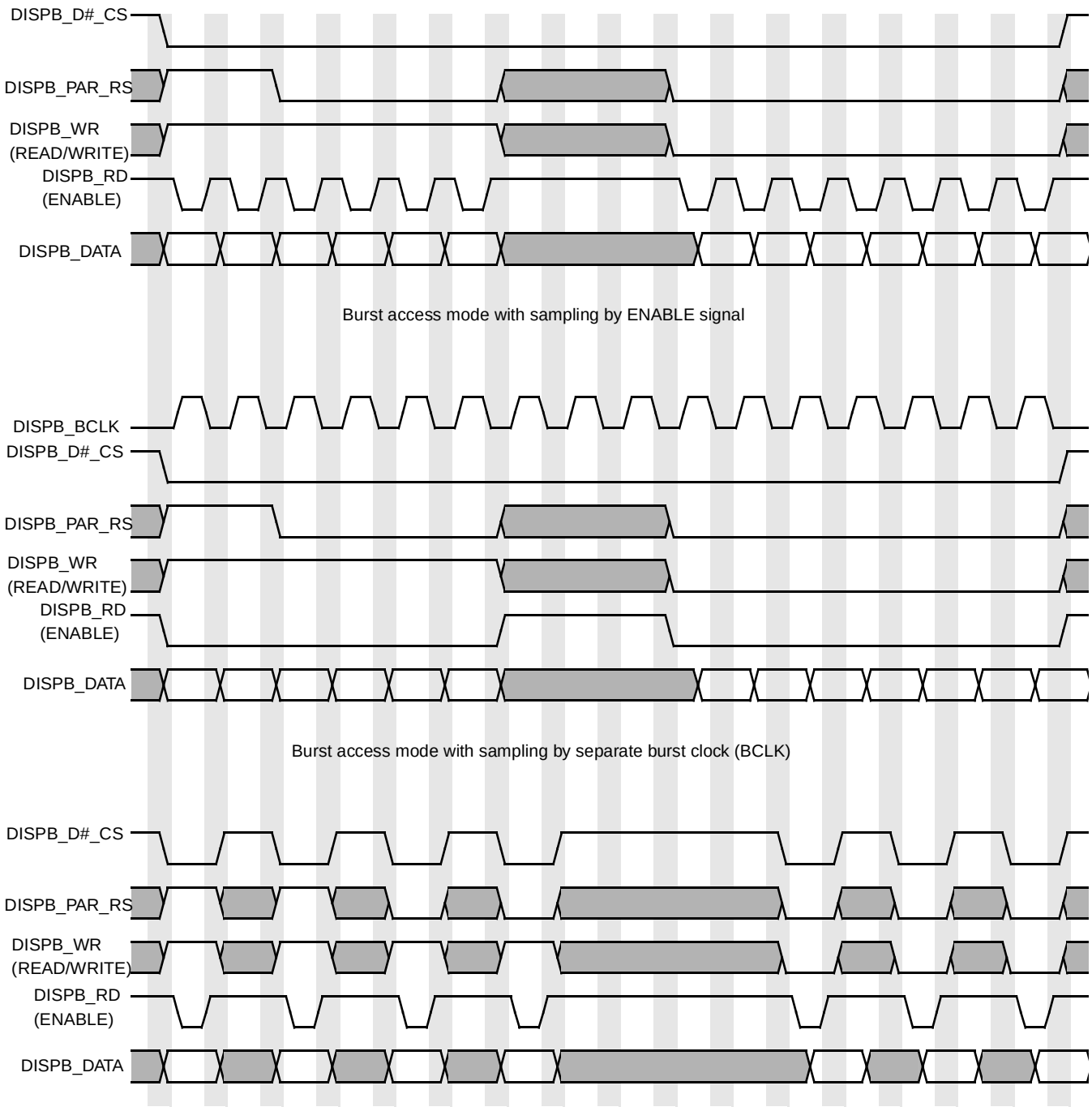


Figure 54. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the DI_DISP0_TIME_CONF_3, DI_DISP1_TIME_CONF_3, DI_DISP2_TIME_CONF_3 Registers. Figure 55 shows timing of the parallel interface with read wait states.

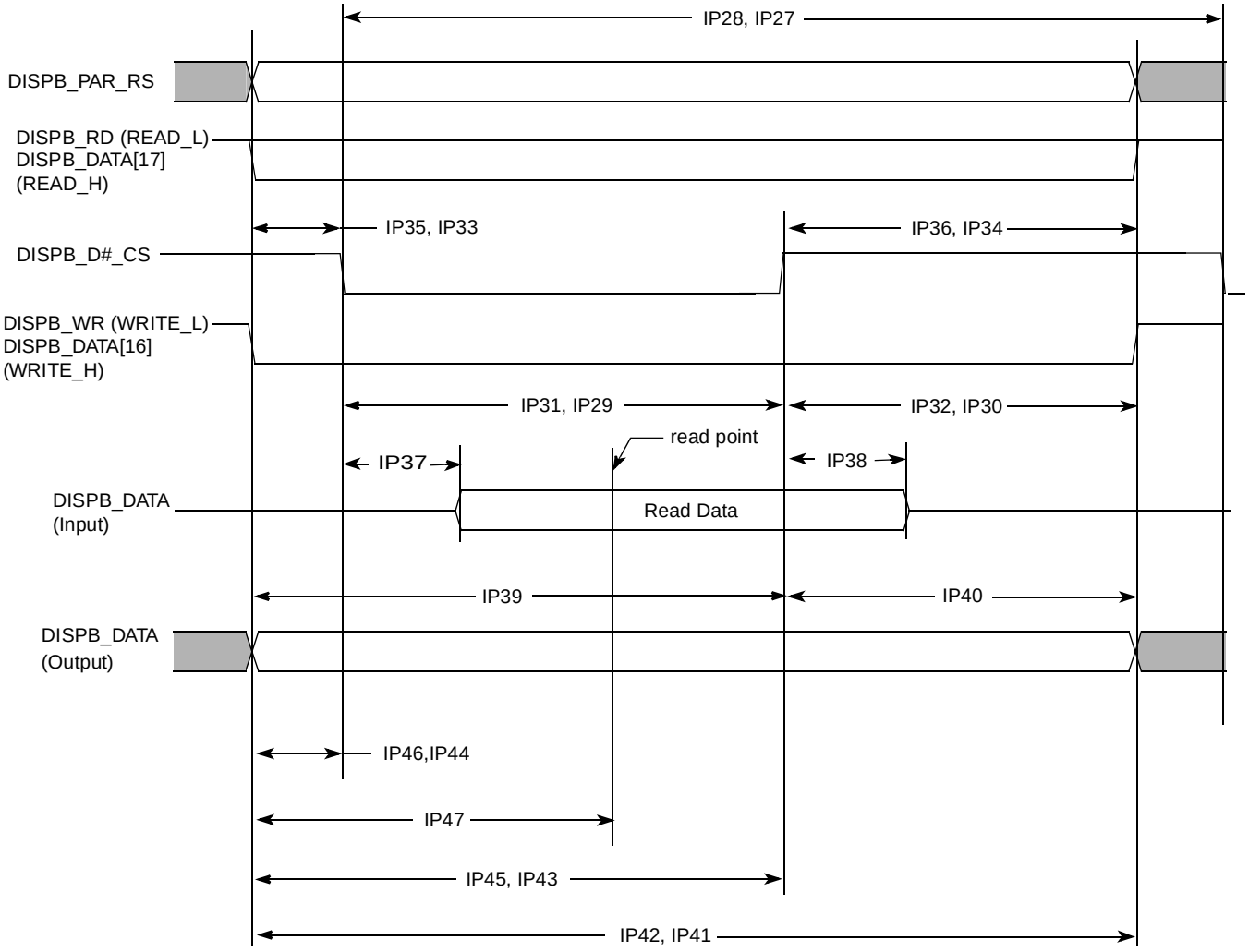


Figure 56. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

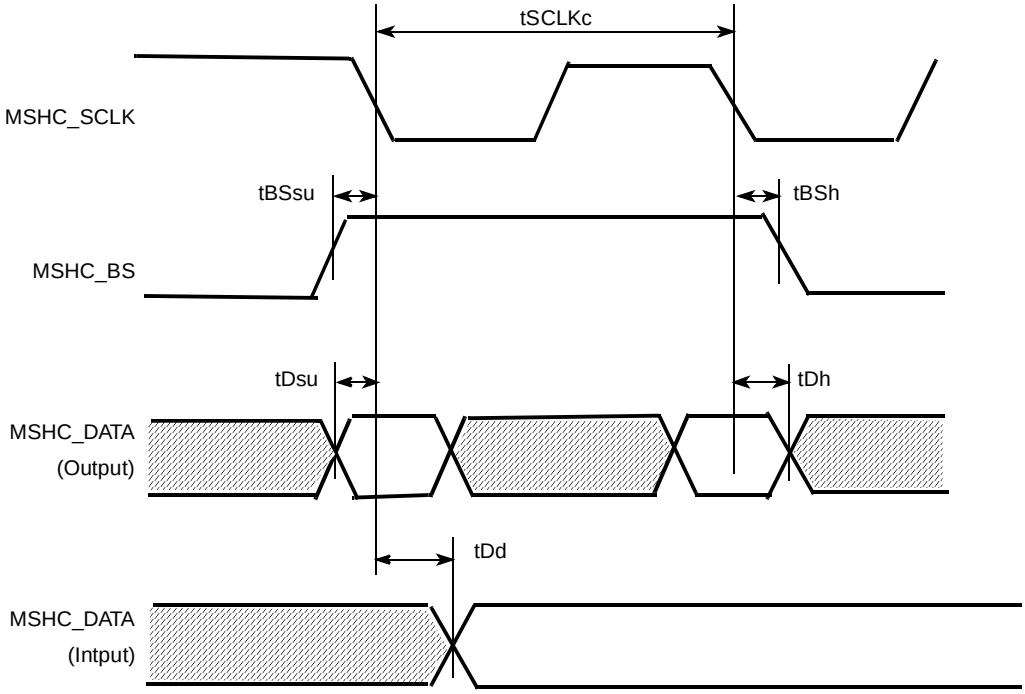


Figure 67. Transfer Operation Timing Diagram (Parallel)

NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31C timing.

Table 49. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V. See NVCC restrictions described in Table 7, "Operating Ranges," on page 12.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the aim card will be used by the SIM card to recover the clock from the data much like a standard UART. All six (or 5 in case bi directional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other.

There are no required timing relationships between the signals in normal mode, but there are some in two specific cases: reset and power down sequences.

4.3.20.1 General Timing Requirements

Figure 72 shows the timing of the SIM module, and Figure 54 lists the timing parameters.

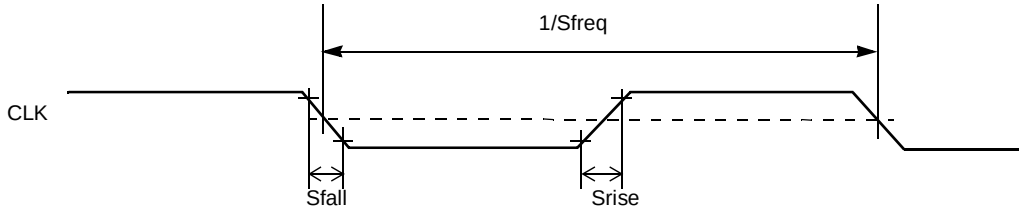


Figure 72. SIM Clock Timing Diagram

Table 54. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM CLK Rise Time [2]	S_{rise}	—	20	ns
3	SIM CLK Fall Time [3]	S_{fall}	—	20	ns
4	SIM Input Transition Time (RX, SIMPD)	S_{trans}	—	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

4.3.20.2 Reset Sequence

4.3.20.2.1 Cards with Internal Reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 73):

- After powerup, the clock signal is enabled on SGCLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

5 Package Information and Pinout

This section includes the contact assignment information and mechanical package drawing for the MCIMX31C.

Table 64. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
RXD1	C9
RXD2	A12
SCK3	P1
SCK4	G6
SCK5	D4
SDCKE0	Y17
SDCKE1	V16
SDCLK	AC20
$\overline{\text{SDCLK}}$	AC19
SDQS0	AB16
SDQS1	AB12
SDQS2	AB9
SDQS3	AB6
SDWE	AB20
SER_RS	P23
SFS3	P2
SFS4	D3
SFS5	G7
SFS6	P4
SIMPD0	B18
SJC_MOD	C17
SRST0	C18
SRX0	A19
SRXD3	N3
SRXD4	C3
SRXD5	C4
SRXD6	R1
STX0	F16
STXD3	N4
STXD4	B3
STXD5	D1
STXD6	P3
SVEN0	D17
TCK	F14
TDI	A18
TDO	B17
TMS	C16

Signal ID	Ball Location
SD7	AB15
SD8	AC15
SD9	AA14
SDBA0	AA6
SDBA1	Y7
TRSTB	F15
TXD1	D9
TXD2	F11
USB_BYP	C8
USB_OC	B8
USB_PWR	A8
USBH2_CLK	L1
USBH2_DATA0	M6
USBH2_DATA1	K1
USBH2_DIR	L2
USBH2_NXT	L4
USBH2_STP	L3
USBOTG_CLK	D8
USBOTG_DATA0	G8
USBOTG_DATA1	C7
USBOTG_DATA2	A6
USBOTG_DATA3	F8
USBOTG_DATA4	D7
USBOTG_DATA5	B6
USBOTG_DATA6	A5
USBOTG_DATA7	C6
USBOTG_DIR	A7
USBOTG_NXT	B7
USBOTG_STP	F9
VPG0	G21
VPG1	G22
VSTBY	H18
VSYNC0	L22
VSYNC3	N20
WATCHDOG_RST	B21
WRITE	N22

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

- *MCIMX31 Product Brief* (order number MCIMX31PB)
- *MCIMX31 Reference Manual* (order number MCIMX31RM)

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