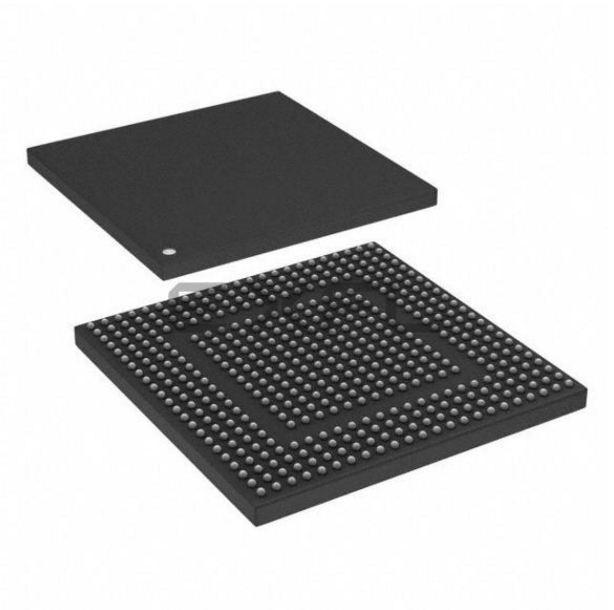

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM1136JF-S |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Multimedia; GPU, IPU, MPEG-4, VFP |
| RAM Controllers | DDR |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keyboard, Keypad, LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 2.0 (3) |
| Voltage - I/O | 1.8V, 2.0V, 2.5V, 2.7V, 3.0V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory |
| Package / Case | 473-LFBGA |
| Supplier Device Package | 473-LFBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31cvmn4dr2 |

Table 7 provides the operating ranges.

### NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

### CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

**Table 7. Operating Ranges**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| QVCC, QVCC1, QVCC4 | Core Operating Voltage[1,2] $0 \leq f_{ARM} \leq 400$ MHz | 1.22 | 1.47 | V |
| | State Retention Voltage[3] | 0.95 | — | |
| NVCC1, NVCC3–10 | I/O Supply Voltage, except DDR[4] | 1.75 | 3.1 | V |
| NVCC2, NVCC21, NVCC22 | I/O Supply Voltage, DDR only | 1.75 | 1.95 | V |
| FVCC, MVCC, SVCC, UVCC | PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[5] | 1.3 | 1.47 | V |
| IOQVDD | On-device Level Shifter Supply Voltage | 1.6 | 1.9 | V |
| FUSE_VDD | Fusebox read Supply Voltage[6] | — | — | V |
| | Fusebox write (program) Supply Voltage[7] | 3.0 | 3.3 | V |
| $T_A$ | Operating Ambient Temperature Range | –40 | 85 | $^oC$ |
| $T_j$ | Operating Junction Temperature Range | — | 105 | $^oC$ |

1 Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

2 The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID

3 The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode.

4 Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

5 PLL voltage must not be altered after power-up, otherwise the PLL will be unstable and lose lock. To minimize inducing noise on the PLL supply line, source the voltage from a low-noise, dedicated supply. PLL parameters in Table 28, "DPLL Specifications," on page 31, are guaranteed over the entire specified voltage range.

6 In read mode, FUSE_VDD can be floated or grounded.

7 Fuses might be inadvertently blown if written to while the voltage is below this minimum.

**Table 8. Specific Operating Ranges for Silicon Revision 2.0 and 2.0.1**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| FUSE_VDD | Fusebox read Supply Voltage[1] | — | — | V |
| | Fusebox write (program) Supply Voltage[2] | 3.0 | 3.3 | V |

## 4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31C board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power-up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31C (worst-case scenario)

### 4.2.1 Powering Up

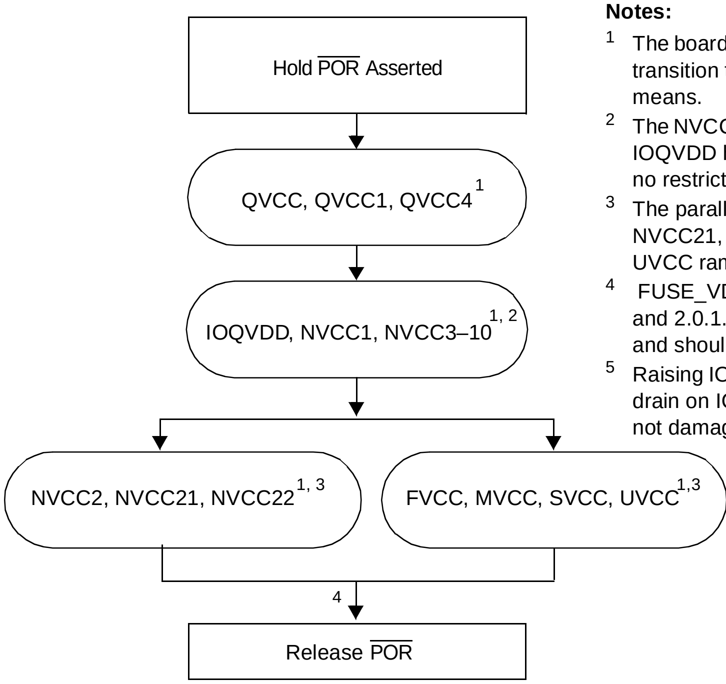
The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power-up sequence. Power-up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 and Figure 3 show two options of the power-up sequence.

**NOTE**

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

**CAUTION**

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.




**Notes:**

1 The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.

2 The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.

3 The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent.

4 FUSE_VDD should not be driven on power-up for Silicon Revision 2.0 and 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.

5 Raising IOQVDD before NVCC21 produces a slight increase in current drain on IOQVDD of approximately 3–5 mA. The current increase will not damage the IC. Refer to Errata ID TLSbo91750 for details.

**Figure 2. Option 1 Power-Up Sequence for Silicon Revision 2.0 and 2.0.1**

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

### 4.3.5.1 Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 21 shows ATA timing parameters.

**Table 21. ATA Timing Parameters**

| Name | Description | Value/ Contributing Factor[1] |
|---|---|---|
| T | Bus clock period (ipg_clk_ata) | peripheral clock frequency |
| ti_ds | Set-up time ata_data to ata_iordy edge (UDMA-in only)<br>UDMA0<br>UDMA1<br>UDMA2, UDMA3<br>UDMA4<br>UDMA5 | <br>15 ns<br>10 ns<br>7 ns<br>5 ns<br>4 ns |
| ti_dh | Hold time ata_iordy edge to ata_data (UDMA-in only)<br>UDMA0, UDMA1, UDMA2, UDMA3, UDMA4<br>UDMA5 | <br>5.0 ns<br>4.6 ns |
| tco | Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en | 12.0 ns |
| tsu | Set-up time ata_data to bus clock L-to-H | 8.5 ns |
| tsui | Set-up time ata_iordy to bus clock H-to-L | 8.5 ns |
| thi | Hold time ata_iordy to bus clock H to L | 2.5 ns |
| tskew1 | Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | 7 ns |
| tskew2 | Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | transceiver |
| tskew3 | Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read) | transceiver |
| tbuf | Max buffer propagation delay | transceiver |
| tcable1 | Cable propagation delay for ata_data | cable |
| tcable2 | Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack | cable |
| tskew4 | Max difference in cable propagation delay between ata_iordy and ata_data (read) | cable |

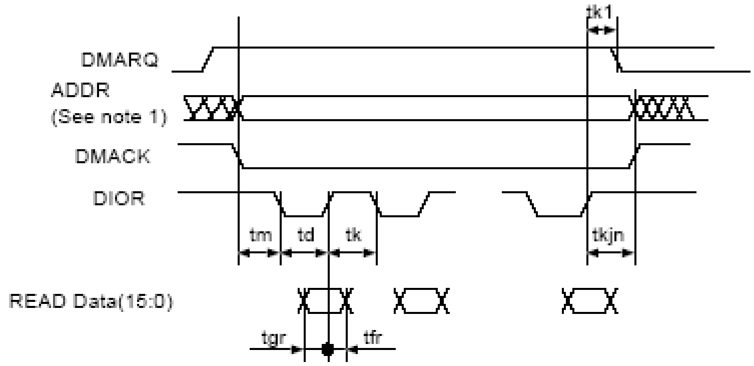



Figure 12. MDMA Read Timing Diagram

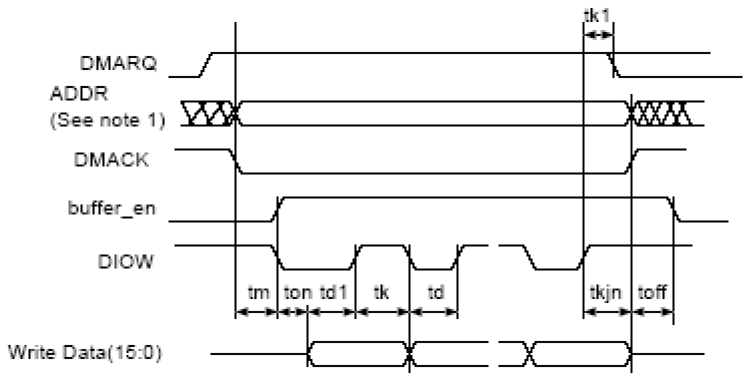



Figure 13. MDMA Write Timing Diagram

Table 24. MDMA Read and Write Timing Parameters

| ATA Parameter | Parameter from Figure 12, Figure 13 | Value | Controlling Variable |
|---|---|---|---|
| tm, ti | tm | tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5) | time_m |
| td | td, td1 | td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6) | time_d |
| tk | tk | tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6) | time_k |
| t0 | — | t0 (min) = (time_d + time_k) * T | time_d, time_k |
| tg(read) | tgr | tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2<br>tgr.(min-drive) = td – te(drive) | time_d |
| tf(read) | tfr | tfr (min-drive) = 0 | — |
| tg(write) | — | tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5) | time_d |
| tf(write) | — | tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6) | time_k |
| tL | — | tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2) | time_d, time_k |
| tn, tj | tkjn | tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6) | time_jn |
| — | ton<br>toff | ton = time_on * T – tskew1<br>toff = time_off * T – tskew1 | — |

### 4.3.5.3 UDMA In Timing

Figure 14 shows timing when the UDMA in transfer starts, Figure 15 shows timing when the UDMA in host terminates transfer, Figure 16 shows timing when the UDMA in device terminates transfer, and Table 25 lists the timing parameters for UDMA in burst.

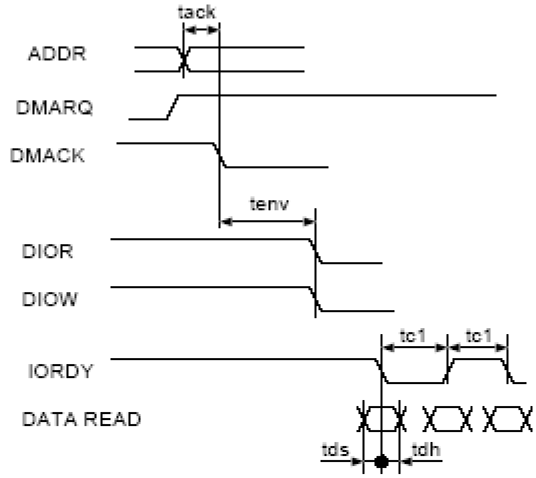



**Figure 14. UDMA In Transfer Starts Timing Diagram**

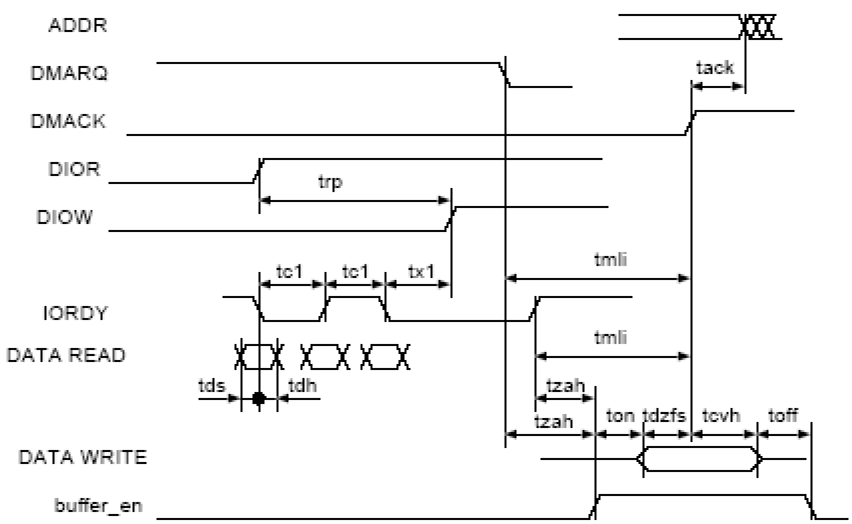



**Figure 15. UDMA In Host Terminates Transfer Timing Diagram**

## 4.3.5.4 UDMA Out Timing

Figure 17 shows timing when the UDMA out transfer starts, Figure 18 shows timing when the UDMA out host terminates transfer, Figure 19 shows timing when the UDMA out device terminates transfer, and Table 26 lists the timing parameters for UDMA out burst.

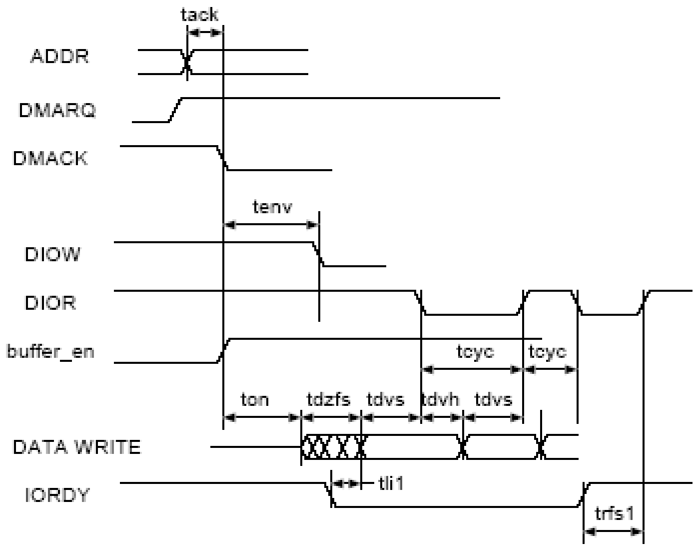



**Figure 17. UDMA Out Transfer Starts Timing Diagram**

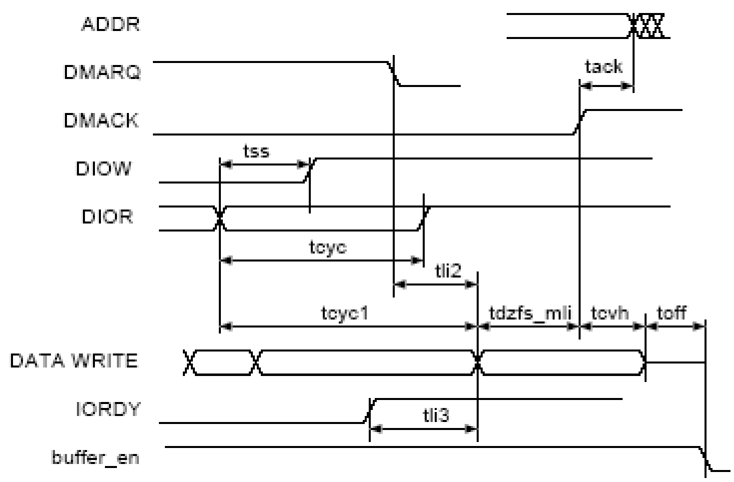



**Figure 18. UDMA Out Host Terminates Transfer Timing Diagram**

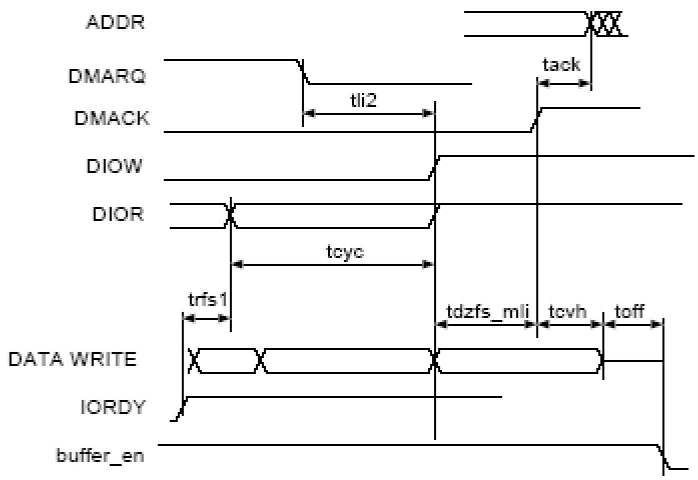



**Figure 19. UDMA Out Device Terminates Transfer Timing Diagram**

**Table 26. UDMA Out Burst Timing Parameters**

| ATA Parameter | Parameter from Figure 17, Figure 18, Figure 19 | Value | Controlling Variable |
|---|---|---|---|
| tack | tack | tack (min) = (time_ack * T) – (tskew1 + tskew2) | time_ack |
| tenv | tenv | tenv (min) = (time_env * T) – (tskew1 + tskew2)<br>tenv (max) = (time_env * T) + (tskew1 + tskew2) | time_env |
| tdvs | tdvs | tdvs = (time_dvs * T) – (tskew1 + tskew2) | time_dvs |
| tdvh | tdvh | tdvs = (time_dvh * T) – (tskew1 + tskew2) | time_dvh |
| tcyc | tcyc | tcyc = time_cyc * T – (tskew1 + tskew2) | time_cyc |
| t2cyc | — | t2cyc = time_cyc * 2 * T | time_cyc |
| trfs1 | trfs | trfs = 1.6 * T + tsui + tco + tbuf + tbuf | — |
| — | tdzfs | tdzfs = time_dzfs * T – (tskew1) | time_dzfs |
| tss | tss | tss = time_ss * T – (tskew1 + tskew2) | time_ss |
| tmli | tdzfs_mli | tdzfs_mli =max (time_dzfs, time_mli) * T – (tskew1 + tskew2) | — |
| tli | tli1 | tli1 > 0 | — |
| tli | tli2 | tli2 > 0 | — |
| tli | tli3 | tli3 > 0 | — |
| tcvh | tcvh | tcvh = (time_cvh *T) – (tskew1 + tskew2) | time_cvh |
| — | ton<br>toff | ton = time_on * T – tskew1<br>toff = time_off * T – tskew1 | — |

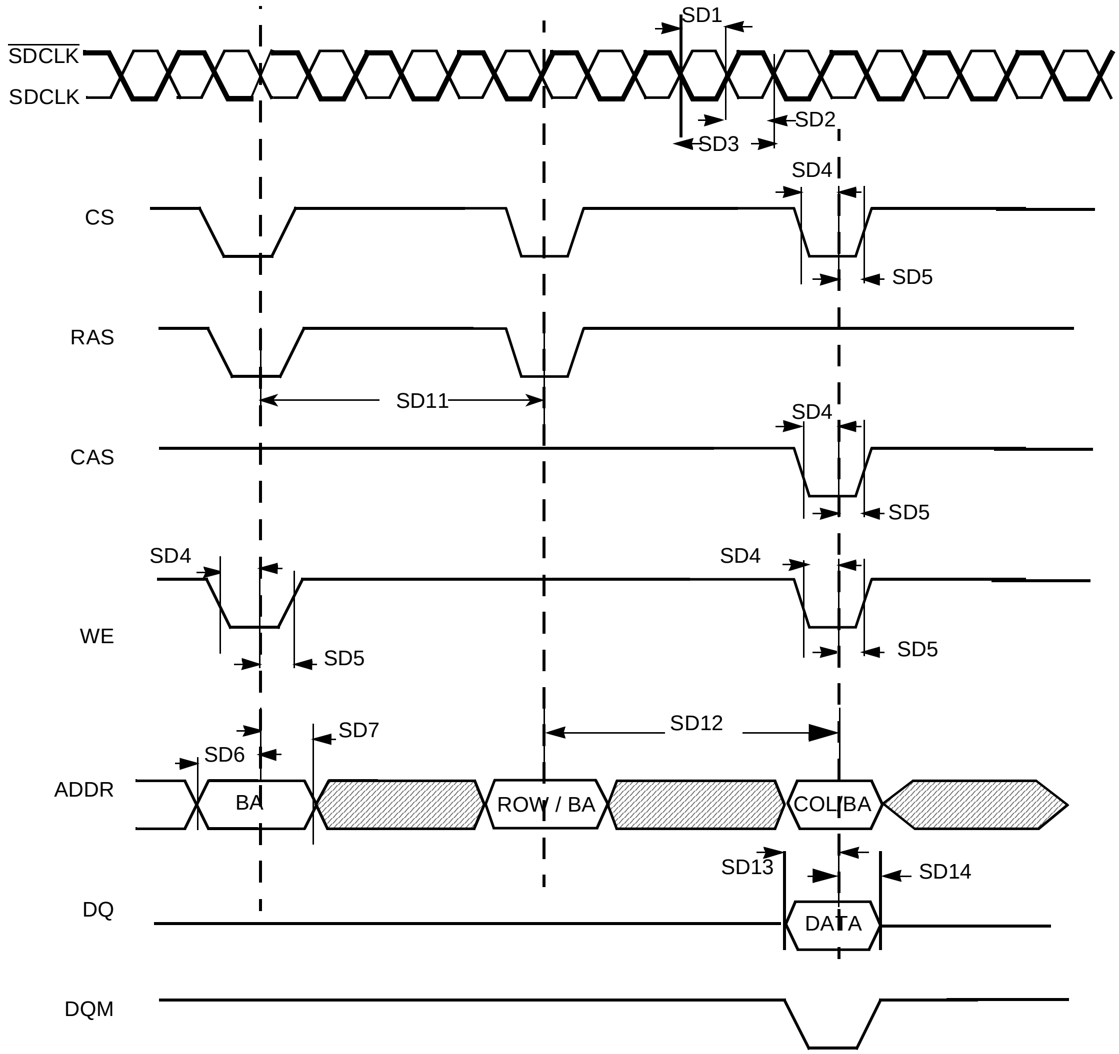



**Figure 34. SDR SDRAM Write Cycle Timing Diagram**

**Table 32. SDR SDRAM Write Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | tCMS | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | tCMH | 1.8 | — | ns |
| SD6 | Address setup time | tAS | 2.0 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD11 | Precharge cycle period[1] | tRP | 1 | 4 | clock |
| SD12 | Active to read/write command delay[1] | tRCD | 1 | 8 | clock |

**Table 32. SDR SDRAM Write Timing Parameters (continued)**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD13 | Data setup time | tDS | 2.0 | — | ns |
| SD14 | Data hold time | tDH | 1.3 | — | ns |

[1] SD11 and SD12 are determined by SDRAM controller register settings.

## NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

## NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 32 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

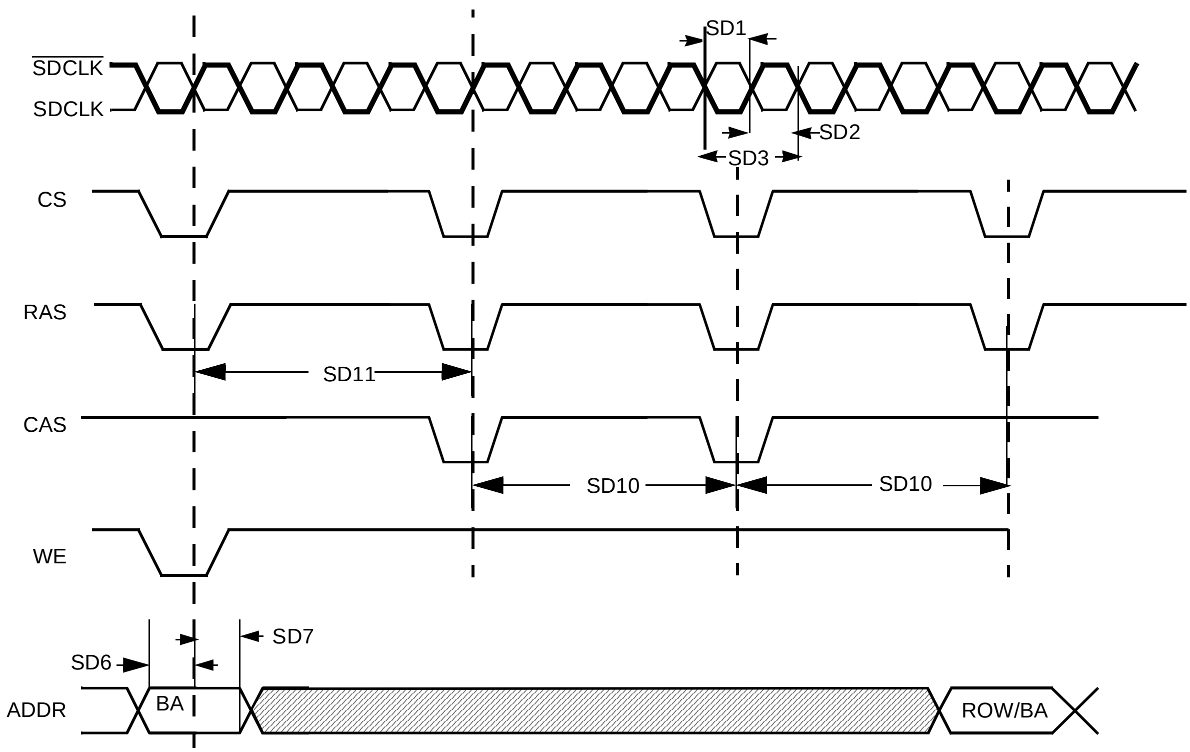



**Figure 35. SDRAM Refresh Timing Diagram**

**Table 37. ETM TRACECLK Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cyc}$ | Clock period | Frequency dependent | — | ns |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |

Figure 40 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 38 lists the timing parameters.

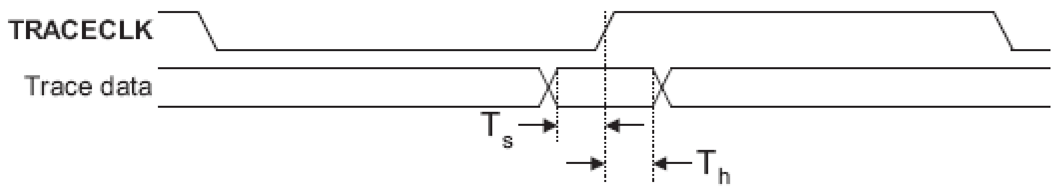



**Figure 40. Trace Data Timing Diagram**

**Table 38. ETM Trace Data Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_s$ | Data setup | 2 | — | ns |
| $T_h$ | Data hold | 1 | — | ns |

### 4.3.10.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 40.

## 4.3.11 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) that are defined by IrDA® (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and MIR protocols.

## 4.3.12 Fusebox Electrical Specifications

**Table 39. Fusebox Timing Characteristics**

| Ref. Num | Description | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| 1 | Program time for eFuse[1] | $t_{program}$ | 125 | — | — | µs |

[1] The program length is defined by the value defined in the epm_pgm_length[2:0] bits of the IIM module. The value to program is based on a 32 kHz clock source (4 * 1/32 kHz = 125 µs)

## 4.3.13 I2C Electrical Specifications

This section describes the electrical information of the I2C Module.

### 4.3.13.1 I2C Module Timing

Figure 41 depicts the timing of I2C module. Table 40 lists the I2C module timing parameters where the I/O supply is 2.7 V. 1

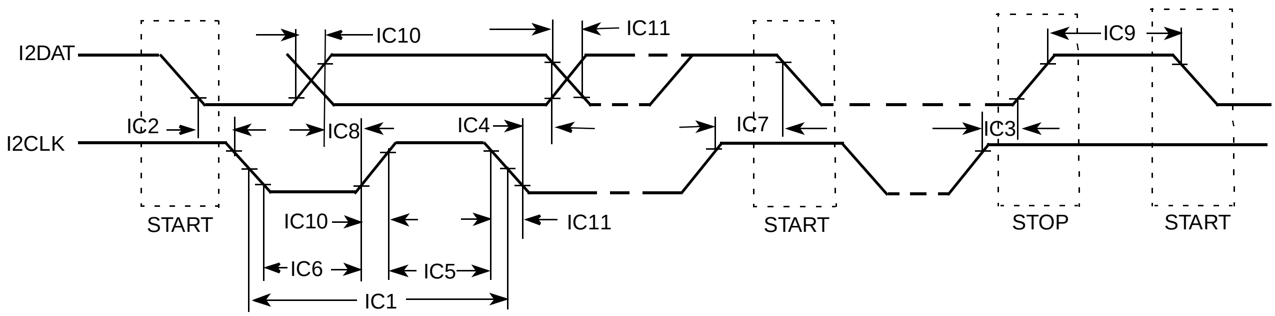



**Figure 41. I2C Bus Timing Diagram**

**Table 40. I2C Module Timing Parameters—I2C Pin I/O Supply=2.7 V**

| ID | Parameter | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| IC1 | I2CLK cycle time | 10 | — | 2.5 | — | µs |
| IC2 | Hold time (repeated) START condition | 4.0 | — | 0.6 | — | µs |
| IC3 | Set-up time for STOP condition | 4.0 | — | 0.6 | — | µs |
| IC4 | Data hold time | 0[1] | 3.45[2] | 0[1] | 0.9[2] | µs |
| IC5 | HIGH Period of I2CLK Clock | 4.0 | — | 0.6 | — | µs |
| IC6 | LOW Period of the I2CLK Clock | 4.7 | — | 1.3 | — | µs |
| IC7 | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | µs |
| IC8 | Data set-up time | 250 | — | 100[3] | — | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | µs |
| IC10 | Rise time of both I2DAT and I2CLK signals | — | 1000 | $20+0.1C_b$[4] | 300 | ns |
| IC11 | Fall time of both I2DAT and I2CLK signals | — | 300 | $20+0.1C_b$[4] | 300 | ns |
| IC12 | Capacitive load for each bus line ($C_b$) | — | 400 | — | 400 | pF |

[1] A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

[3] A Fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

[4] $C_b$ = total capacitance of one bus line in pF.

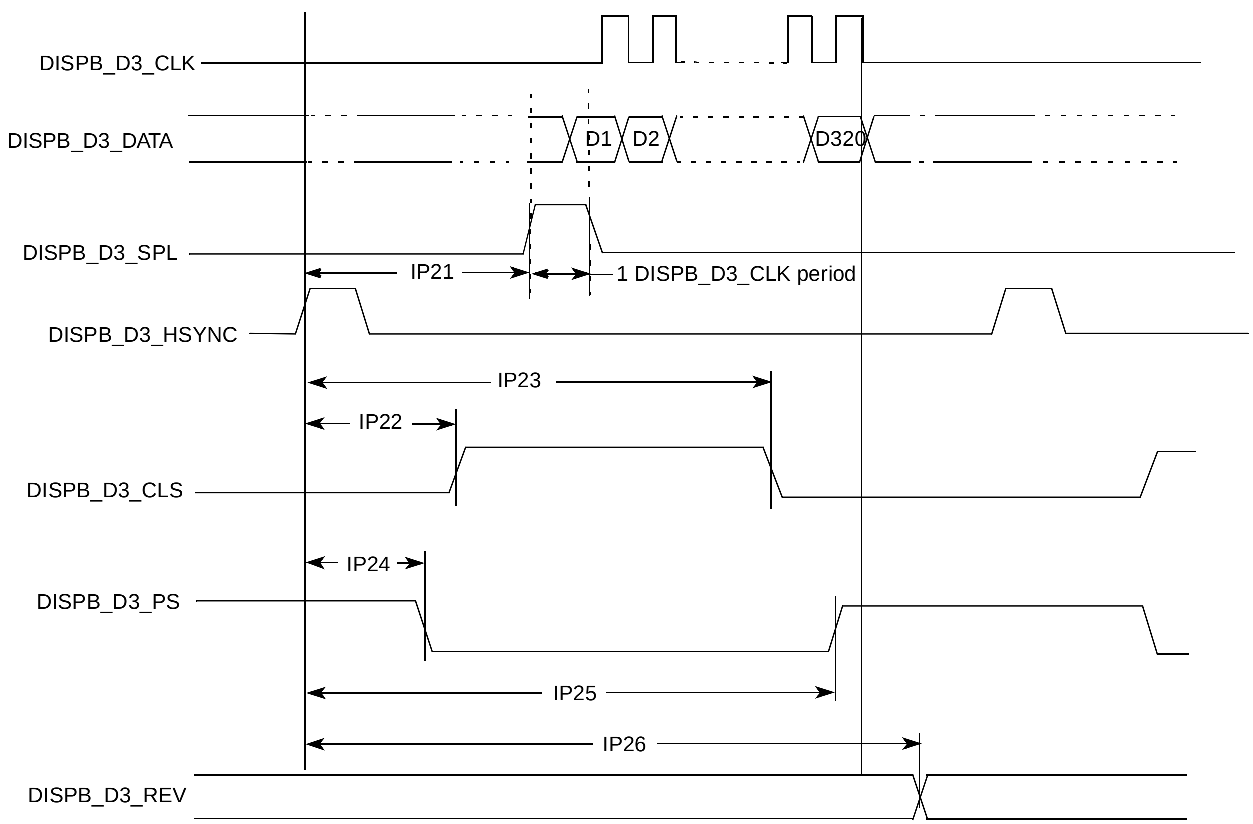
[3] Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

### 4.3.15.3 Interface to Sharp HR-TFT Panels

Figure 49 depicts the Sharp HR-TFT panel interface timing, and Table 46 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics," on page 55. The timing images correspond to straight polarity of the Sharp signals.




Example is drawn with FW+1=320 pixel/line, FH+1=240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

**Figure 49. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level**

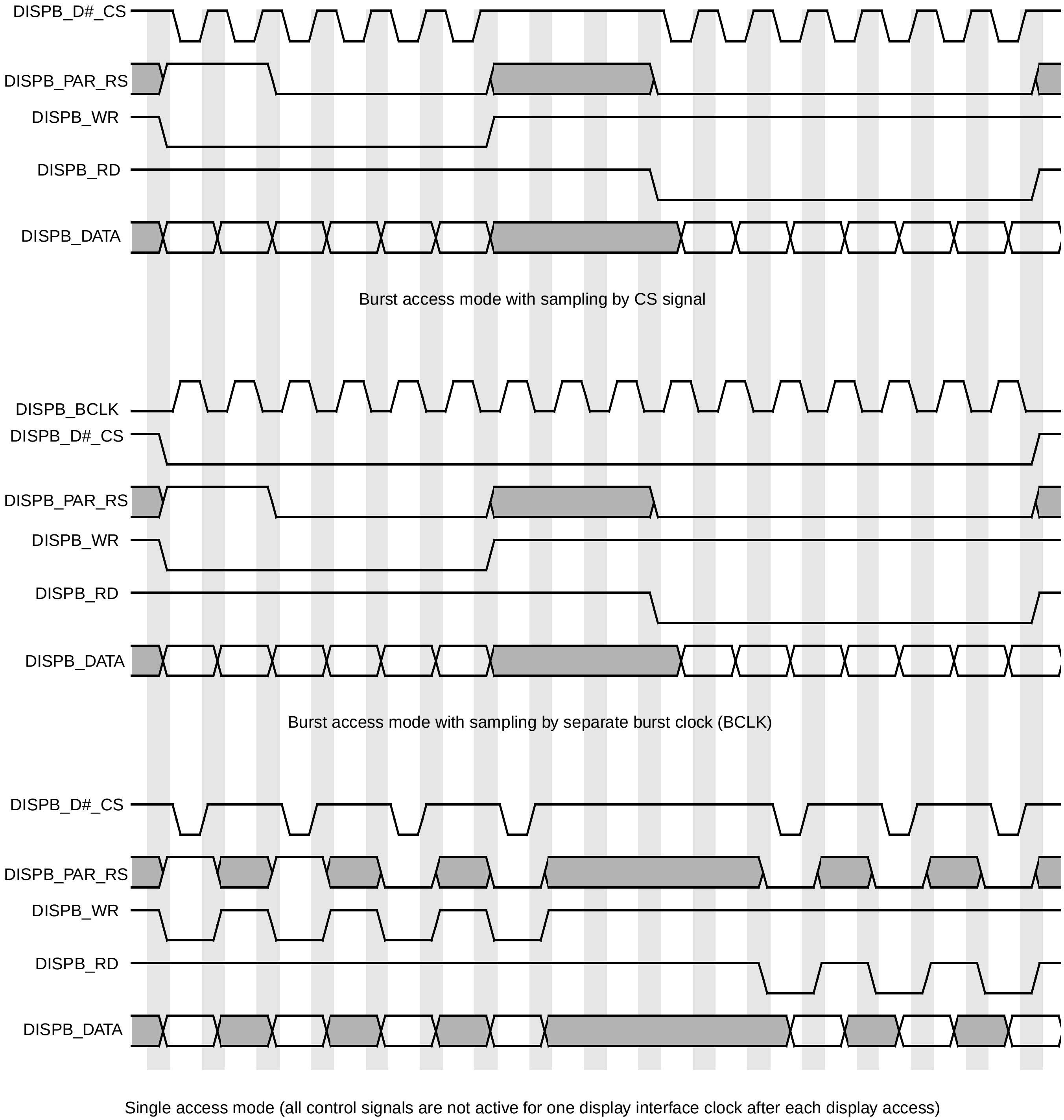



**Figure 51. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram**

**Table 47. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP36 | Controls hold time for write | Tdchw | Tdicpw–Tdicdw–1.5 | Tdicpw–Tdicdw | — | ns |
| IP37 | Slave device data delay[8] | Tracc | 0 | — | Tdrp[9]–Tlbd[10]–Tdicur–1.5 | ns |
| IP38 | Slave device data hold time[8] | Troh | Tdrp–Tlbd–Tdicdr+1.5 | — | Tdicpr–Tdicdr–1.5 | ns |
| IP39 | Write data setup time | Tds | Tdicdw–1.5 | Tdicdw | — | ns |
| IP40 | Write data hold time | Tdh | Tdicpw–Tdicdw–1.5 | Tdicpw–Tdicdw | — | ns |
| IP41 | Read period[2] | Tdicpr | Tdicpr–1.5 | Tdicpr | Tdicpr+1.5 | ns |
| IP42 | Write period[3] | Tdicpw | Tdicpw–1.5 | Tdicpw | Tdicpw+1.5 | ns |
| IP43 | Read down time[4] | Tdicdr | Tdicdr–1.5 | Tdicdr | Tdicdr+1.5 | ns |
| IP44 | Read up time[5] | Tdicur | Tdicur–1.5 | Tdicur | Tdicur+1.5 | ns |
| IP45 | Write down time[6] | Tdicdw | Tdicdw–1.5 | Tdicdw | Tdicdw+1.5 | ns |
| IP46 | Write up time[7] | Tdicuw | Tdicuw–1.5 | Tdicuw | Tdicuw+1.5 | ns |
| IP47 | Read time point[9] | Tdrp | Tdrp–1.5 | Tdrp | Tdrp+1.5 | ns |

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

#### 4.3.15.5.3 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 60 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP1_CONF and DI_SER_DISP2_CONF Registers.

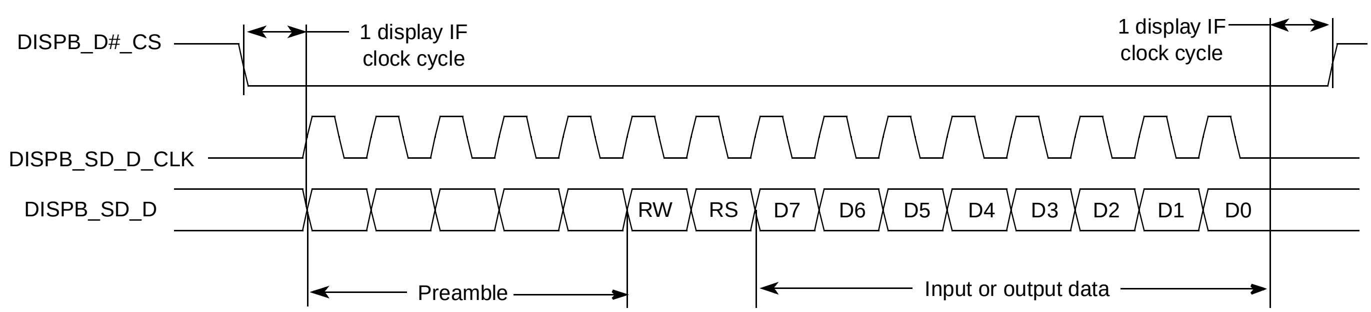



**Figure 60. 3-Wire Serial Interface Timing Diagram**

Figure 61 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

**Table 50. Parallel Interface Timing Parameters[1]**

| Signal | Parameter | Symbol | Standards | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| MSHC_SCLK | Cycle | tSCLKc | 25 | — | ns |
| | H pulse length | tSCLKwh | 5 | — | ns |
| | L pulse length | tSCLKwl | 5 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |
| MSHC_BS | Setup time | tBSsu | 8 | — | ns |
| | Hold time | tBSh | 1 | — | ns |
| MSHC_DATA | Setup time | tDsu | 8 | — | ns |
| | Hold time | tDh | 1 | — | ns |
| | Output delay time | tDd | — | 15 | ns |

[1] Timing is guaranteed for NVCC from 2.7 through 3.1 V. See NVCC restrictions described in Table 7, "Operating Ranges," on page 12.

### 4.3.17 Personal Computer Memory Card International Association (PCMCIA)

Figure 68 and Figure 69 depict the timings pertaining to the PCMCIA module, each of which is an example of one clock of strobe set-up time and one clock of strobe hold time. Table 51 lists the timing parameters.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the aim card will be used by the SIM card to recover the clock from the data much like a standard UART. All six (or 5 in case bi directional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other.

There are no required timing relationships between the signals in normal mode, but there are some in two specific cases: reset and power down sequences.

### 4.3.20.1 General Timing Requirements

Figure 72 shows the timing of the SIM module, and Figure 54 lists the timing parameters.

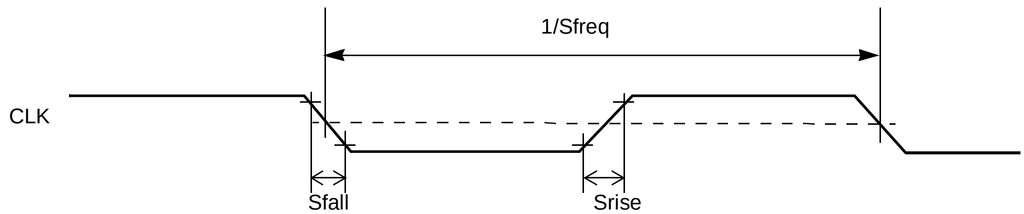



**Figure 72. SIM Clock Timing Diagram**

**Table 54. SIM Timing Specification—High Drive Strength**

| Num | Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | SIM Clock Frequency (CLK)[1] | $S_{freq}$ | 0.01 | 5 (Some new cards may reach 10) | MHz |
| 2 | SIM CLK Rise Time [2] | $S_{rise}$ | — | 20 | ns |
| 3 | SIM CLK Fall Time [3] | $S_{fall}$ | — | 20 | ns |
| 4 | SIM Input Transition Time (RX, SIMPD) | $S_{trans}$ | — | 25 | ns |

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

### 4.3.20.2 Reset Sequence

#### 4.3.20.2.1 Cards with Internal Reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 73):

- After powerup, the clock signal is enabled on SGCLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

**Table 63. 19 x 19 BGA No Connects[1]**

| Signal | Ball Location |
|---|---|
| NC | N7 |
| NC | P7 |
| NC | U21 |

[1] These contacts are not used and must be floated by the user.

### 5.1.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

**Table 64. 19 x 19 BGA Signal ID by Ball Grid Location**

| Signal ID | Ball Location | Signal ID | Ball Location |
|---|---|---|---|
| A0 | Y6 | CKIL | E21 |
| A1 | AC5 | CLKO | C20 |
| A10 | V15 | CLKSS | H17 |
| A11 | AB3 | COMPARE | A20 |
| A12 | AA3 | CONTRAST | N21 |
| A13 | Y3 | CS0 | U17 |
| A14 | Y15 | CS1 | Y22 |
| A15 | Y14 | CS2 | Y18 |
| A16 | V14 | CS3 | Y19 |
| A17 | Y13 | CS4 | Y20 |
| A18 | V13 | CS5 | AA21 |
| A19 | Y12 | CSI_D10 | K21 |
| A2 | AB5 | CSI_D11 | K22 |
| A20 | V12 | CSI_D12 | K23 |
| A21 | Y11 | CSI_D13 | L20 |
| A22 | V11 | CSI_D14 | L18 |
| A23 | Y10 | CSI_D15 | L21 |
| A24 | Y9 | CSI_D4 | J20 |
| A25 | Y8 | CSI_D5 | J21 |
| A3 | AA5 | CSI_D6 | L17 |
| A4 | Y5 | CSI_D7 | J22 |
| A5 | AC4 | CSI_D8 | J23 |
| A6 | AB4 | CSI_D9 | K20 |
| A7 | AA4 | CSI_HSYNC | H22 |
| A8 | Y4 | CSI_MCLK | H20 |
| A9 | AC3 | CSI_PIXCLK | H23 |
| ATA_CS0 | E1 | CSI_VSYNC | H21 |
| ATA_CS1 | G4 | CSPI1_MISO | N2 |
| ATA_DIOR | E3 | CSPI1_MOSI | N1 |
| ATA_DIOW | H6 | CSPI1_SCLK | M4 |
| ATA_DMACK | E2 | CSPI1_SPI_RDY | M1 |
| $\overline{\text{ATA\_RESET}}$ | F3 | CSPI1_SS0 | M2 |
| BATT_LINE | F6 | CSPI1_SS1 | N6 |
| BCLK | W20 | CSPI1_SS2 | M3 |
| BOOT_MODE0 | F17 | CSPI2_MISO | B4 |
| BOOT_MODE1 | C21 | CSPI2_MOSI | D5 |

**Table 64. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| EB1 | W21 |
| ECB | Y21 |
| FPSHIFT | M23 |
| GPIO1_0 | C19 |
| GPIO1_1 | G17 |
| GPIO1_2 | B20 |
| LD7 | T20 |
| LD8 | R17 |
| LD9 | U23 |
| M_GRANT | U18 |
| M_REQUEST | T17 |
| MA10 | Y2 |
| MCUPG | See VPG0 |
| NFALE | T2 |
| NFCE | R4 |
| NFCLE | T1 |
| NFRB | R3 |
| NFRE | T4 |
| NFWE | T3 |
| NFWP | P6 |
| OE | T18 |
| PAR_RS | P22 |
| PC_BVD1 | G2 |
| PC_BVD2 | H4 |
| PC_CD1 | J3 |
| PC_CD2 | H1 |
| PC_POE | J6 |
| PC_PWRON | K6 |
| PC_READY | H2 |
| PC_RST | F1 |
| PC_RW | G3 |
| PC_VS1 | H3 |
| PC_VS2 | G1 |
| PC_WAIT | J4 |
| POR | F21 |
| POWER_FAIL | F20 |
| PWMO | F2 |
| RAS | AA19 |
| READ | N18 |
| RESET_IN | F22 |
| RI_DCE1 | D10 |
| RI_DTE1 | B11 |
| RTCK | D15 |
| RTS1 | B9 |
| RTS2 | B12 |
| RW | V18 |

| Signal ID | Ball Location |
|---|---|
| LD17 | W23 |
| LD2 | R21 |
| LD3 | R20 |
| LD4 | T23 |
| LD5 | T22 |
| LD6 | T21 |
| SCK6 | R2 |
| SCLK0 | B19 |
| SD_D_CLK | M21 |
| SD_D_I | M20 |
| SD_D_IO | M18 |
| SD0 | AC18 |
| SD1 | AA17 |
| SD1_CLK | K2 |
| SD1_CMD | K3 |
| SD1_DATA0 | K4 |
| SD1_DATA1 | J1 |
| SD1_DATA2 | J2 |
| SD1_DATA3 | L6 |
| SD10 | AB14 |
| SD11 | AC14 |
| SD12 | AA13 |
| SD13 | AB13 |
| SD14 | AC13 |
| SD15 | AA12 |
| SD16 | AC12 |
| SD17 | AA11 |
| SD18 | AB11 |
| SD19 | AC11 |
| SD2 | AB17 |
| SD20 | AA10 |
| SD21 | AB10 |
| SD22 | AC10 |
| SD23 | AC9 |
| SD24 | AA9 |
| SD25 | AC8 |
| SD26 | AB8 |
| SD27 | AC7 |
| SD28 | AA8 |
| SD29 | AB7 |
| SD3 | AC17 |
| SD30 | AA7 |
| SD31 | AC6 |
| SD4 | AA16 |
| SD5 | AC16 |
| SD6 | AA15 |

- *MCIMX31 Chip Errata* (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

# 7 Revision History

Table 65 summarizes revisions to the *MCIMX31C/MCIMX31LC Data Sheet* since the release of Rev. 3.

**Table 65. Revision History of the MCIMX31C/MCIMX31LC Data Sheet**

| Rev | Location | Change |
|---|---|---|
| 4 | Table 7, "Operating Ranges," on page 12 | Operating Junction Temperature Range Max: changed from 100 to 105. |
| 4.1 | Table 1, "MCIMX31C and MCIMX31LC Ordering Information," on page 3 | Added new part numbers MCIMX31CVMN4D and MCIMX31LCVMN4D. |
| 4.1 | Section 1.2.1, "Feature Differences Between TO2.0 and TO 2.0.1 | Added new section describing differences between silicon revisions. |
| 4.2 | Table 1, "MCIMX31C and MCIMX31LC Ordering Information," on page 3 | Added new part numbers MCIMX31CJMN4C and MCIMX31LCJMN4D and a footnote. |
| 4.3 | Table 1, "MCIMX31C and MCIMX31LC Ordering Information," on page 3 | Added new part number MCIMX31CJMN4D. |