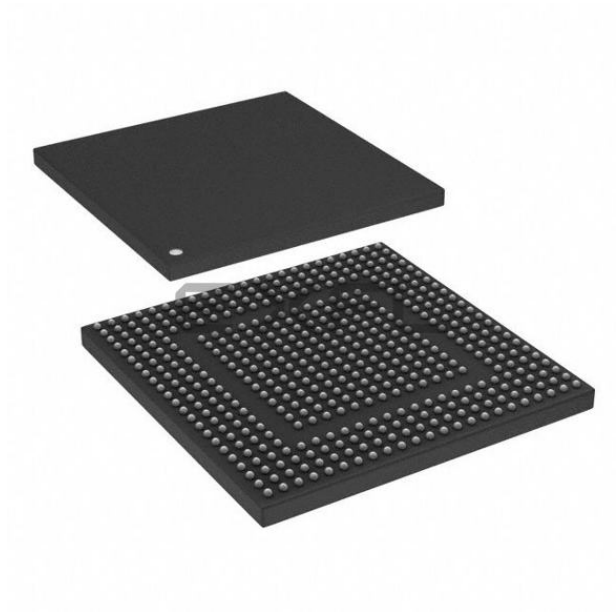

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31lcvmn4cr2

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31C.

Table 1. MCIMX31C and MCIMX31LC Ordering Information[1]

Part Number	Silicon Revision	Operating Temperature Range (°C)	Package[2]
MCIMX31CVMN4C!	2.0	–40 to 85	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LCVMN4C!	2.0	–40 to 85	
MCIMX31CVMN4D!	2.0.1	–40 to 85	
MCIMX31LCVMN4D!	2.0.1	–40 to 85	
MCIMX31CJMN4C	2.0.1	–40 to 85	
MCIMX31LCJMN4D	2.0.1	–40 to 85	
MCIMX31CJMN4D	2.0.1	–40 to 85	

1 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

2 Case 1931 is RoHS compliant, lead-free, MSL = 3.

1.2.1 Feature Differences Between TO2.0 and TO 2.0.1

The following is a summary of the differences between silicon Revision 2.0 and Revision 2.0.1:

- Revision 2.0.1 - iROM updated to support boot from USB HS and SD/MMC.

Table 4. MCIMX31C Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, “Absolute Maximum Ratings”	on page 10
Table 6, “Thermal Resistance Data—19 × 19 mm Package”	on page 10
Table 7, “Operating Ranges”	on page 12
Table 8, “Specific Operating Ranges for Silicon Revision 2.0 and 2.0.1”	on page 12
Table 9, “Interface Frequency”	on page 13
Section 4.1.1, “Supply Current Specifications”	on page 14
Section 4.2, “Supply Power-Up/Power-Down Requirements and Restrictions”	on page 15

CAUTION

Stresses beyond those listed under Table 5, "Absolute Maximum Ratings," on page 10 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 7, "Operating Ranges," on page 12 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	–0.5	1.47	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.1	V
Input Voltage Range	V_{Imax}	–0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	–40	125	^{o}C
ESD Damage Immunity:				
Human Body Model (HBM)	V_{esd}	—	H1C[1]	V
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	C2[2]	
Offset voltage allowed in run mode between core supplies.	V_{core_offset}[3]	—	15	mV

1 HBM ESD classification level according to the AEC-Q100-002-Rev-D standard.

2 Integrated circuit CDM ESD classification level according to the AEC-Q100-011-Rev-B standard.

3 The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 6 provides the thermal resistance data for the 19 × 19 mm, 0.8 mm pitch package.

Table 6. Thermal Resistance Data—19 × 19 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	46	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	29	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	38	°C/W	1, 2, 3

Table 6. Thermal Resistance Data—19 × 19 mm Package (continued)

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	25	°C/W	1, 2, 3
Junction to Board	—	$R_{\theta JB}$	19	°C/W	1, 3
Junction to Case (Top)	—	$R_{\theta JCtop}$	10	°C/W	1, 4
Junction to Package Top (natural convection)	—	Ψ_{JT}	2	°C/W	1, 5

NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 7 provides the operating ranges.

NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

Table 7. Operating Ranges

Symbol	Parameter	Min	Max	Units
QVCC, QVCC1, QVCC4	Core Operating Voltage[1,2] $0 \le f_{ARM} \le 400$ MHz	1.22	1.47	V
	State Retention Voltage[3]	0.95	—	
NVCC1, NVCC3–10	I/O Supply Voltage, except DDR[4]	1.75	3.1	V
NVCC2, NVCC21, NVCC22	I/O Supply Voltage, DDR only	1.75	1.95	V
FVCC, MVCC, SVCC, UVCC	PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[5]	1.3	1.47	V
IOQVDD	On-device Level Shifter Supply Voltage	1.6	1.9	V
FUSE_VDD	Fusebox read Supply Voltage[6]	—	—	V
	Fusebox write (program) Supply Voltage[7]	3.0	3.3	V
T_A	Operating Ambient Temperature Range	–40	85	°C
T_j	Operating Junction Temperature Range	—	105	°C

1 Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

2 The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID

3 The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode.

4 Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

5 PLL voltage must not be altered after power-up, otherwise the PLL will be unstable and lose lock. To minimize inducing noise on the PLL supply line, source the voltage from a low-noise, dedicated supply. PLL parameters in Table 28, "DPLL Specifications," on page 31, are guaranteed over the entire specified voltage range.

6 In read mode, FUSE_VDD can be floated or grounded.

7 Fuses might be inadvertently blown if written to while the voltage is below this minimum.

Table 8. Specific Operating Ranges for Silicon Revision 2.0 and 2.0.1

Symbol	Parameter	Min	Max	Units
FUSE_VDD	Fusebox read Supply Voltage[1]	—	—	V
	Fusebox write (program) Supply Voltage[2]	3.0	3.3	V

1 In read mode, FUSE_VDD should be floated or grounded.

2 Fuses might be inadvertently blown if written to while the voltage is below the minimum.

Table 9 provides information for interface frequency limits. For more details about clocks characteristics, see Section 4.3.8, “DPLL Electrical Specifications” on page 31 and Section 4.3.3, “Clock Amplifier Module (CAMP) Electrical Characteristics” on page 19.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min	Typ	Max	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz
2	CKIL Frequency[1]	f_{CKIL}	32	32.768	38.4	kHz
3	CKIH Frequency[2]	f_{CKIH}	15	26	75	MHz

1 CKIL must be driven by an external clock source to ensure proper start-up and operation of the device. CKIL is needed to clock the internal reset synchronizer, the watchdog, and the real-time clock.

2 DPTC functionality, specifically the voltage/frequency relation table, is dependent on CKIH frequency. At the time of publication, standard tables used by Freescale OSs provided for a CKIH frequency of 26 MHz only. Any deviation from this frequency requires an update to the OS. For more details, refer to the particular OS user's guide documentation. DPTC/DVFS are not supported for fARM ≤ 400MHz.

Table 10 shows the fusebox supply current parameters.

Table 10. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current.[1] Current to program one eFuse bit: efuse_pgm = 3.0V	$I_{program}$	—	35	60	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

4.1.1 Supply Current Specifications

Table 11 shows the core current consumption for –40°C to 85°C for Silicon Revision 2.0 and 2.0.1 for the MCIMX31C.

Table 11. Current Consumption for –40°C to 85°C[1, 2] for Silicon Revision 2.0 and 2.0.1

Mode	Conditions	QVCC (Peripheral)		QVCC1 (ARM)		QVCC4 (L2)		FVCC + MVCC + SVCC + UVCC (PLL)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Deep Sleep	• QVCC = 0.95 V • ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.20	9.00	—	—	—	—	0.04	0.14	mA
State Retention	• QVCC and QVCC1 = 0.95 V • L2 caches are power gated (QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.20	9.00	0.15	3.50	—	—	0.04	0.14	mA
Wait	• QVCC,QVCC1, and QVCC4 = 1.22 V • ARM is in wait for interrupt mode • MAX is active • L2 cache is stopped but powered • MCU PLL is on (400 MHz), VCC = 1.4 V • USB PLL and SPLL are off, VCC = 1.4 V • FPM is on • CKIH input is on • CAMP is on • 32 kHz input is on • All clocks are gated off • All modules are off (by programming CGR[2:0] registers) • RNGA oscillator is off • No external resistive loads	7.00	19.00	3.00	100.00	0.03	0.90	4.00	6.00	mA

1 Typical column: TA = 25°C

2 Maximum column: TA = 85°C

Table 17. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1] – 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

4.3.4 1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 18 lists the RPP timing parameters.

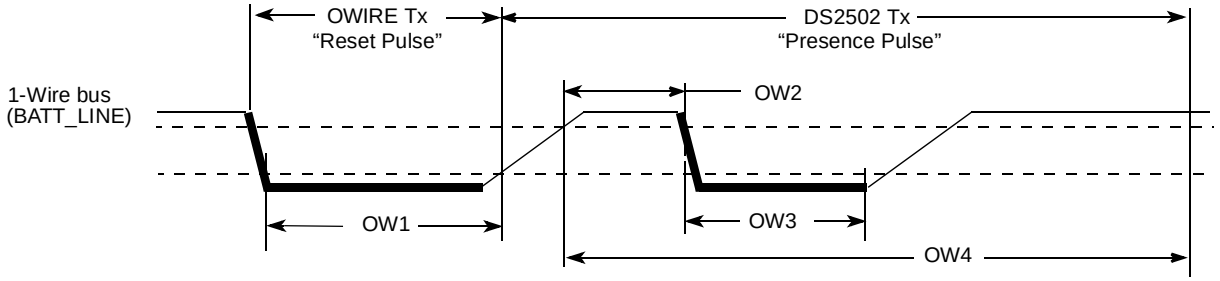

Figure 6. Reset and Presence Pulses (RPP) Timing Diagram

Table 18. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 7 depicts Write 0 Sequence timing, and Table 19 lists the timing parameters.

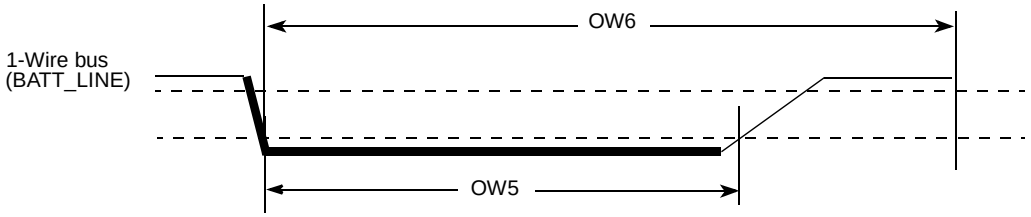

Figure 7. Write 0 Sequence Timing Diagram

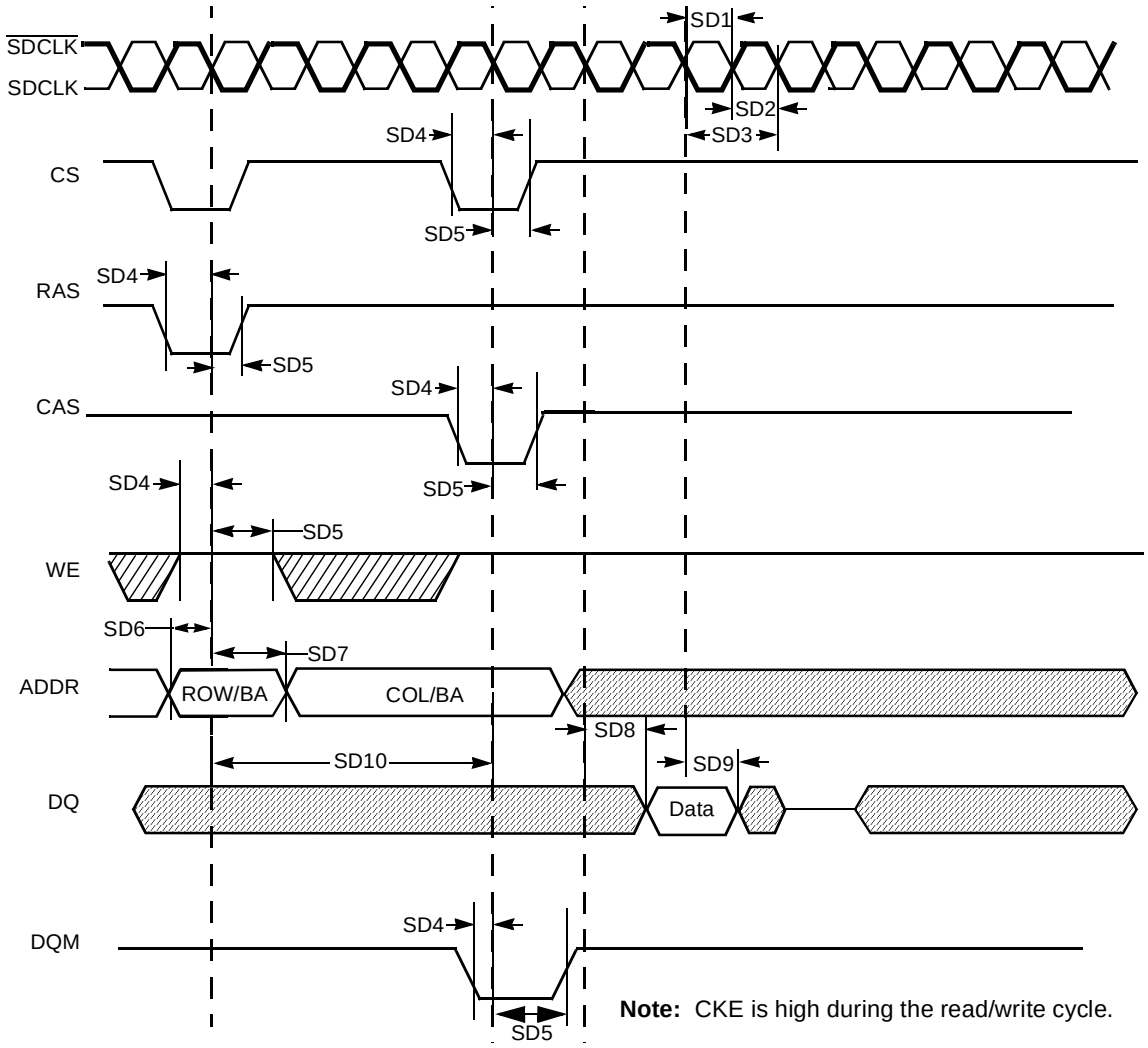

Figure 33. SDRAM Read Cycle Timing Diagram

Table 31. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

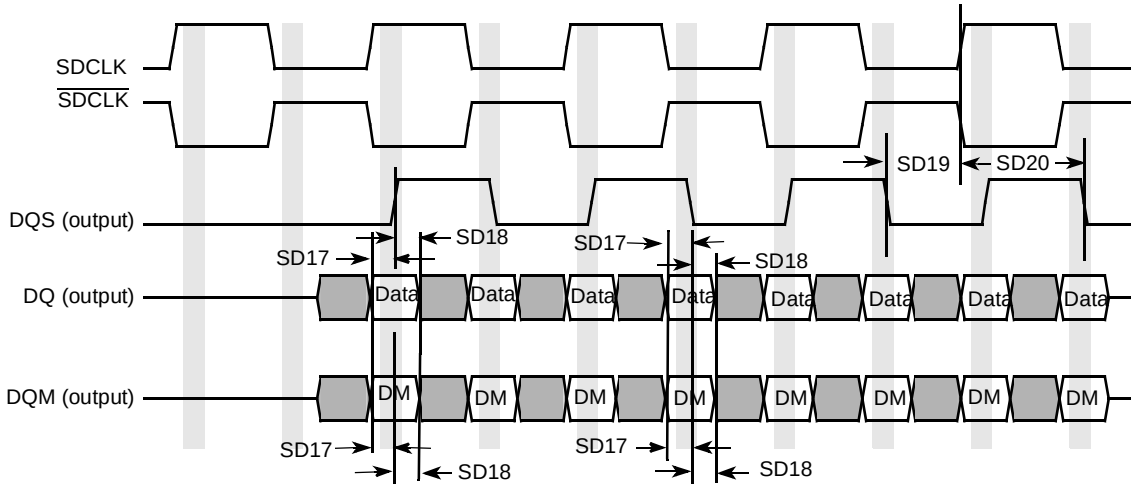

Figure 37. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 35. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min	Max	Unit
SD17	DQ & DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ & DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

1 Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

The timing described in Figure 43 is that of a Motorola sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.3.14.3 Electrical Characteristics

Figure 44 depicts the sensor interface timing, and Table 42 lists the timing parameters.

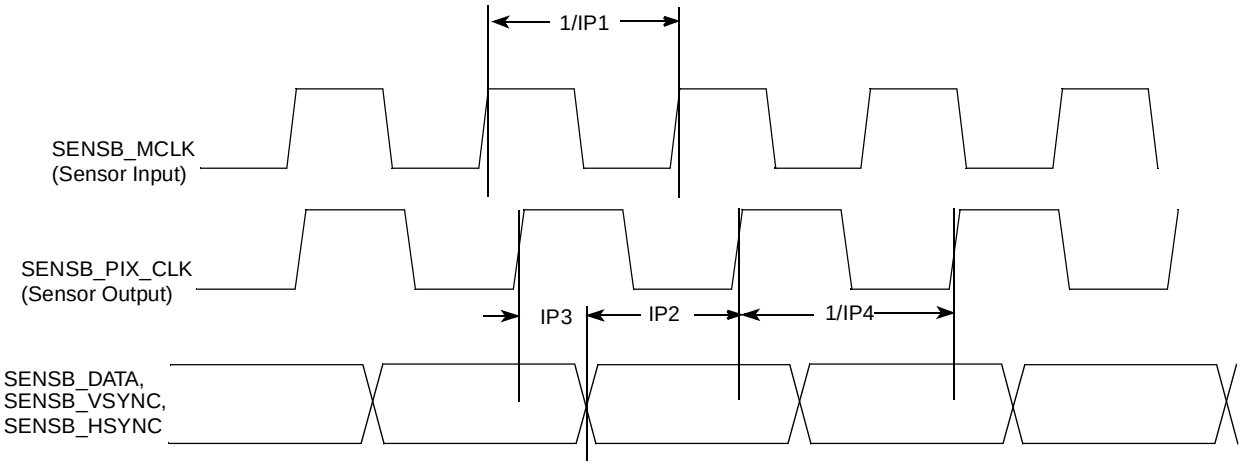

Figure 44. Sensor Interface Timing Diagram

Table 42. Sensor Interface Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

1 The timing specifications for Figure 43 are referenced to the rising edge of SENS_PIX_CLK when the SENS_PIX_CLK_POL bit in the CSI_SENS_CONF register is cleared. When the SENS_PIX_CLK_POL is set, the clock is inverted and all timing specifications will remain the same but are referenced to the falling edge of the clock.

4.3.15 IPU—Display Interfaces

4.3.15.1 Supported Display Components

Table 43 lists the known supported display components at the time of publication.

Table 43. Supported Display Components[1]

Type	Vendor	Model
TFT displays (memory-less)	Sharp (HR-TFT Super Mobile LCD family)	LQ035Q7 DB02, LM019LC1Sxx
	Samsung (QCIF and QVGA TFT modules for mobile phones)	LTS180S1-HF1, LTS180S3-HF1, LTS350Q1-PE1, LTS350Q1-PD1, LTS220Q1-HE1[2]
	Toshiba (LTM series)	LTM022P806[2], LTM04C380K[2], LTM018A02A[2], LTM020P332[2], LTM021P337[2], LTM019P334[2], LTM022A783[2], LTM022A05ZZ[2]
	NEC	NL6448BC20-08E, NL8060BC31-27
Display controllers	Epson	S1D15xxx series, S1D19xxx series, S1D13713, S1D13715
	Solomon Systech	SSD1301 (OLED), SSD1828 (LDCD)
	Hitachi	HD66766, HD66772
	ATI	W2300
Smart display modules	Epson	L1F10043 T[2], L1F10044 T[2], L1F10045 T[2], L2D22002[2], L2D20014[2], L2F50032[2], L2D25001 T[2]
	Hitachi	120 160 65K/4096 C-STN (#3284 LTD-1398-2) based on HD 66766 controller
	Densitron Europe LTD	All displays with MPU 80/68K series interface and serial peripheral interface
	Sharp	LM019LC1Sxx
	Sony	ACX506AKM
Digital video encoders (for TV)	Analog Devices	ADV7174/7179
	Crystal (Cirrus Logic)	CS49xx series
	Focus	FS453/4

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only display component suppliers.

2 These display components not validated at time of publication.

4.3.15.2 Synchronous Interfaces

4.3.15.2.1 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 45 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

Table 47. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP36	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP37	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]–Tdicur–1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp–Tlbd–Tdicdr+1.5	—	Tdicpr–Tdicdr–1.5	ns
IP39	Write data setup time	Tds	Tdicdw–1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP41	Read period[2]	Tdicpr	Tdicpr–1.5	Tdicpr	Tdicpr+1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw–1.5	Tdicpw	Tdicpw+1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr–1.5	Tdicdr	Tdicdr+1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur–1.5	Tdicur	Tdicur+1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw–1.5	Tdicdw	Tdicdw+1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw–1.5	Tdicuw	Tdicuw+1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.3.15.5.3 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 60 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP1_CONF and DI_SER_DISP2_CONF Registers.

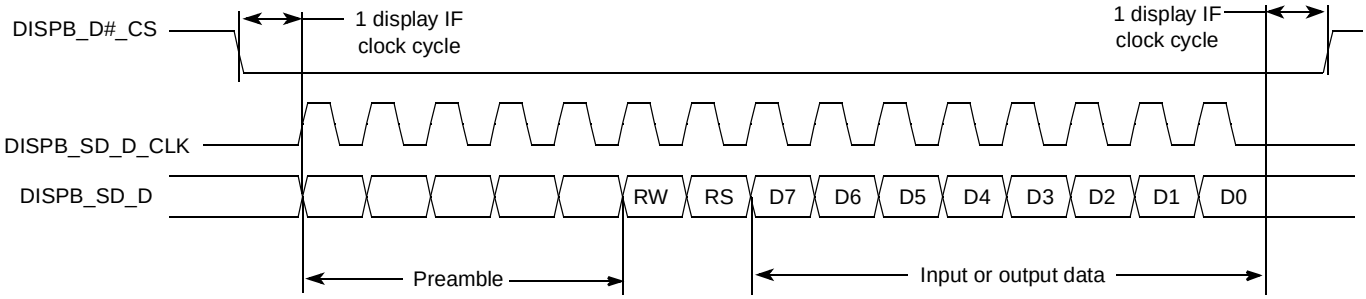

Figure 60. 3-Wire Serial Interface Timing Diagram

Figure 61 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

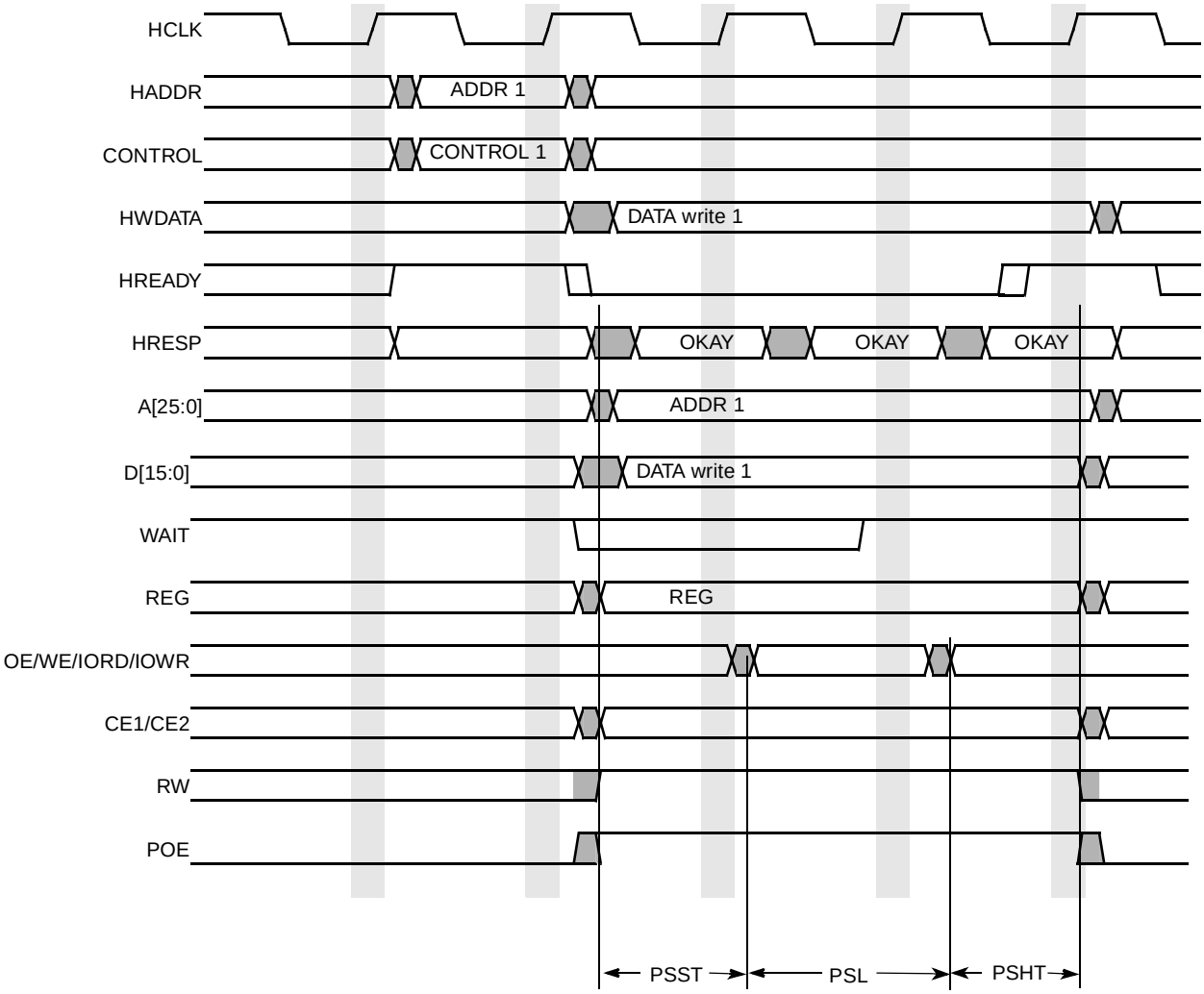

Figure 68. Write Accesses Timing Diagram—PSHT=1, PSST=1

4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 75 and Table 55 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

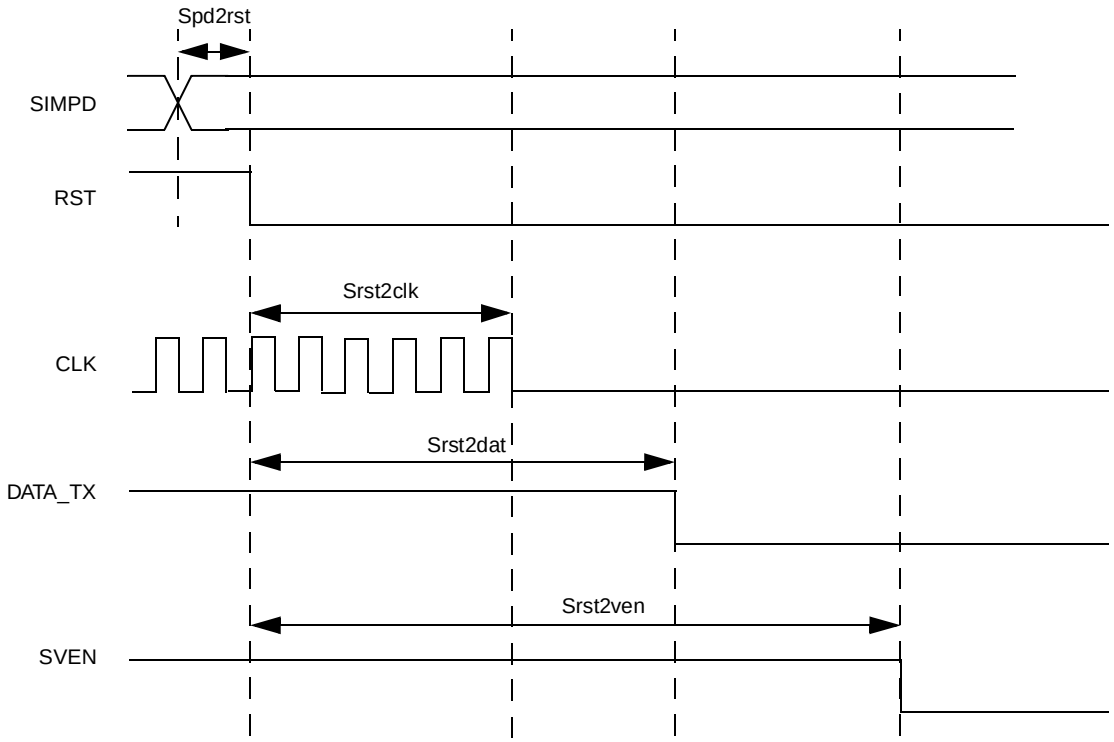

Figure 75. SmartCard Interface Power Down AC Timing

Table 55. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9*1/FCKIL	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8*1/FCKIL	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7*1/FCKIL	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9*1/FCKIL	25	ns