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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31lcvmn4d

4.1.1 Supply Current Specifications

Table 11 shows the core current consumption for –40°C to 85°C for Silicon Revision 2.0 and 2.0.1 for the MCIMX31C.

Table 11. Current Consumption for –40°C to 85°C[1, 2] for Silicon Revision 2.0 and 2.0.1

Mode	Conditions	QVCC (Peripheral)		QVCC1 (ARM)		QVCC4 (L2)		FVCC + MVCC + SVCC + UVCC (PLL)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Deep Sleep	• QVCC = 0.95 V • ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.20	9.00	—	—	—	—	0.04	0.14	mA
State Retention	• QVCC and QVCC1 = 0.95 V • L2 caches are power gated (QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.20	9.00	0.15	3.50	—	—	0.04	0.14	mA
Wait	• QVCC,QVCC1, and QVCC4 = 1.22 V • ARM is in wait for interrupt mode • MAX is active • L2 cache is stopped but powered • MCU PLL is on (400 MHz), VCC = 1.4 V • USB PLL and SPLL are off, VCC = 1.4 V • FPM is on • CKIH input is on • CAMP is on • 32 kHz input is on • All clocks are gated off • All modules are off (by programming CGR[2:0] registers) • RNGA oscillator is off • No external resistive loads	7.00	19.00	3.00	100.00	0.03	0.90	4.00	6.00	mA

1 Typical column: TA = 25°C

2 Maximum column: TA = 85°C

NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual. NVCC for Table 12 refers to NVCC1 and NVCC3–10; QVCC refers to QVCC, QVCC1, and QVCC4.

Table 12. GPIO DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = –1 mA	NVCC –0.15	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.15	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current, slow slew rate	I_{OH_S}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive	 –2 –4 –8	—	—	mA
High-level output current, fast slew rate	I_{OH_F}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive	 –4 –6 –8	—	—	mA
Low-level output current, slow slew rate	I_{OL_S}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 2 4 8	—	—	mA
Low-level output current, fast slew rate	I_{OL_F}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 4 6 8	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	—	NVCC	V
Low-Level DC input voltage	V_{IL}	—	0	—	0.3*QVCC	V
Input Hysteresis	V_{HYS}	Hysteresis enabled	0.25	—	—	V
Schmitt trigger VT+	V_T +	Hysteresis enabled	0.5*QVCC	—	—	V
Schmitt trigger VT–	V_T –	Hysteresis enabled	—	—	0.5*QVCC	V
Pull-up resistor (100 kΩ PU)	R_{PU}[1]	—	—	100	—	kΩ
Pull-down resistor (100 kΩ PD)	R_{PD}[1]	—	—	100	—	
Input current (no PU/PD)	I_{IN}	V_I = NVCC or GND	—	—	±1	µA
Input current (100 kΩ PU)	I_{IN}	V_I = 0	—	—	25	µA µA
Input current (100 kΩ PD)	I_{IN}	V_I = NVCC	—	—	28	µA
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

1 Not a precise value. Measurements made on small sample size have shown variations of ±50% or more.

Table 17. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1] – 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

4.3.4 1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 18 lists the RPP timing parameters.

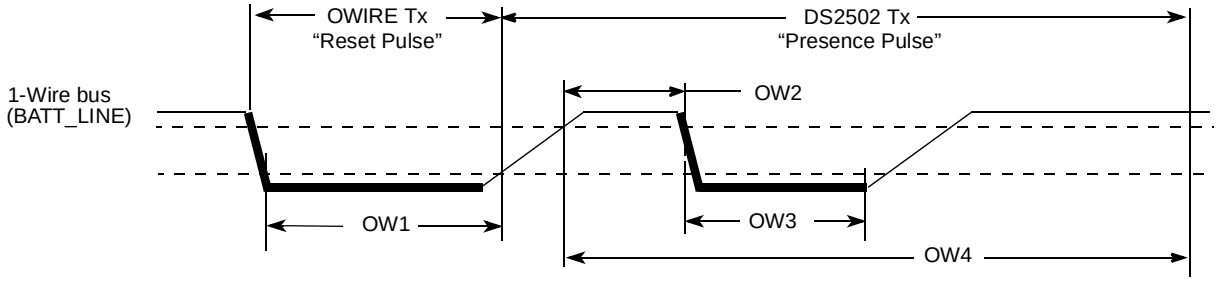


Figure 6. Reset and Presence Pulses (RPP) Timing Diagram

Table 18. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 7 depicts Write 0 Sequence timing, and Table 19 lists the timing parameters.

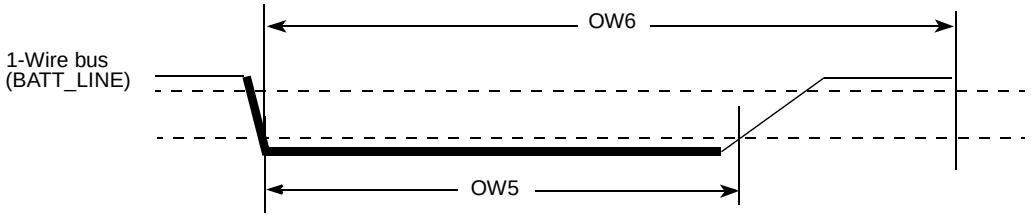


Figure 7. Write 0 Sequence Timing Diagram

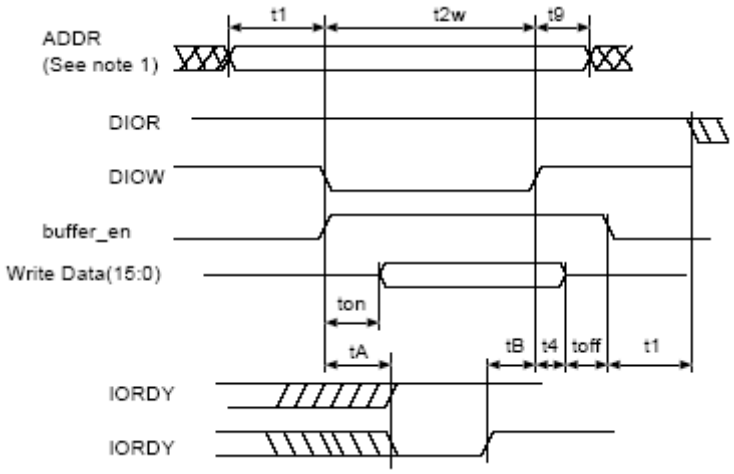


Figure 11. Multiword DMA (MDMA) Timing

Table 23. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 12 shows timing for MDMA read, Figure 13 shows timing for MDMA write, and Table 24 lists the timing parameters for MDMA read and write.

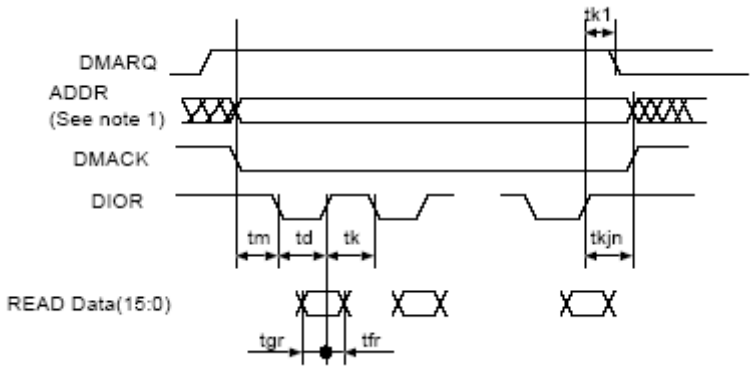


Figure 12. MDMA Read Timing Diagram

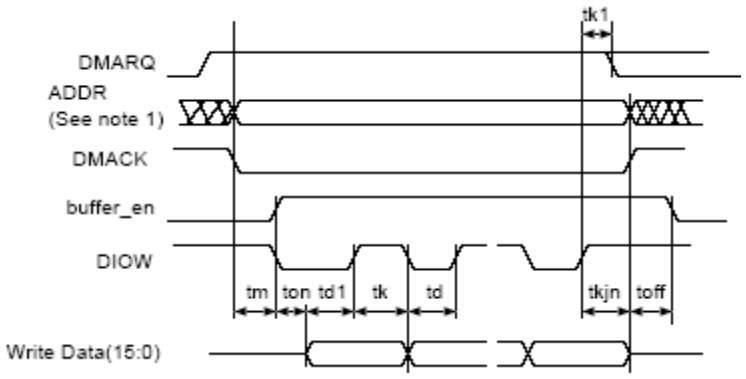


Figure 13. MDMA Write Timing Diagram

Table 24. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 12, Figure 13	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

Table 27. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	30	—	ns
CS3	SCLK Rise or Fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	SSx pulse width	t_{CSLH}	25	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	25	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	25	—	ns
CS7	Data Out Setup Time	t_{Smosi}	5	—	ns
CS8	Data Out Hold Time	t_{Hmosi}	5	—	ns
CS9	Data In Setup Time	t_{Smiso}	6	—	ns
CS10	Data In Hold Time	t_{Hmiso}	5	—	ns
CS11	$\overline{\text{SPI_RDY}}$ Setup Time[1]	t_{SRDY}	—	—	ns

1 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31C (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

4.3.8.1 Electrical Specifications

Table 28 lists the DPLL specification.

Table 28. DPLL Specifications

Parameter	Min	Typ	Max	Unit	Comments
CKIH frequency	15	26[1]	75[2]	MHz	—
CKIL frequency (Frequency Pre-multiplier (FPM) enable mode)	—	32; 32.768, 38.4	—	kHz	FPM lock time ≈ 480 µs.
Predivision factor (PD bits)	1	—	16	—	—
PLL reference frequency range after Predivider	15	—	35	MHz	15 ≤ CKIH frequency/PD ≤ 35 MHz 15 ≤ FPM output/PD ≤ 35 MHz
PLL output frequency range: MPLL and SPLL UPLL	 52 190	—	 400 240	MHz	—
Maximum allowed reference clock phase noise.	—	—	± 100	ps	—
Frequency lock time (FOL mode or non-integer MF)	—	—	398	—	Cycles of divided reference clock.

Table 30. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{OE}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{EB}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{EB}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{LBA}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{LBA}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{ECB}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{ECB}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{DTACK}$ setup time[1]	0	—	ns
WE20	$\overline{DTACK}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 27, Figure 28, Figure 29, Figure 30, Figure 31, and Figure 32 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 30 for specific control parameter settings.

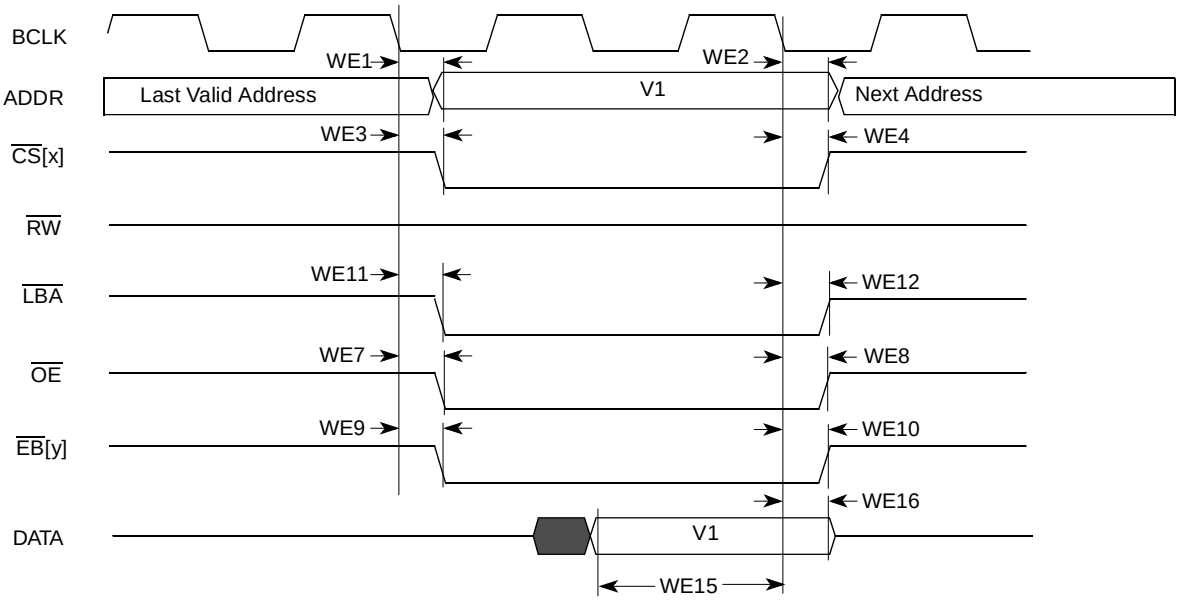


Figure 27. Asynchronous Memory Timing Diagram for Read Access—WSC=1

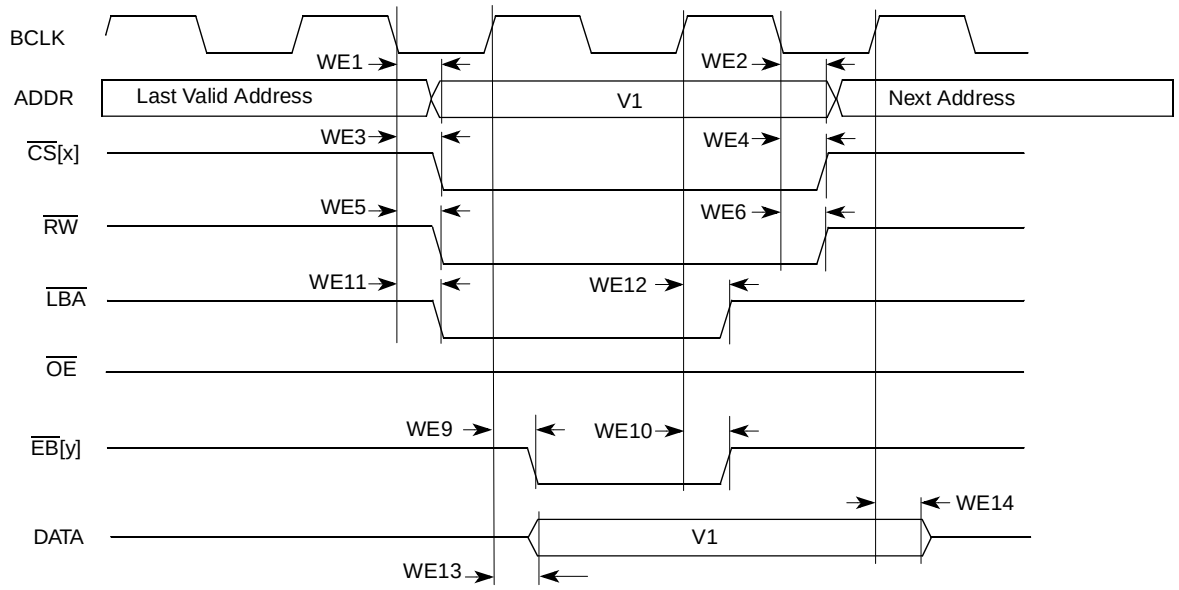


Figure 28. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

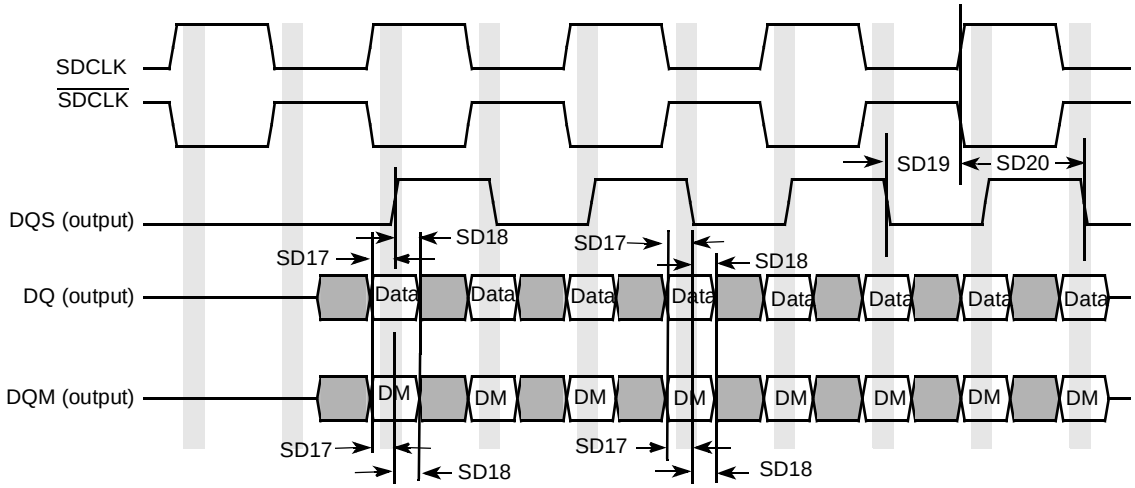


Figure 37. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 35. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min	Max	Unit
SD17	DQ & DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ & DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

1 Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.15.4.2 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.3.15.2.2, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics” on page 55.

4.3.15.5 Asynchronous Interfaces

4.3.15.5.1 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock. The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) of by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals changes only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k) and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK. In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode. In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 51, Figure 52, Figure 53, and Figure 54. These timing images correspond to active-low DISPB_D#_CS, DISPB_D#_WR and DISPB_D#_RD signals.

Additionally, the IPU allows a programmable pause between two burst. The pause is defined in the HSP_CLK cycles. It allows to avoid timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

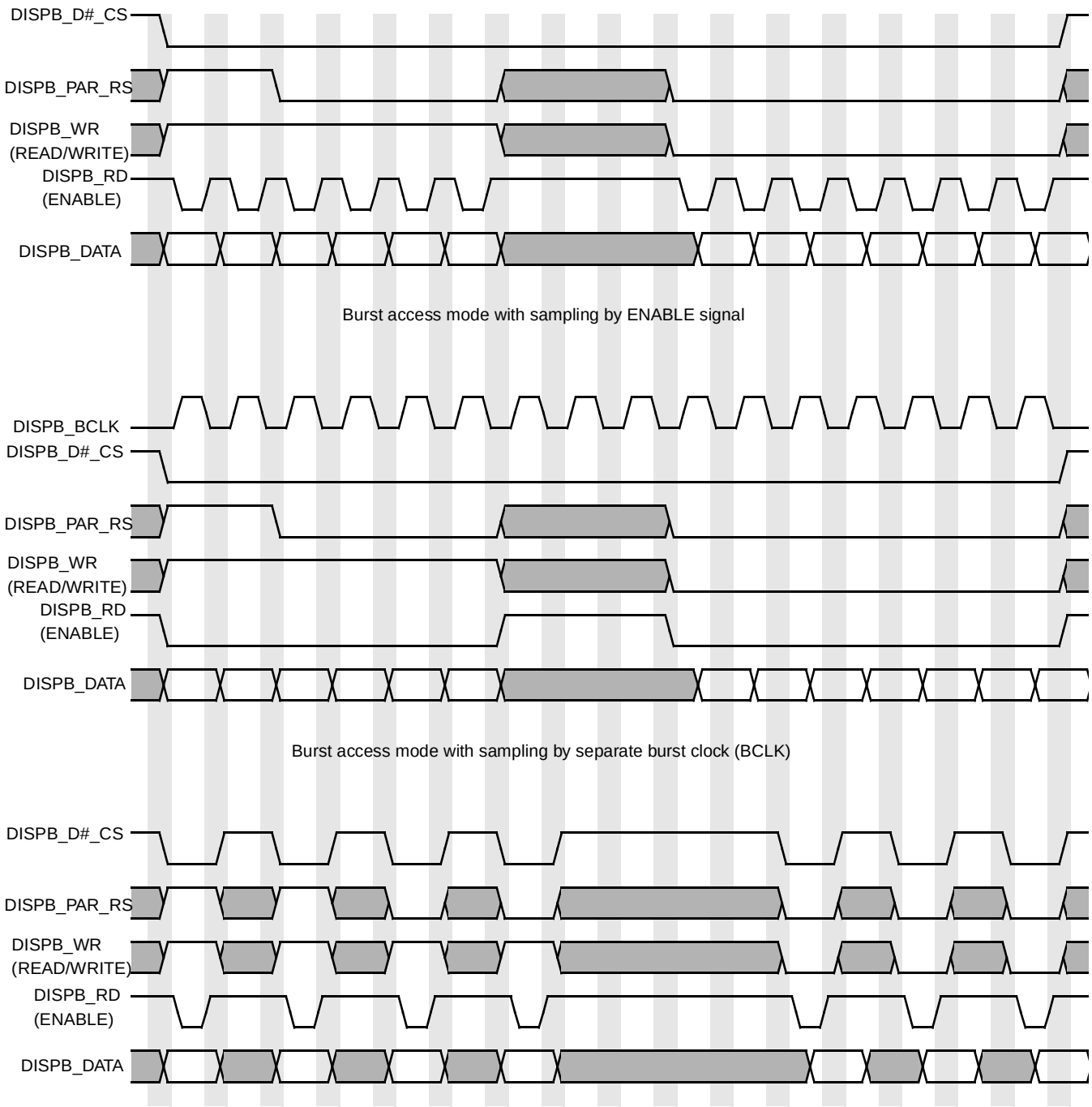


Figure 54. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the DI_DISP0_TIME_CONF_3, DI_DISP1_TIME_CONF_3, DI_DISP2_TIME_CONF_3 Registers. Figure 55 shows timing of the parallel interface with read wait states.

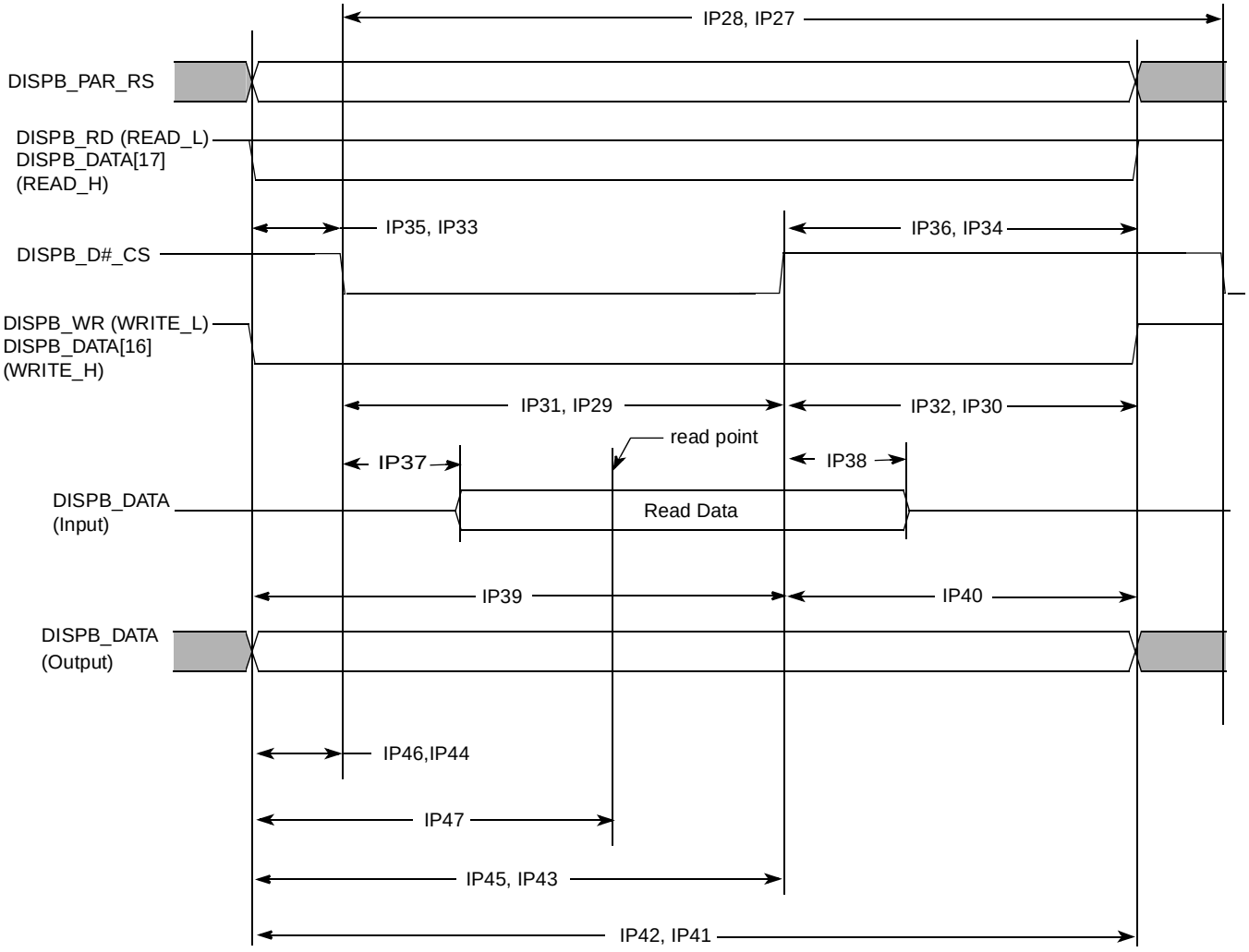


Figure 56. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

Figure 63 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

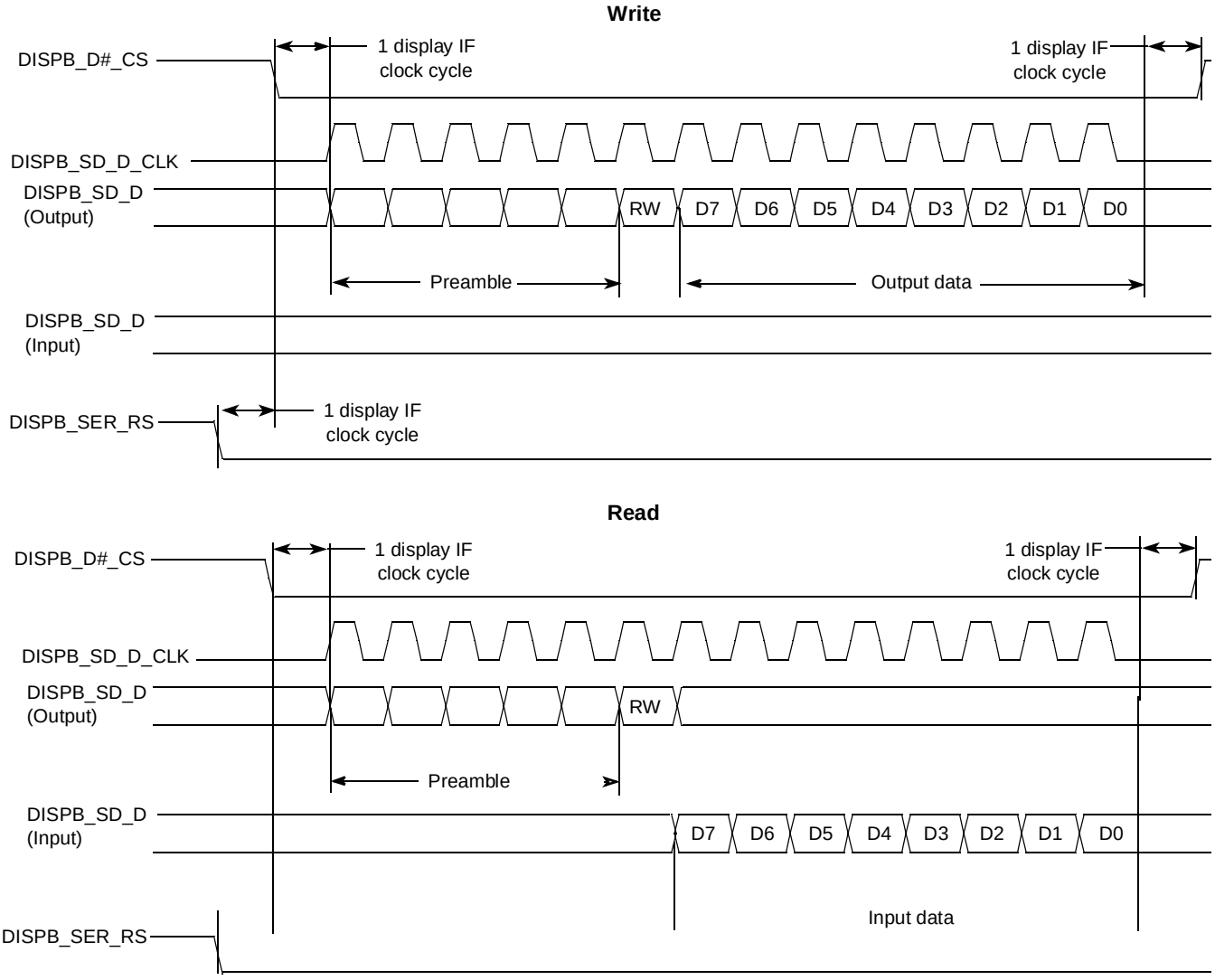


Figure 63. 5-Wire Serial Interface (Type 2) Timing Diagram

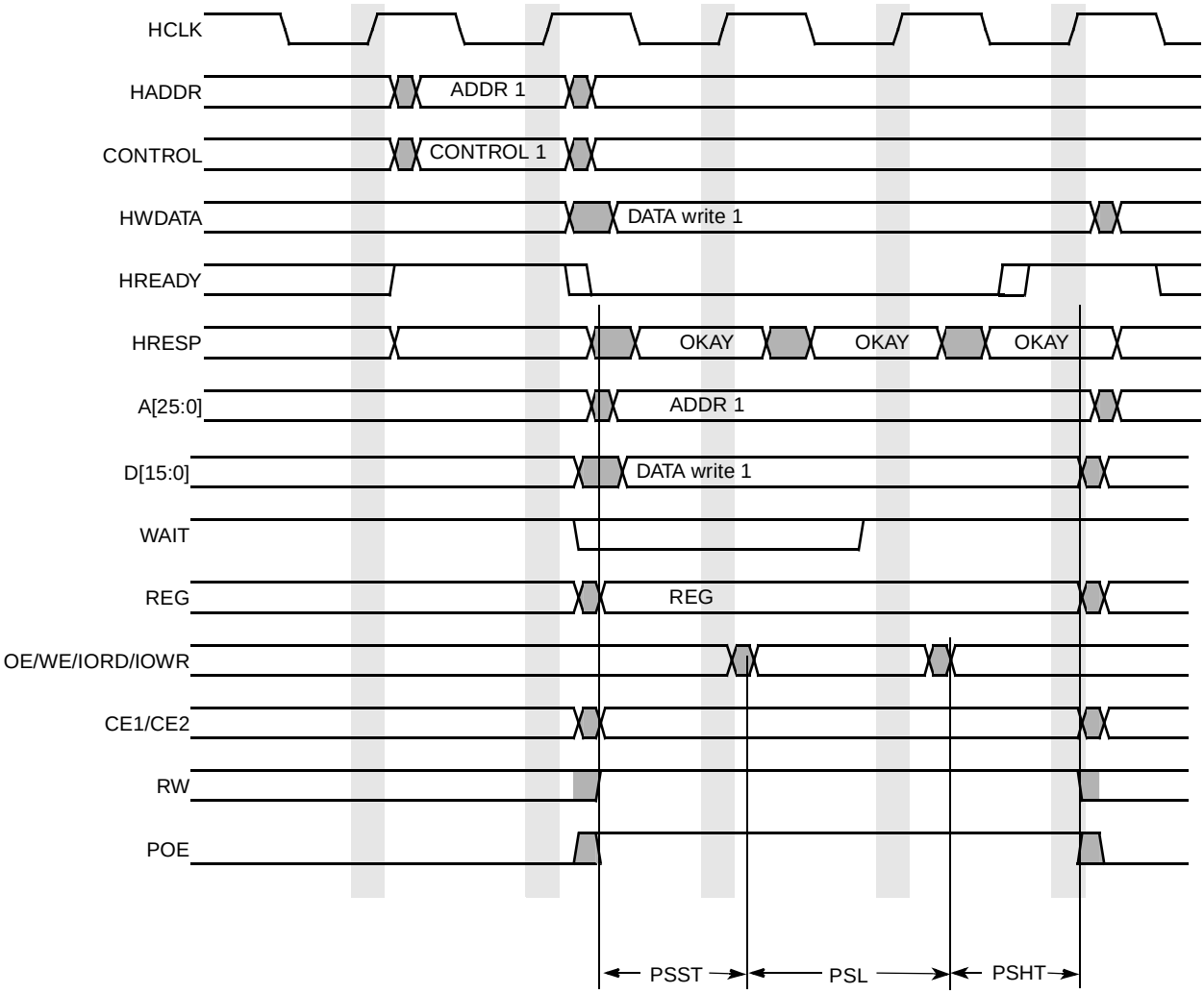


Figure 68. Write Accesses Timing Diagram—PSHT=1, PSST=1

4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 76 depicts the SJC test clock input timing. Figure 77 depicts the SJC boundary scan timing, Figure 78 depicts the SJC test access port, Figure 79 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 56 lists the SJC timing parameters.

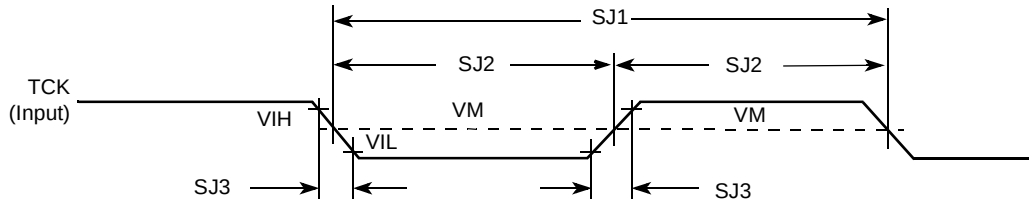


Figure 76. Test Clock Input Timing Diagram

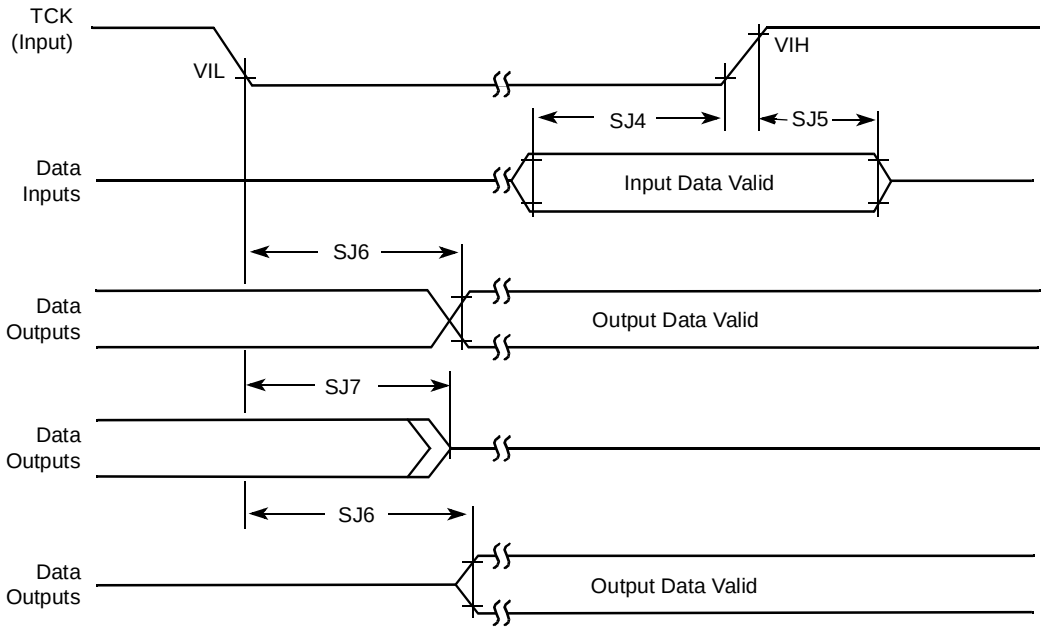
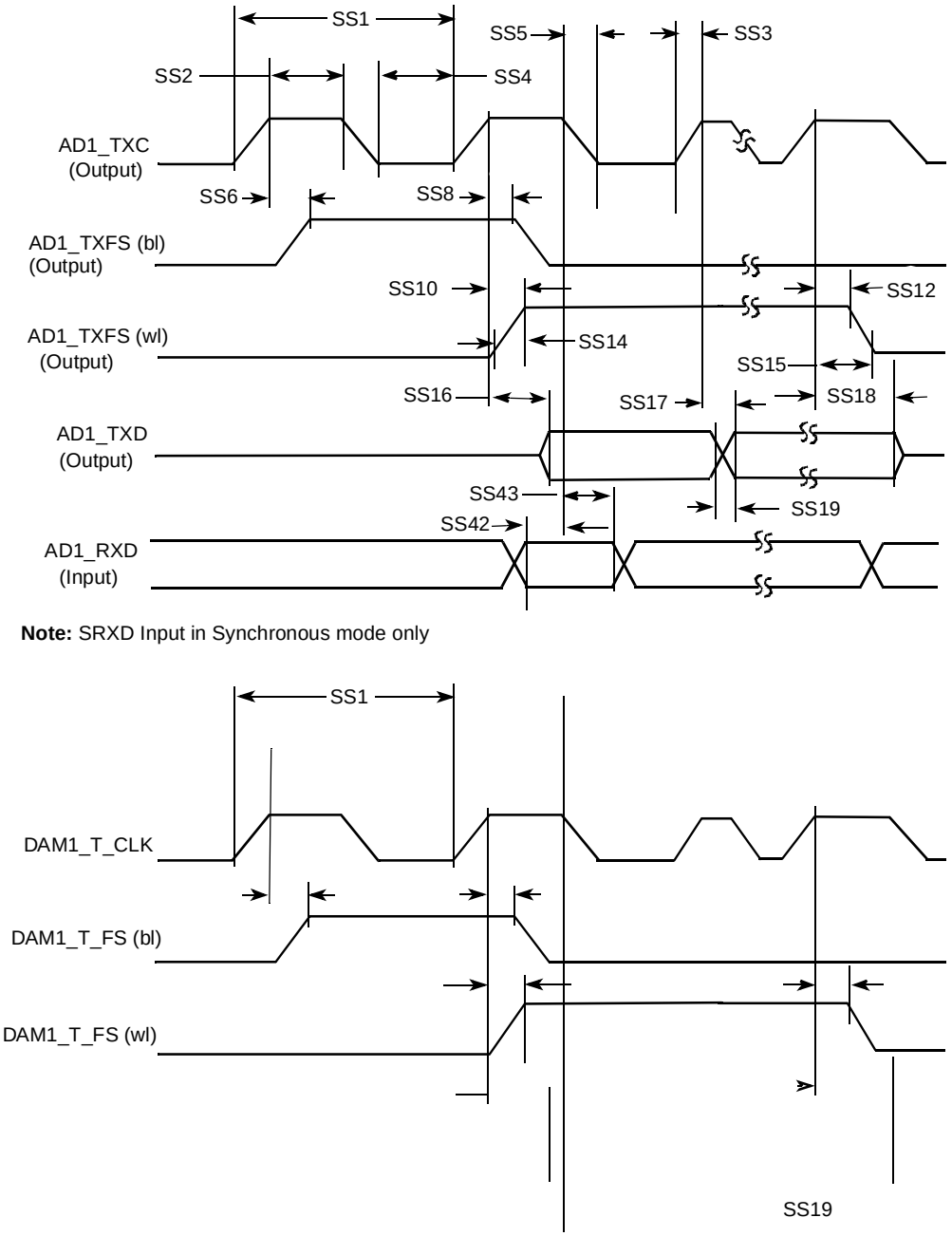


Figure 77. Boundary Scan (JTAG) Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 80. SSI Transmitter with Internal Clock Timing Diagram

5 Package Information and Pinout

This section includes the contact assignment information and mechanical package drawing for the MCIMX31C.

5.1.3 Connection Tables–19 x 19 mm 0.8 mm

Table 62 shows the device connection list for power and ground, alpha-sorted followed by Table 63 on page 103 which shows the no-connects. Table 64 on page 103 shows the device connection list for signals.

5.1.3.1 Ground and Power ID Locations—19 x 19 mm 0.8 mm

Table 62. 19 x 19 BGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	U16
FUSE_VDD	T15
FVCC	T16
GND	A1, A2, A3, A21, A22, A23, B1, B2, B22, B23, C1, C2, C22, C23, D22, D23, J12, J13, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R12, Y1, Y23, AA1, AA2, AA22, AA23, AB1, AB2, AB21, AB22, AB23, AC1, AC2, AC21, AC22, AC23
IOQVDD	T8
MGND	U14
MVCC	U15
NVCC1	G15, G16, H16, J17
NVCC2	N16, P16, R15, R16, T14
NVCC3	K7, K8, L7, L8
NVCC4	H14, J15, K15
NVCC5	G9, G10, H8, H9
NVCC6	G11, G12, G13, H12
NVCC7	H15, J16, K16, L16, M16
NVCC8	H10, H11, J11
NVCC9	G14
NVCC10	P8, R7, R8, R9, T9
NVCC21	T11, T12, T13, U11
NVCC22	T10, U7, U8, U9, U10, V6, V7, V8, V9, V10
QVCC	H13, J14, L15, M15, N9, N15, P9, P15, R10, R11, R13, R14
QVCC1	J8, J9, J10, K9
QVCC4	L9, M7, M8, N8
SGND	U13
SVCC	U12
UVCC	P18
UGND	P17

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