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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c31x2-lcb

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4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C31X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: TCON, TH0, TH1, TMOD, TL0, TL1
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: CKCON

Table 1. All SFRs with their address and their reset value

	Bit address- able			Non	n Bit address	able			
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h									CFh
C0h									C7h
B8h	IP XXX0 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XXX0 0000	B7h
A8h	IE 0XX0 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000		CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved



Table 2.	Pin	Description	for	40/44	pin	packages
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MNEMONIC	PIN NUMBER		TVDE	NAME AND FUNCTION			
MINEMONIC	DIL	LCC	VQFP 1.4	ITTE	NAME AND FUNCTION		
V _{SS}	20	22	16	Ι	Ground: 0V reference		
Vss1		1	39	Ι	Optional Ground: Contact the Sales Office for ground connection.		
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle and power- down operation		
P0.0-P0.7	39-32	43-36	37-30	I/O	Port 0 : Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1 written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption Port 0 is also the multiplexed low-order address and data bus during access t external program and data memory. In this application, it uses strong internal pull-up when emitting 1s.		
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups.		
P2.0-P2.7	21-28	24-31	18-25	I/O	Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR.		
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.		
	10	11	5	I	RXD (P3.0): Serial input port		
	11	13	7	0	TXD (P3.1): Serial output port		
	12	14	8	I	INTO (P3.2): External interrupt 0		
	13	15	9	I	INT1 (P3.3): External interrupt 1		
	14	16	10	I	T0 (P3.4): Timer 0 external input		
	15	17	11	I	T1 (P3.5): Timer 1 external input		
	16	18	12	0	WR (P3.6): External data memory write strobe		
	17	19	13	0	RD (P3.7): External data memory read strobe		
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} .		
ALE	30	33	27	O (I)	Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.		
PSEN	29	32	26	0	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, <u>PSEN</u> is activated twice each machine cycle, except that two <u>PSEN</u> activations are skipped during each access to external data memory. <u>PSEN</u> is not activated during fetches from internal program memory.		
ĒĀ	31	35	29	I	External Access Enable: \overline{EA} must be externally held low to enable the device to fetch code from external program memory locations.		
XTAL1	19	21	15	Ι	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits		
XTAL 2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier		
111112	10	20	1.4		crystar 2. Sutput nom die inverting ösemator ampliner		



6. TS80C31X2 Enhanced Features

In comparison to the original 80C31, the TS80C31X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- Enhanced UART

6.1 X2 Feature

The TS80C31X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1+2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.







Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)



6.2 Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).



Figure 3. Use of Dual Pointer



Table 4. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	DPS	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX XXX0 Not bit addressable

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.



Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 5. and Figure 6.).







Figure 6. UART Timings in Modes 2 and 3

6.3.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).



6.3.3 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b. For example:

SADDR	0101	0110b
SADEN	1111	1100b
Given	0101	01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR <u>SADEN</u> Given	1111 0001b <u>1111 1010b</u> 1111 0X0Xb
Slave B:	SADDR <u>SADEN</u> Given	1111 0011b <u>1111 1001b</u> 1111 0XX1b
Slave C:	SADDR <u>SADEN</u> Given	1111 0010b <u>1111 1101b</u> 1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

6.3.4 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

0101	0110b
1111	1100b
1111	111Xb
	0101 1111 1111

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR <u>SADEN</u> Broadcast	1111 0001b <u>1111 1010b</u> 1111 1X11b,
Slave B:	SADDR <u>SADEN</u> Broadcast	1111 0011b <u>1111 1001b</u> 1111 1X11B,
Slave C:	SADDR= <u>SADEN</u> Broadcast	1111 0010b <u>1111 1101b</u> 1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.



6.4 Interrupt System

The TS80C31X2 has a total of 5 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (timers 0 and 1) and the serial port interrupt. These interrupts are shown in Figure 7.



Figure 7. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 8.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 9.) and in the Interrupt Priority High register (See Table 10.). shows the bit values and priority levels associated with each combination.



Table 7. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 8. IE Register

IE - Interrupt Enable Register (A8h)							
7	6	5	4	3	2	1	0
EA	-	-	ES	ET1	EX1	ЕТО	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b Bit addressable



IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0		
-	-	-	PS	PT1	PX1	PT0	PX0		
Bit Number	Bit Mnemonic		Description						
7	-	Reserved The value read f	rom this bit is inde	eterminate. Do not s	set this bit.				
6	-	Reserved The value read f	from this bit is inde	eterminate. Do not	set this bit.				
5	-	Reserved The value read f	rom this bit is inde	eterminate. Do not	set this bit.				
4	PS	Serial port Priority Refer to PSH fo	bit r priority level.						
3	PT1	Timer 1 overflow in Refer to PT1H f	terrupt Priority I for priority level.	bit					
2	PX1	External interrupt Refer to PX1H	External interrupt 1 Priority bit Refer to PX1H for priority level.						
1	PT0	Timer 0 overflow in Refer to PT0H f	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.						
0	PX0	External interrupt Refer to PX0H	0 Priority bit for priority level.						

Reset Value = XXX0 0000b Bit addressable



Table 10. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	-	PSH	PT1H	PX1H	РТОН	РХОН

Bit Number	Bit Mnemonic	Descri	otion					
7	-	Reserved The value read from this bit is indeterminate. Do not	eserved The value read from this bit is indeterminate. Do not set this bit.					
6	-	Reserved The value read from this bit is indeterminate. Do not	set this bit.					
5	-	Reserved The value read from this bit is indeterminate. Do not	set this bit.					
4	PSH	Serial port Priority High bitPSHPSPriority Level00Lowest01110111Highest						
3	PT1H	Timer 1 overflow interrupt Priority High bit PT1H PT1 Priority Level 0 0 Lowest 0 1 1 1 0 1 1 1 Highest						
2	PX1H	External interrupt 1 Priority High bitPX1HPX1Priority Level00Lowest01110111Highest						
1	РТОН	Timer 0 overflow interrupt Priority High bit PT0H PT0 Priority Level 0 0 Lowest 0 1 1 1 0 1 1 1 Highest						
0	РХ0Н	External interrupt 0 Priority High bit <u>PX0H</u> <u>PX0</u> 0 0 Lowest 0 1 1 0 1 1 Highest						

Reset Value = XXX0 0000b Not bit addressable



6.5 Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give and indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The over way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

6.6 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 6., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 8. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C31X2 into power-down mode.



Figure 8. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content. NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.



6.7 ONCETM Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C31X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C31X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C31X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 12. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active



6.8 Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 13.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 13. PCON Register

PCON - Power Control Register (87h)

7	6	5	5 4 3 2 1								
SMOD1	SMOD) -	- POF GF1 GF0								
Bit Number	Bit Mnemonic		Description								
7	SMOD1	Serial port Mode bi Set to select dou	t 1 ible baud rate in m	ode 1, 2 or 3.							
6	SMOD0	Serial port Mode bi Clear to select S Set to to select F	t 0 M0 bit in SCON re E bit in SCON reg	egister. ister.							
5	-	Reserved The value read f	rom this bit is inde	terminate. Do not s	set this bit.						
4	POF	Power-Off Flag Clear to recogniz Set by hardware	ze next reset type. when V _{CC} rises fr	om 0 to its nomina	l voltage. Can also	be set by software					
3	GF1	General purpose Flac Cleared by user Set by user for g	ag for general purpose eneral purpose usa	e usage. ge.							
2	GF0	General purpose Flac Cleared by user Set by user for g	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.								
1	PD	Power-Down mode Cleared by hard Set to enter powe	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.								
0	IDL	Idle mode bit Clear by hardwa Set to enter idle	dle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.								

Reset Value = 00X1 0000b Not bit addressable



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I _{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 13.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.; $\overline{EA} = RST = Port 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used.

2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port $0 = V_{CC}$; $\overline{EA} = RST = V_{SS}$ (see Figure 11.).

3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT $0 = V_{CC}$; XTAL2 NC.; RST = V_{SS} (see Figure 12.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port:

Port 0: 26 mA

Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 13.), $V_{IL} = V_{SS} + 0.5$ V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port \ 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 9. I_{CC} Test Condition, under reset



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	х	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

Table 20. AC Parameter	s for	a Variable	Clock:	derating	formula
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7.5.3 External Program Memory Read Cycle



Figure 14. External Program Memory Read Cycle



7.5.4 External Data Memory Characteristics

Table 21. Symbol Description

Symbol	Parameter
T _{RLRH}	RD Pulse Width
T _{WLWH}	WR Pulse Width
T _{RLDV}	RD to Valid Data In
T _{RHDX}	Data Hold After RD
T _{RHDZ}	Data Float After RD
T _{LLDV}	ALE to Valid Data In
T _{AVDV}	Address to Valid Data In
T _{LLWL}	ALE to WR or RD
T _{AVWL}	Address to \overline{WR} or \overline{RD}
T _{QVWX}	Data Valid to WR Transition
T _{QVWH}	Data set-up to WR High
T _{WHQX}	Data Hold After WR
T _{RLAZ}	RD Low to Address Float
T _{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE high



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T _{RHDX}	Min	x	x	0	0	0	ns
T _{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T _{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T _{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T _{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T _{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T _{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T _{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T _{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T _{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T _{RLAZ}	Max	x	x	0	0	0	ns
T _{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T _{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

 Table 23. AC Parameters for a Variable Clock: derating formula

7.5.5 External Data Memory Write Cycle



Figure 15. External Data Memory Write Cycle





Table 29. Possible Ordering Entries

	TS80C31X2 ROMless
-MCA	Х
-MCB	Х
-MCC	Х
-MCE	Х
-VCA	Х
-VCB	Х
-VCC	Х
-VCE	Х
-LCA	Х
-LCB	Х
-LCC	Х
-LCE	Х
-MIA	Х
-MIB	Х
-MIC	Х
-MIE	Х
-VIA	Х
-VIB	Х
-VIC	Х
-VIE	Х
-LIA	Х
-LIB	Х
-LIC	Х
-LIE	Х
-EA	Х
-EB	Х
-EC	Х
-EE	Х

- -Ex for samples
- Tape and Reel available for B, C and E packages
- Dry pack mandatory for E packages