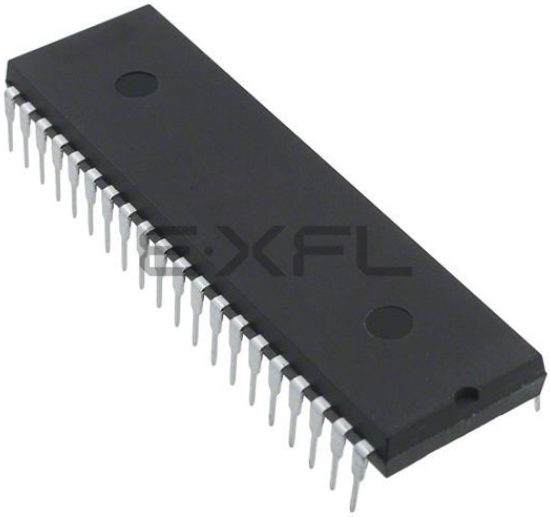

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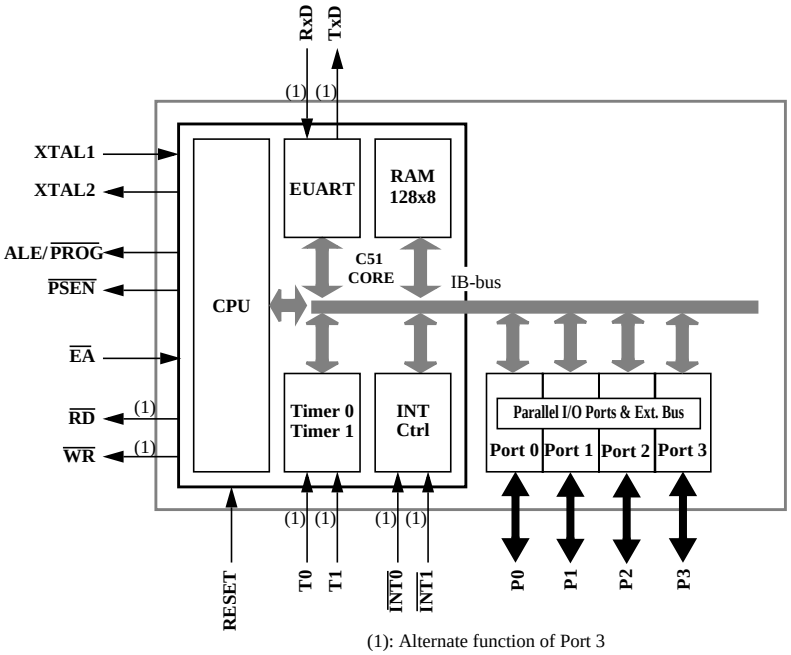
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c31x2-lia

3. Block Diagram



(1): Alternate function of Port 3

Table 2. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIL	LCC	VQFP 1.4		
V_{SS}	20	22	16	I	**Ground:** 0V reference
Vss1		1	39	I	**Optional Ground:** Contact the Sales Office for ground connection.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR.
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	**RXD (P3.0):** Serial input port
	11	13	7	O	**TXD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt 0
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt 1
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to $V_{CC.}$
ALE	30	33	27	O (I)	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{PSEN}$	29	32	26	O	**Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$	31	35	29	I	**External Access Enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier

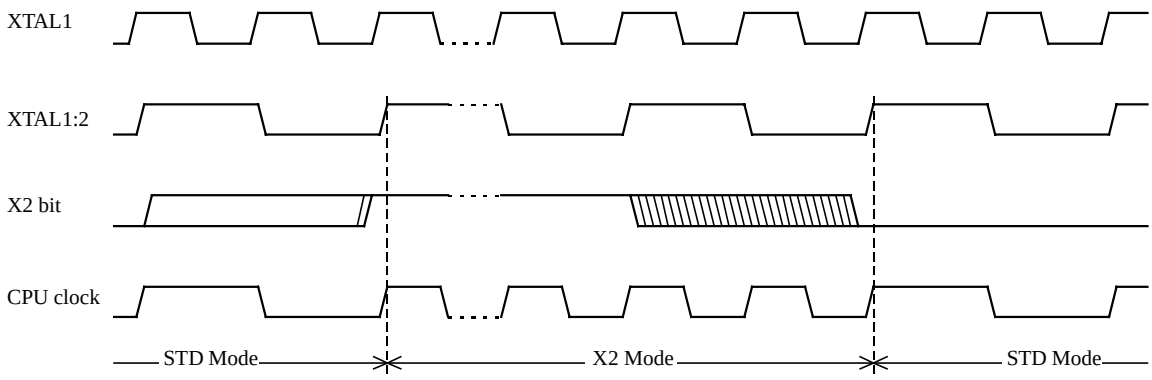


Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 4. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**DPS**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX XXX0
Not bit addressable

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a ’source’ pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE      ; address of SOURCE
0003 05A2   INC   AUXR1          ; switch data pointers
0005 90A000 MOV DPTR,#DEST       ; address of DEST
0008          LOOP:
0008 05A2   INC   AUXR1          ; switch data pointers
000A E0     MOVX A,@DPTR         ; get a byte from SOURCE
000B A3     INC   DPTR           ; increment SOURCE address
000C 05A2   INC   AUXR1          ; switch data pointers
000E F0     MOVX @DPTR,A         ; write the byte to DEST
000F A3     INC   DPTR           ; increment DEST address
0010 70F6   JNZ   LOOP           ; check for 0 terminator
0012 05A2   INC   AUXR1          ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 5. and Figure 6.).

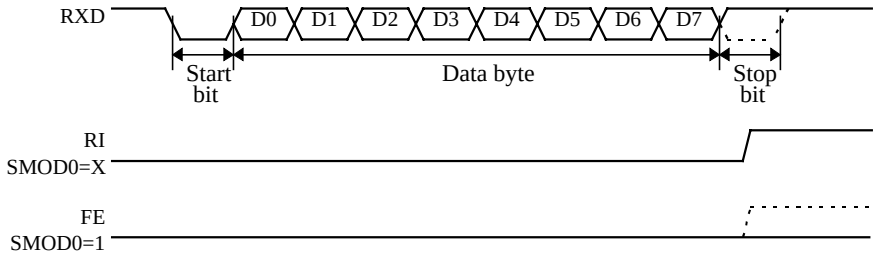


Figure 5. UART Timings in Mode 1

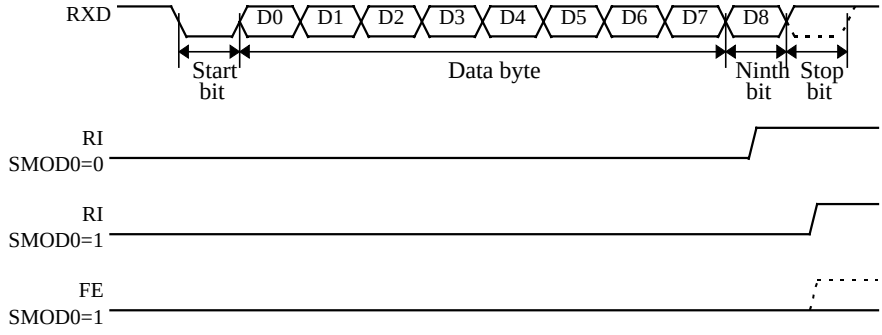


Figure 6. UART Timings in Modes 2 and 3

6.3.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

6.3.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 5. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register F_{XTAL}/12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F_{XTAL}/64 or F_{XTAL}/32 (/32, /16 in X2 mode) 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.** Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 5. and Figure 6. in the other modes.

Reset Value = 0000 0000b
Bit addressable

Table 6. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

6.4 Interrupt System

The TS80C31X2 has a total of 5 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (timers 0 and 1) and the serial port interrupt. These interrupts are shown in Figure 7.

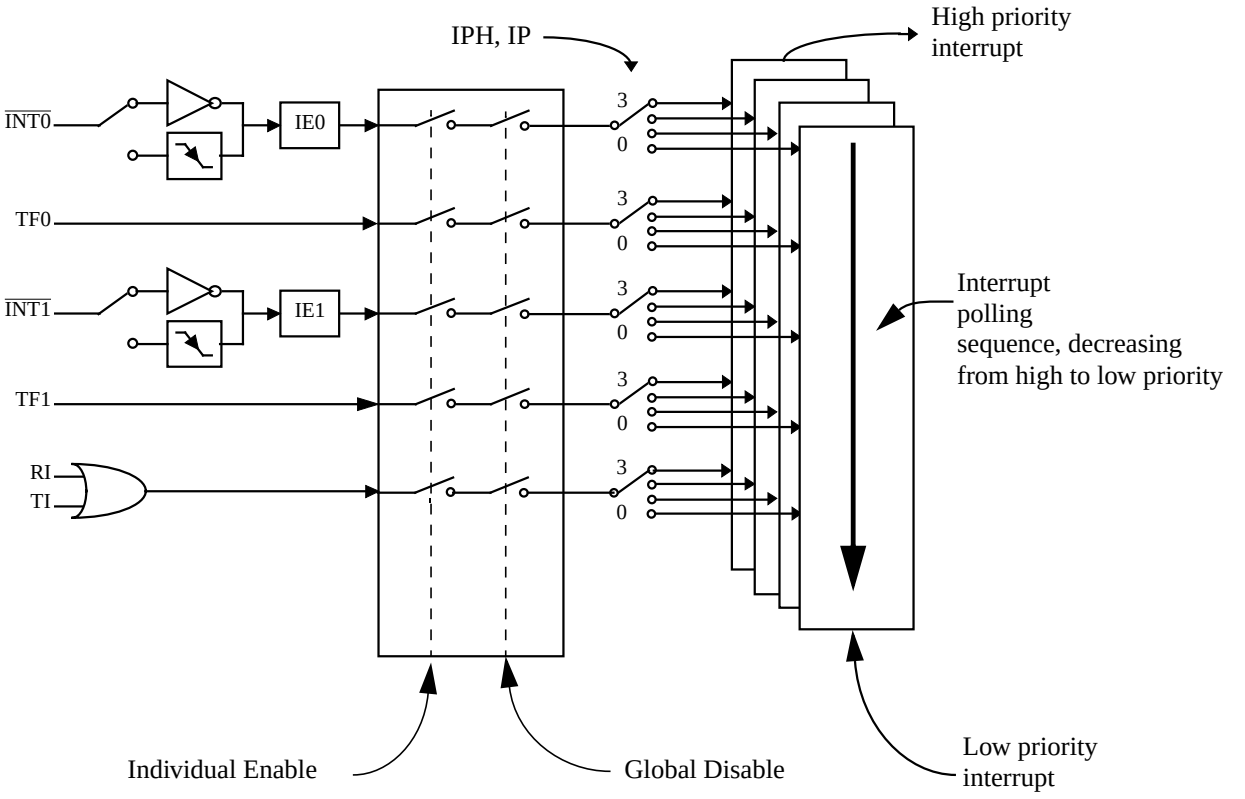


Figure 7. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 8.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 9.) and in the Interrupt Priority High register (See Table 10.). shows the bit values and priority levels associated with each combination.

6.7 ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C31X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C31X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{PSEN}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C31X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 12. External Pin Status during ONCE Mode

ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

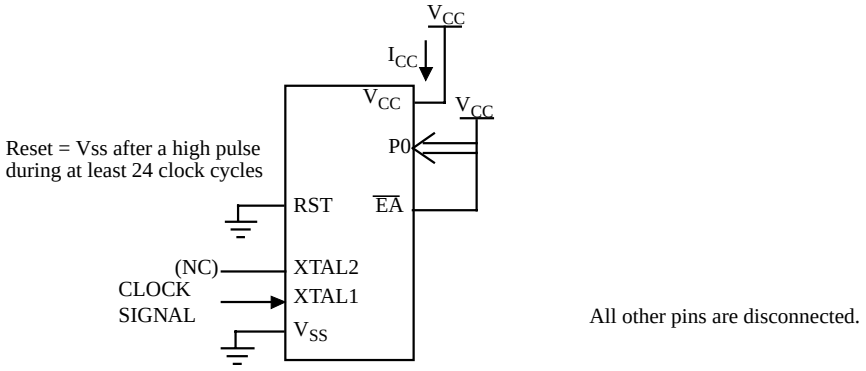


Figure 10. Operating I_{CC} Test Condition

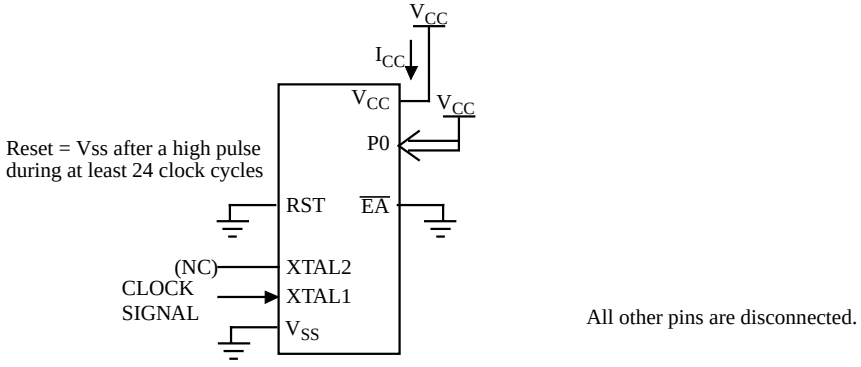


Figure 11. I_{CC} Test Condition, Idle Mode

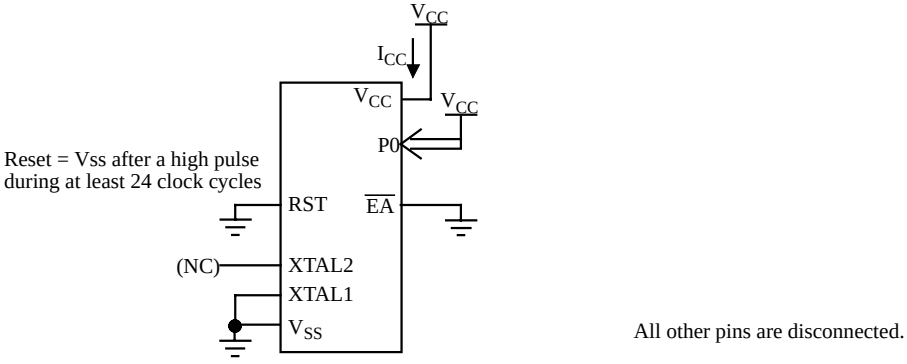


Figure 12. I_{CC} Test Condition, Power-Down Mode

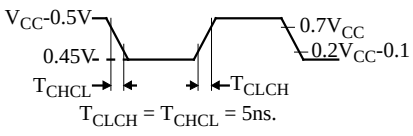


Figure 13. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

7.5 AC Parameters

7.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

TA = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
TA = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
TA = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.
TA = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.

Table 16. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{PSEN}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 16. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{PSEN}$	100	30	100

Table 18., Table 21. and Table 24. give the description of each AC symbols.

Table 19., Table 22. and Table 25. give for each range the AC parameter.

Table 20., Table 23. and Table 26. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 17. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:
T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):
x= 25 (Table 20.)
T= 50ns
T_{LLIV}= 2T - x = 2 x 50 - 25 = 75ns

7.5.2 External Program Memory Characteristics

Table 18. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 19. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T	25		33		25		50		33		ns
T_{LHLL}	40		25		42		35		52		ns
T_{AVLL}	10		4		12		5		13		ns
T_{LLAX}	10		4		12		5		13		ns
T_{LLIV}		70		45		78		65		98	ns
T_{LLPL}	15		9		17		10		18		ns
T_{PLPH}	55		35		60		50		75		ns
T_{PLIV}		35		25		50		30		55	ns
T_{PXIX}	0		0		0		0		0		ns
T_{PXIZ}		18		12		20		10		18	ns
T_{AVIV}		85		53		95		80		122	ns
T_{PLAZ}		10		10		10		10		10	ns

Table 20. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

7.5.3 External Program Memory Read Cycle

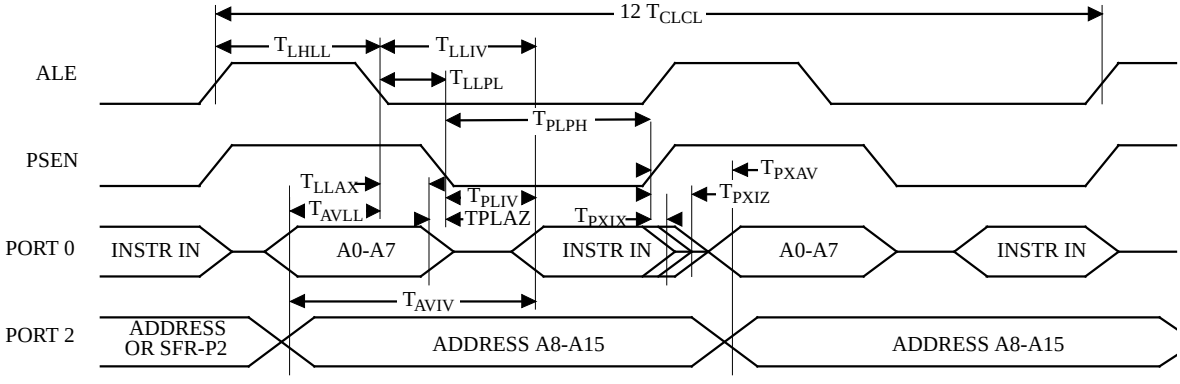


Figure 14. External Program Memory Read Cycle

7.5.4 External Data Memory Characteristics

Table 21. Symbol Description

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

Table 22. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDX}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Table 23. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T_{RHDX}	Min	x	x	0	0	0	ns
T_{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T_{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T_{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T_{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T_{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T_{RLAZ}	Max	x	x	0	0	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T_{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

7.5.5 External Data Memory Write Cycle

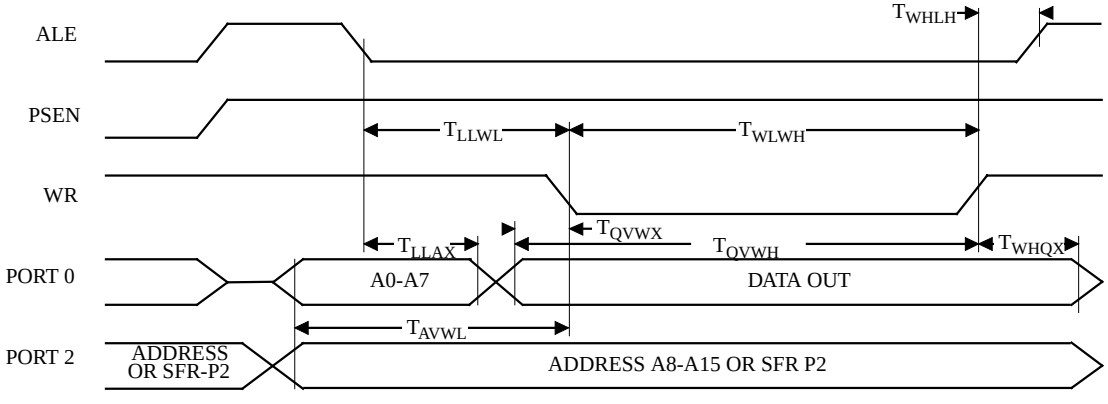


Figure 15. External Data Memory Write Cycle

Table 26. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDX}	Min	x	x	0	0	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	133	133	ns

7.5.8 Shift Register Timing Waveforms

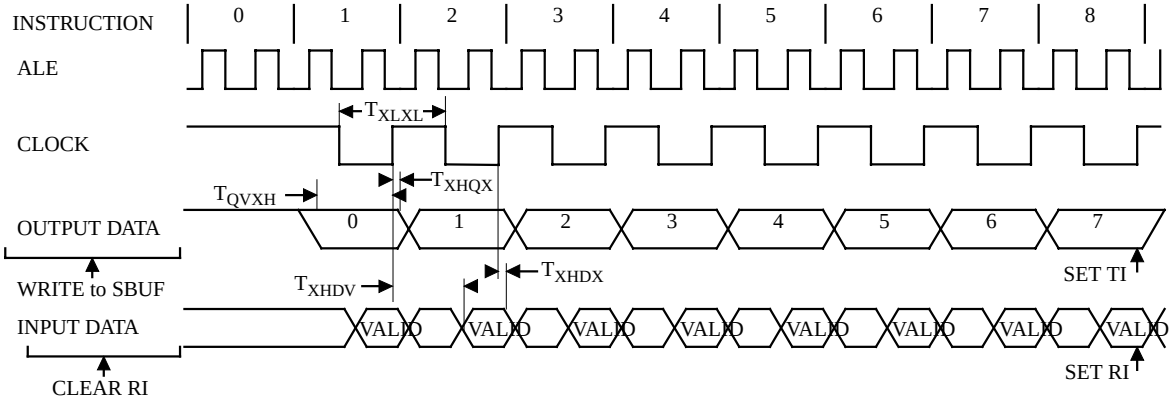


Figure 17. Shift Register Timing Waveforms

7.5.9 External Clock Drive Characteristics (XTAL1)

Table 27. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

7.5.10 External Clock Drive Waveforms

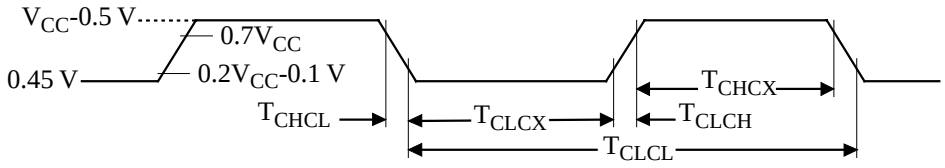


Figure 18. External Clock Drive Waveforms

7.5.11 AC Testing Input/Output Waveforms

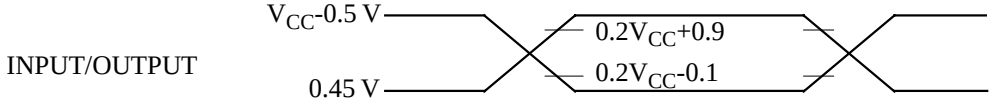


Figure 19. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

7.5.12 Float Waveforms

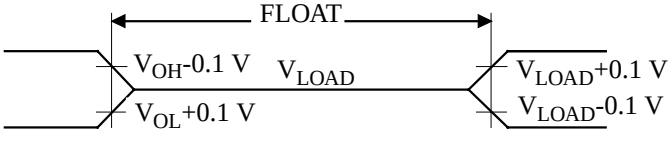


Figure 20. Float Waveforms