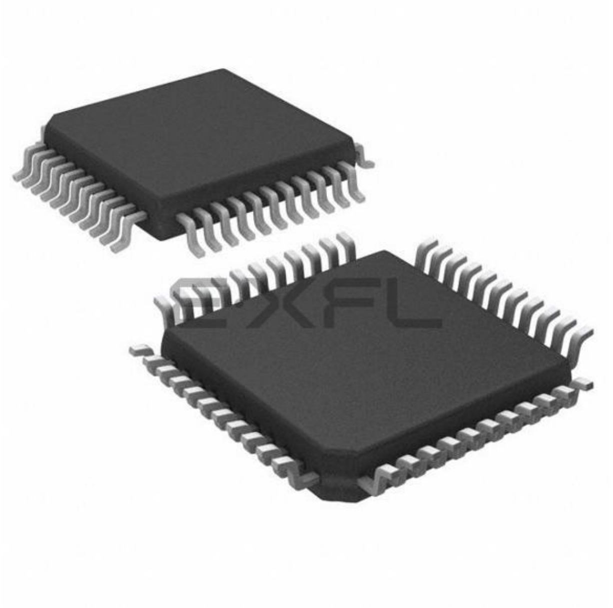
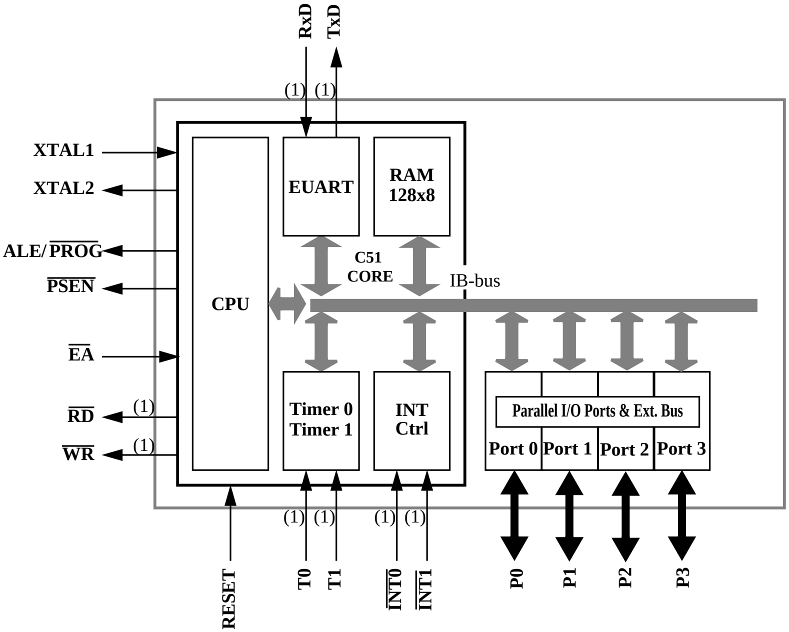
# Microchip Technology - TS80C31X2-LIC Datasheet



| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 30/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-QFP |
| Supplier Device Package | 44-PQFP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts80c31x2-lic |

## 3. Block Diagram



(1): Alternate function of Port 3

### Table 2. Pin Description for 40/44 pin packages

| MNEMONIC | PIN NUMBER | | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|
| | DIL | LCC | VQFP 1.4 | | |
| $V_{SS}$ | 20 | 22 | 16 | I | **Ground:** 0V reference |
| Vss1 | | 1 | 39 | I | **Optional Ground:** Contact the Sales Office for ground connection. |
| $V_{CC}$ | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for normal, idle and power-down operation |
| P0.0-P0.7 | 39-32 | 43-36 | 37-30 | I/O | **Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. |
| P1.0-P1.7 | 1-8 | 2-9 | 40-44<br>1-3 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. |
| P2.0-P2.7 | 21-28 | 24-31 | 18-25 | I/O | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. |
| P3.0-P3.7 | 10-17 | 11,<br>13-19 | 5,<br>7-13 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below. |
| | 10 | 11 | 5 | I | **RXD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TXD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{\text{INT0}}$ (P3.2):** External interrupt 0 |
| | 13 | 15 | 9 | I | **$\overline{\text{INT1}}$ (P3.3):** External interrupt 1 |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input |
| | 16 | 18 | 12 | O | **$\overline{\text{WR}}$ (P3.6):** External data memory write strobe |
| | 17 | 19 | 13 | O | **$\overline{\text{RD}}$ (P3.7):** External data memory read strobe |
| Reset | 9 | 10 | 4 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC.}$ |
| ALE | 30 | 33 | 27 | O (I) | **Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. |
| $\overline{\text{PSEN}}$ | 29 | 32 | 26 | O | **Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. |
| $\overline{\text{EA}}$ | 31 | 35 | 29 | I | **External Access Enable:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations. |
| XTAL1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier |

# 6. TS80C31X2 Enhanced Features

In comparison to the original 80C31, the TS80C31X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- Enhanced UART

## 6.1 X2 Feature

The TS80C31X2 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.

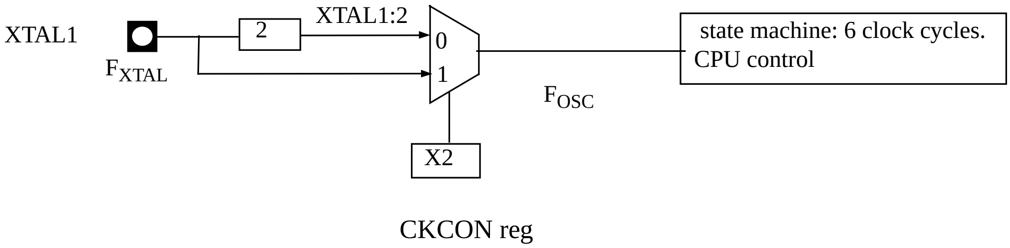


**Figure 1. Clock Generation Diagram**

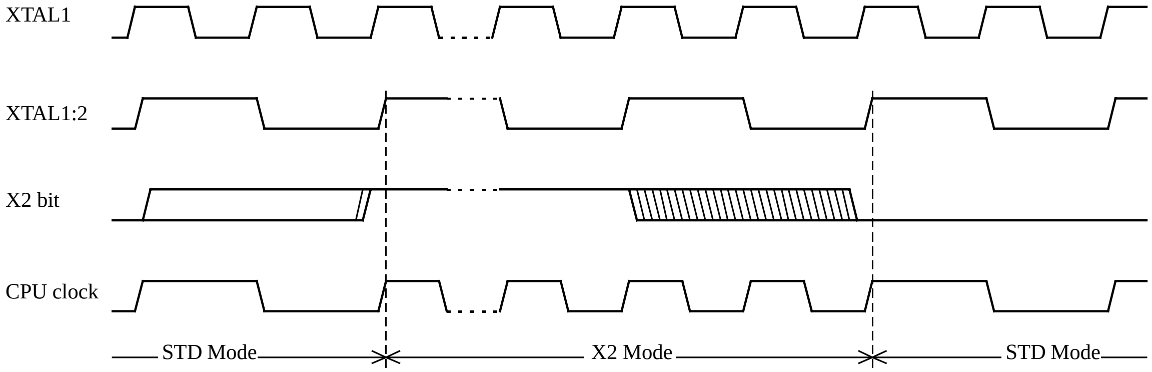


**Figure 2. Mode Switching Waveforms**

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

**CAUTION**
In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

## 6.2 Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

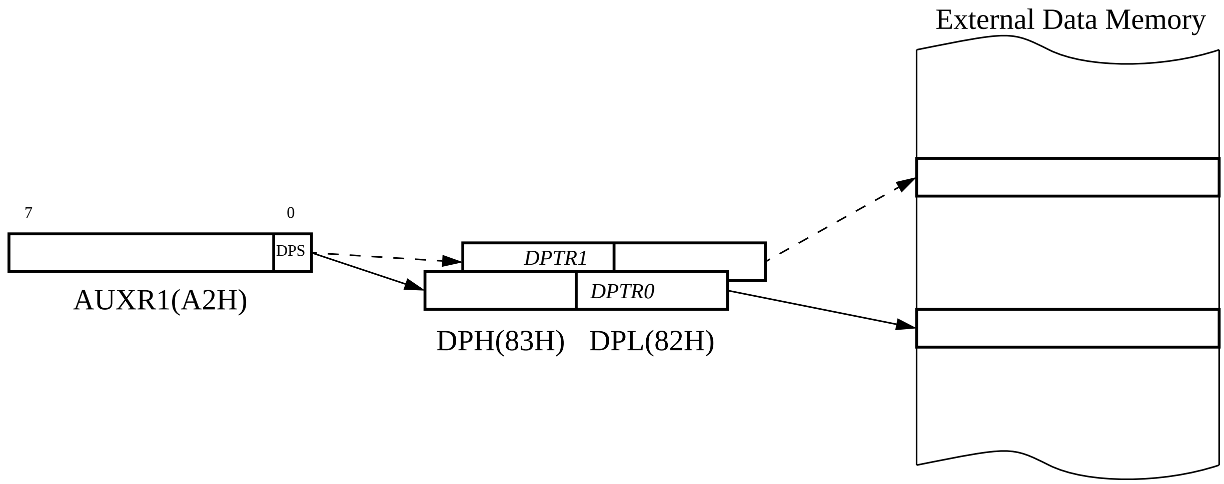


**Figure 3. Use of Dual Pointer**

## 6.3 TS80C31X2 Serial I/O Port

The serial I/O port in the TS80C31X2 is compatible with the serial I/O port in the 80C31.
It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

### 6.3.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 4).

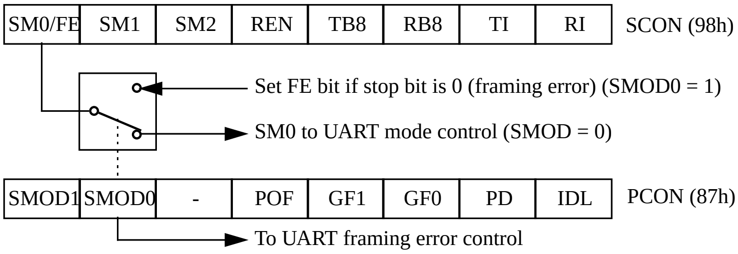


**Figure 4. Framing Error Block Diagram**

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 5.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 5. and Figure 6.).

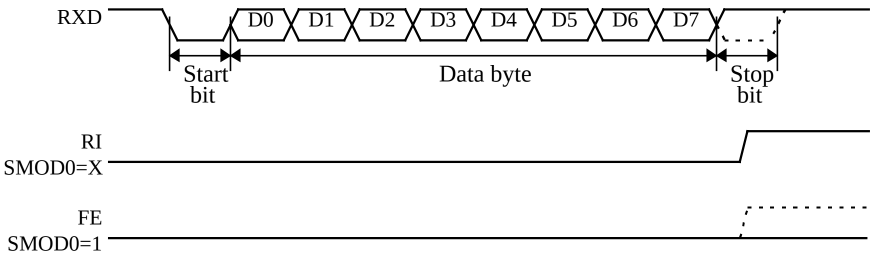


**Figure 5. UART Timings in Mode 1**

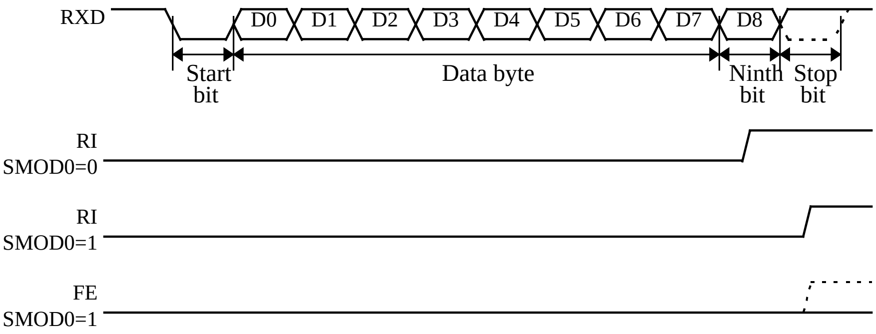


**Figure 6. UART Timings in Modes 2 and 3**

### 6.3.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device’s address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

*NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).*

### 6.3.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are `XXXX XXXXb` (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

**SADEN - Slave Address Mask Register (B9h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Reset Value = 0000 0000b
Not bit addressable

**SADDR - Slave Address Register (A9h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Reset Value = 0000 0000b
Not bit addressable

## Table 5. SCON Register

**SCON - Serial Control Register (98h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **FE/SM0** | **SM1** | **SM2** | **REN** | **TB8** | **RB8** | **TI** | **RI** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | FE | **Framing Error bit (SMOD0=1)**<br>Clear to reset the error state, not cleared by a valid stop bit.<br>Set by hardware when an invalid stop bit is detected.<br>SMOD0 must be set to enable access to the FE bit |
|  | SM0 | **Serial port Mode bit 0**<br>Refer to SM1 for serial port mode selection.<br>SMOD0 must be cleared to enable access to the SM0 bit |
| 6 | SM1 | **Serial port Mode bit 1**<br>SM0 SM1 Mode Description Baud Rate<br>0 0 0 Shift Register $F_{XTAL}$/12 (/6 in X2 mode)<br>0 1 1 8-bit UART Variable<br>1 0 2 9-bit UART $F_{XTAL}$/64 or $F_{XTAL}$/32 (/32, /16 in X2 mode)<br>1 1 3 9-bit UART Variable |
| 5 | SM2 | **Serial port Mode 2 bit / Multiprocessor Communication Enable bit**<br>Clear to disable multiprocessor communication feature.<br>Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0. |
| 4 | REN | **Reception Enable bit**<br>Clear to disable serial reception.<br>Set to enable serial reception. |
| 3 | TB8 | **Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.**<br>Clear to transmit a logic 0 in the 9th bit.<br>Set to transmit a logic 1 in the 9th bit. |
| 2 | RB8 | **Receiver Bit 8 / Ninth bit received in modes 2 and 3**<br>Cleared by hardware if 9th bit received is a logic 0.<br>Set by hardware if 9th bit received is a logic 1.<br>In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used. |
| 1 | TI | **Transmit Interrupt flag**<br>Clear to acknowledge interrupt.<br>Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes. |
| 0 | RI | **Receive Interrupt flag**<br>Clear to acknowledge interrupt.<br>Set by hardware at the end of the 8th bit time in mode 0, see Figure 5. and Figure 6. in the other modes. |

Reset Value = 0000 0000b
Bit addressable

### Table 7. Priority Level Bit Values

| IPH.x | IP.x | Interrupt Level Priority |
|---|---|---|
| 0 | 0 | 0 (Lowest) |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 (Highest) |

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can’t be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

### Table 8. IE Register

**IE - Interrupt Enable Register (A8h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **EA** | **-** | **-** | **ES** | **ET1** | **EX1** | **ET0** | **EX0** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | EA | **Enable All interrupt bit**<br>Clear to disable all interrupts.<br>Set to enable all interrupts.<br>If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | ES | **Serial port Enable bit**<br>Clear to disable serial port interrupt.<br>Set to enable serial port interrupt. |
| 3 | ET1 | **Timer 1 overflow interrupt Enable bit**<br>Clear to disable timer 1 overflow interrupt.<br>Set to enable timer 1 overflow interrupt. |
| 2 | EX1 | **External interrupt 1 Enable bit**<br>Clear to disable external interrupt 1.<br>Set to enable external interrupt 1. |
| 1 | ET0 | **Timer 0 overflow interrupt Enable bit**<br>Clear to disable timer 0 overflow interrupt.<br>Set to enable timer 0 overflow interrupt. |
| 0 | EX0 | **External interrupt 0 Enable bit**<br>Clear to disable external interrupt 0.<br>Set to enable external interrupt 0. |

Reset Value = 0XX0 0000b
Bit addressable

### Table 9. IP Register

## 6.7 ONCE$^{TM}$ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C31X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C31X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C31X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 12. External Pin Status during ONCE Mode**

| ALE | $\overline{\text{PSEN}}$ | Port 0 | Port 1 | Port 2 | Port 3 | XTAL1/2 |
|---|---|---|---|---|---|---|
| Weak pull-up | Weak pull-up | Float | Weak pull-up | Weak pull-up | Weak pull-up | Active |

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings (1)

| | |
|---|---|
| Ambiant Temperature Under Bias: | |
| C = commercial | 0°C to 70°C |
| I = industrial | -40°C to 85°C |
| Storage Temperature | -65°C to + 150°C |
| Voltage on $V_{CC}$ to $V_{SS}$ | -0.5 V to + 7 V |
| Voltage on $V_{PP}$ to $V_{SS}$ | -0.5 V to + 13 V |
| Voltage on Any Pin to $V_{SS}$ | -0.5 V to $V_{CC}$ + 0.5 V |
| Power Dissipation | 1 W(2) |

*NOTES*

1. *Stresses at or above those listed under “ Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*
2. *This value is based on the maximum allowable die temperature and the thermal resistance of the package.*

## 7.2 Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That’s why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

```
Label:    SJMP Label (80 FE)
```

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

## 7.3 DC Parameters for Standard Voltage

$T_A$ = 0°C to +70°C; $V_{SS}$ = 0 V; $V_{CC}$ = 5 V ± 10%; F = 0 to 40 MHz.
$T_A$ = -40°C to +85°C; $V_{SS}$ = 0 V; $V_{CC}$ = 5 V ± 10%; F = 0 to 40 MHz.

**Table 14. DC Parameters in Standard Voltage**

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 (6) | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 μA(4)<br>$I_{OL}$ = 1.6 mA(4)<br>$I_{OL}$ = 3.5 mA(4) |
| $V_{OL1}$ | Output Low Voltage, port 0 (6) | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 200 μA(4)<br>$I_{OL}$ = 3.2 mA(4)<br>$I_{OL}$ = 7.0 mA(4) |
| $V_{OL2}$ | Output Low Voltage, ALE, $\overline{\text{PSEN}}$ | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 μA(4)<br>$I_{OL}$ = 1.6 mA(4)<br>$I_{OL}$ = 3.5 mA(4) |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -10 μA<br>$I_{OH}$ = -30 μA<br>$I_{OH}$ = -60 μA<br>$V_{CC}$ = 5 V ± 10% |
| $V_{OH1}$ | Output High Voltage, port 0 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -200 μA<br>$I_{OH}$ = -3.2 mA<br>$I_{OH}$ = -7.0 mA<br>$V_{CC}$ = 5 V ± 10% |
| $V_{OH2}$ | Output High Voltage,ALE, $\overline{\text{PSEN}}$ | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -100 μA<br>$I_{OH}$ = -1.6 mA<br>$I_{OH}$ = -3.5 mA<br>$V_{CC}$ = 5 V ± 10% |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | | -50 | μA | Vin = 0.45 V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | μA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | | -650 | μA | Vin = 2.0 V |
| $C_{IO}$ | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power Down Current | | 20 (5) | 50 | μA | 2.0 V < $V_{CC}$ < 5.5 V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.4 Freq (MHz)<br>@12MHz 5.8<br>@16MHz 7.4 | mA | $V_{CC}$ = 5.5 V(1) |

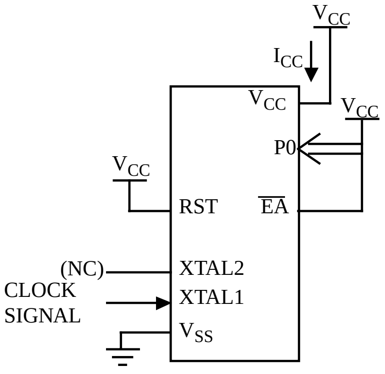
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{CC}$<br>idle | Power Supply Current Maximum values, X1 mode: (7) | | | 0.15 Freq (MHz) + 0.2<br>@12MHz 2<br>@16MHz 2.6 | mA | $V_{CC}$ = 3.3 V(2) |

*NOTES*

1. *$I_{CC}$ under reset is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 13.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ would be slightly higher if a crystal oscillator used..*
2. *Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$ (see Figure 11.).*
3. *Power Down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = $V_{SS}$, PORT 0 = $V_{CC}$; XTAL2 NC.; RST = $V_{SS}$ (see Figure 12.).*
4. *Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi $V_{OL}$ peak 0.6V. A Schmitt Trigger use is not necessary.*
5. *Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.*
6. *Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:*
   *Maximum $I_{OL}$ per port pin: 10 mA*
   *Maximum $I_{OL}$ per 8-bit port:*
   *Port 0: 26 mA*
   *Ports 1, 2 and 3: 15 mA*
   *Maximum total $I_{OL}$ for all output pins: 71 mA*

*If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.*

7. *For other values, please contact your sales office.*
8. *Operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 13.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = $V_{CC}$; RST = $V_{SS}$. The internal ROM runs the code 80 FE (label: SJMP label). $I_{CC}$ would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.*



All other pins are disconnected.

**Figure 9. $I_{CC}$ Test Condition, under reset**

### 7.5.4 External Data Memory Characteristics

**Table 21. Symbol Description**

| Symbol | Parameter |
|---|---|
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width |
| $T_{RLDV}$ | $\overline{RD}$ to Valid Data In |
| $T_{RHDX}$ | Data Hold After $\overline{RD}$ |
| $T_{RHDZ}$ | Data Float After $\overline{RD}$ |
| $T_{LLDV}$ | ALE to Valid Data In |
| $T_{AVDV}$ | Address to Valid Data In |
| $T_{LLWL}$ | ALE to $\overline{WR}$ or $\overline{RD}$ |
| $T_{AVWL}$ | Address to $\overline{WR}$ or $\overline{RD}$ |
| $T_{QVWX}$ | Data Valid to $\overline{WR}$ Transition |
| $T_{QVWH}$ | Data set-up to $\overline{WR}$ High |
| $T_{WHQX}$ | Data Hold After $\overline{WR}$ |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float |
| $T_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE high |

### 7.5.6 External Data Memory Read Cycle

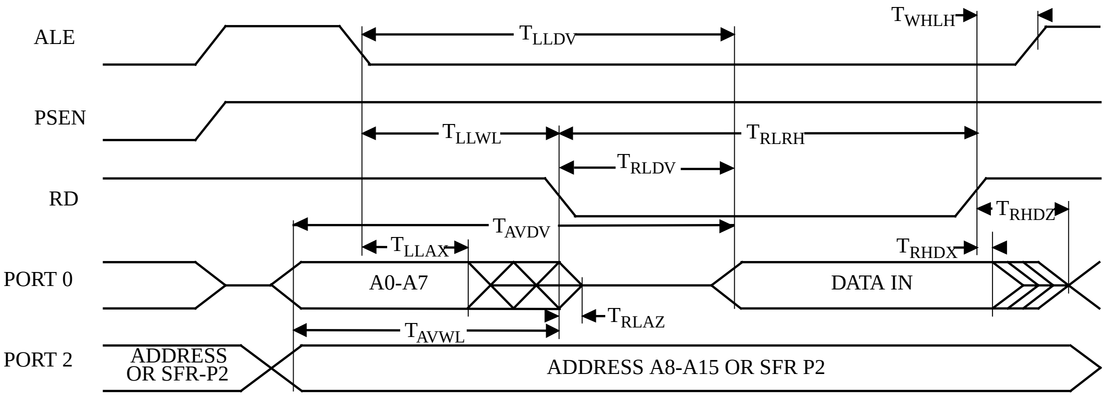


**Figure 16. External Data Memory Read Cycle**

### 7.5.7 Serial Port Timing - Shift Register Mode

**Table 24. Symbol Description**

| Symbol | Parameter |
|---|---|
| $T_{XLXL}$ | Serial port clock cycle time |
| $T_{QVHX}$ | Output data set-up to clock rising edge |
| $T_{XHQX}$ | Output data hold after clock rising edge |
| $T_{XHDX}$ | Input data hold after clock rising edge |
| $T_{XHDV}$ | Clock rising edge to input data valid |

**Table 25. AC Parameters for a Fix Clock**

| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $T_{XLXL}$ | 300 | | 200 | | 300 | | 300 | | 400 | | ns |
| $T_{QVHX}$ | 200 | | 117 | | 200 | | 200 | | 283 | | ns |
| $T_{XHQX}$ | 30 | | 13 | | 30 | | 30 | | 47 | | ns |
| $T_{XHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{XHDV}$ | | 117 | | 34 | | 117 | | 117 | | 200 | ns |

**Table 26. AC Parameters for a Variable Clock: derating formula**

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{XLXL}$ | Min | 12 T | 6 T | | | | ns |
| $T_{QVHX}$ | Min | 10 T - x | 5 T - x | 50 | 50 | 50 | ns |
| $T_{XHQX}$ | Min | 2 T - x | T - x | 20 | 20 | 20 | ns |
| $T_{XHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{XHDV}$ | Max | 10 T - x | 5 T- x | 133 | 133 | 133 | ns |

### 7.5.8 Shift Register Timing Waveforms

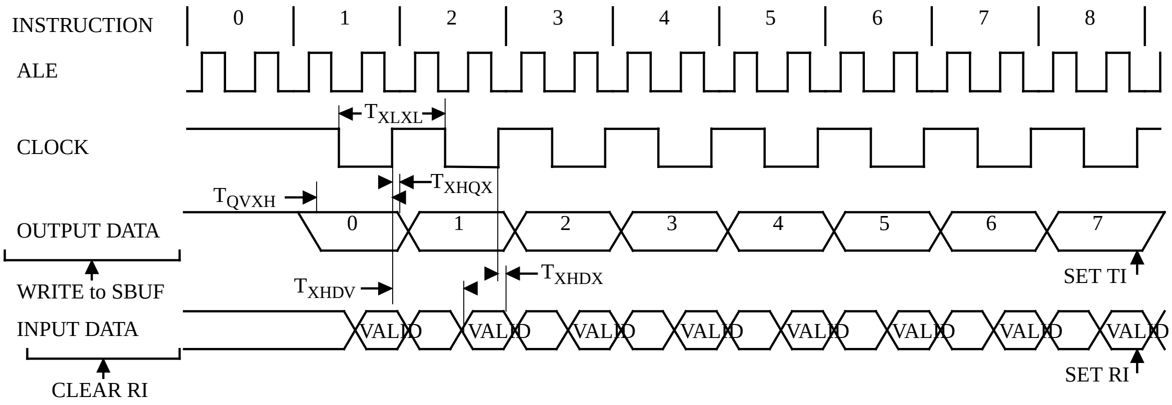


Figure 17. Shift Register Timing Waveforms

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} \geq \pm$ 20mA.

### 7.5.13 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

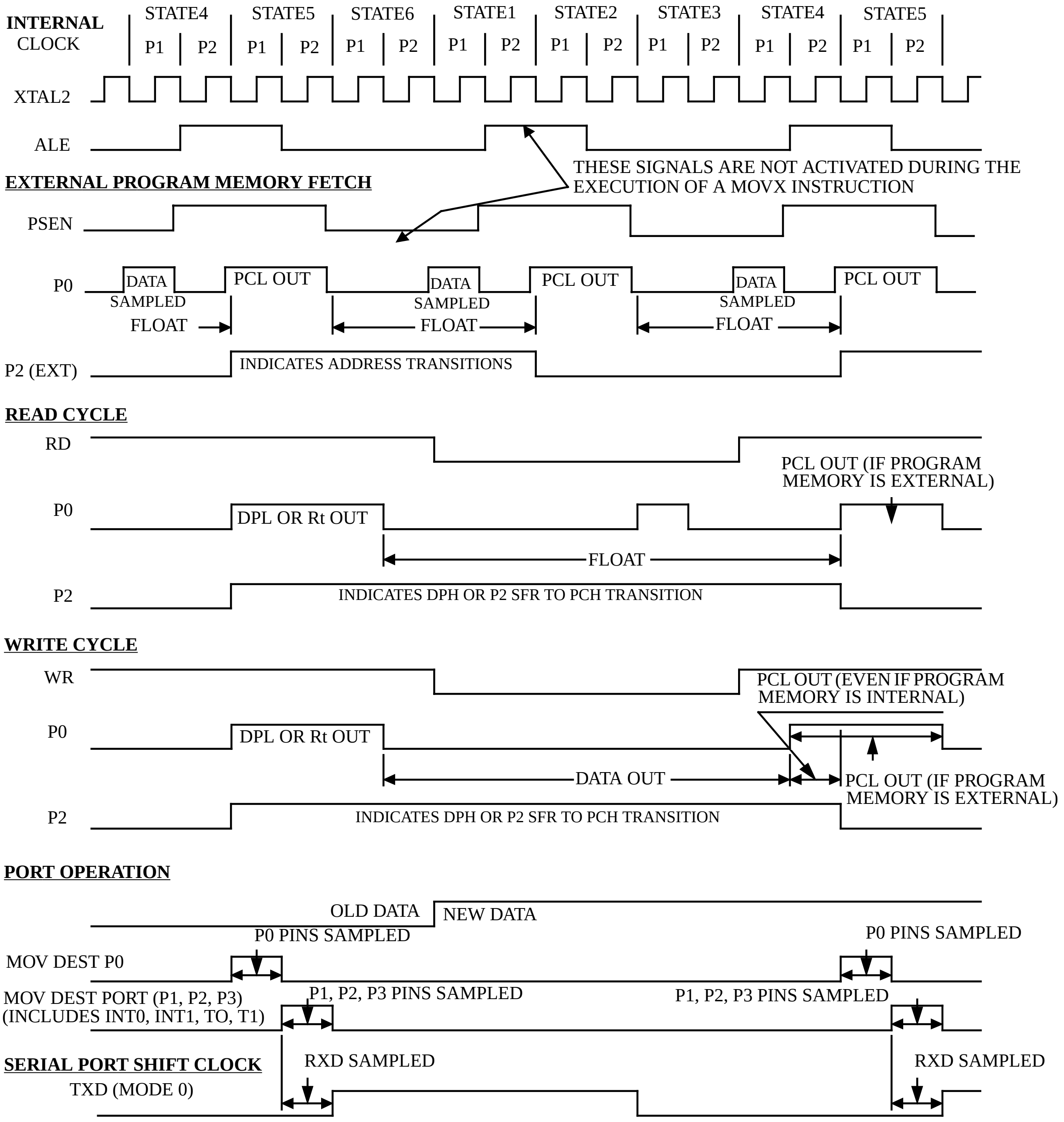
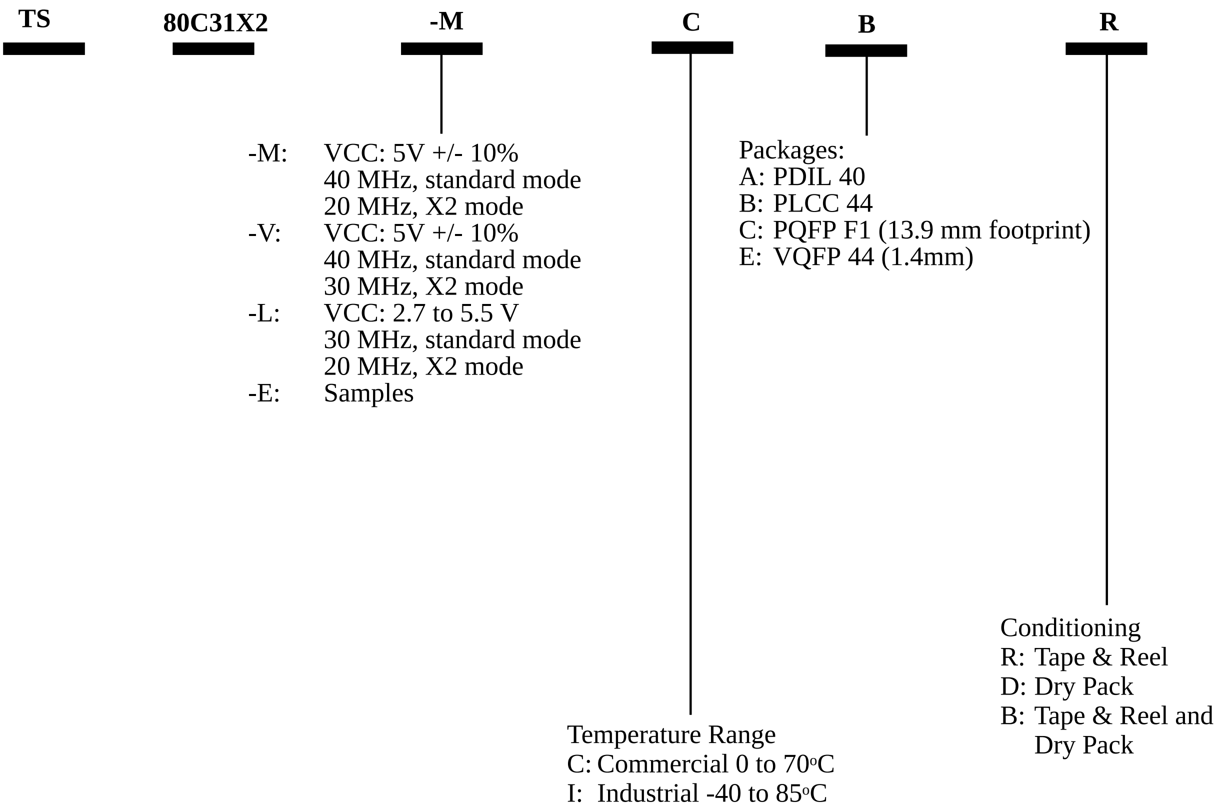


**Figure 21. Clock Waveforms**

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A$=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

## 8. Ordering Information



-M: VCC: 5V +/- 10%
40 MHz, standard mode
20 MHz, X2 mode
-V: VCC: 5V +/- 10%
40 MHz, standard mode
30 MHz, X2 mode
-L: VCC: 2.7 to 5.5 V
30 MHz, standard mode
20 MHz, X2 mode
-E: Samples

Packages:
A: PDIL 40
B: PLCC 44
C: PQFP F1 (13.9 mm footprint)
E: VQFP 44 (1.4mm)

Conditioning
R: Tape & Reel
D: Dry Pack
B: Tape & Reel and Dry Pack

Temperature Range
C: Commercial 0 to 70°C
I: Industrial -40 to 85°C

**Table 28. Maximum Clock Frequency**

| Code | -M | -V | -L | Unit |
|---|---|---|---|---|
| Standard Mode, oscillator frequency<br>Standard Mode, internal frequency | 40<br>40 | 40<br>40 | 30<br>30 | MHz |
| X2 Mode, oscillator frequency<br>X2 Mode, internal equivalent frequency | 20<br>40 | 30<br>**60** | 20<br>**40** | MHz |

**Table 29. Possible Ordering Entries**

| | TS80C31X2 ROMless |
|---|---|
| -MCA | X |
| -MCB | X |
| -MCC | X |
| -MCE | X |
| -VCA | X |
| -VCB | X |
| -VCC | X |
| -VCE | X |
| -LCA | X |
| -LCB | X |
| -LCC | X |
| -LCE | X |
| -MIA | X |
| -MIB | X |
| -MIC | X |
| -MIE | X |
| -VIA | X |
| -VIB | X |
| -VIC | X |
| -VIE | X |
| -LIA | X |
| -LIB | X |
| -LIC | X |
| -LIE | X |
| -EA | X |
| -EB | X |
| -EC | X |
| -EE | X |

- -Ex for samples
- Tape and Reel available for B, C and E packages
- Dry pack mandatory for E packages