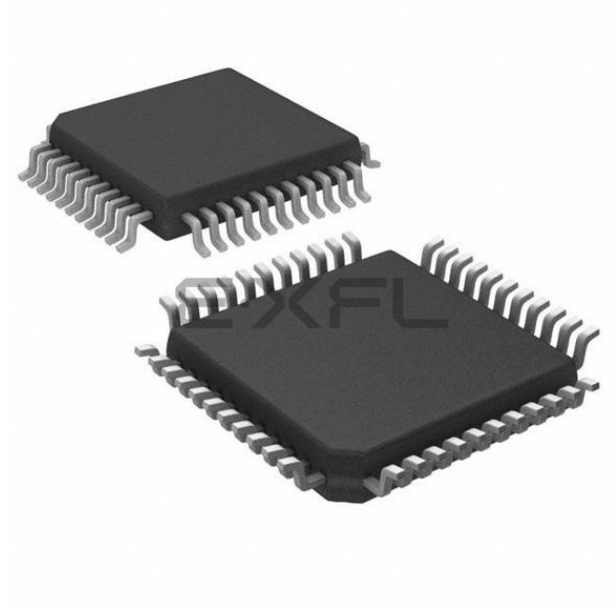

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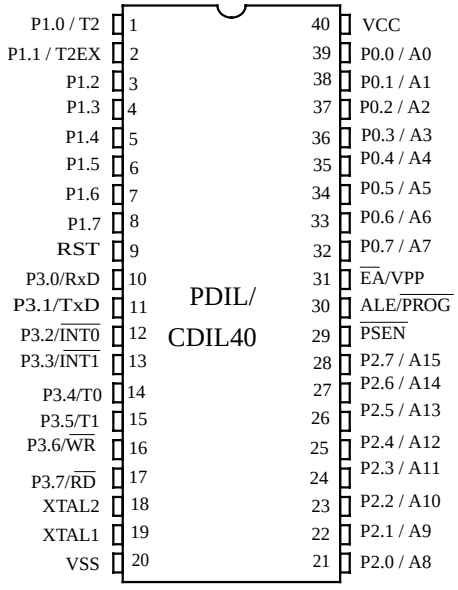
## What is "Embedded - Microcontrollers"?

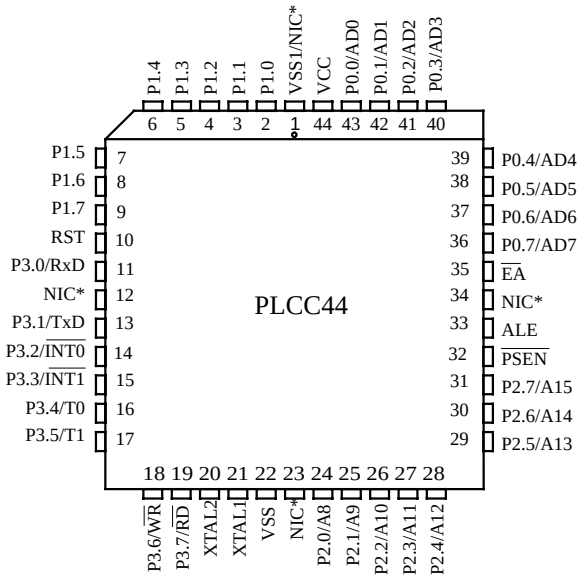
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

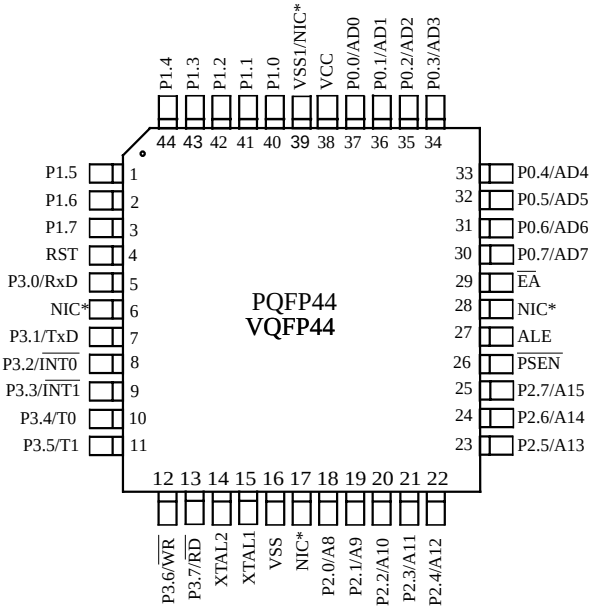
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 40/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-QFP |
| Supplier Device Package | 44-VQFP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts80c31x2-mce |

## 5. Pin Configuration




*NIC: No Internal Connection

**Table 2. Pin Description for 40/44 pin packages**

| MNEMONIC | PIN NUMBER | | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|
| | DIL | LCC | VQFP 1.4 | | |
| $V_{SS}$ | 20 | 22 | 16 | I | **Ground:** 0V reference |
| Vss1 | | 1 | 39 | I | **Optional Ground:** Contact the Sales Office for ground connection. |
| $V_{CC}$ | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for normal, idle and power-down operation |
| P0.0-P0.7 | 39-32 | 43-36 | 37-30 | I/O | **Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. |
| P1.0-P1.7 | 1-8 | 2-9 | 40-44<br>1-3 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. |
| P2.0-P2.7 | 21-28 | 24-31 | 18-25 | I/O | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. |
| P3.0-P3.7 | 10-17 | 11,<br>13-19 | 5,<br>7-13 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below. |
| | 10 | 11 | 5 | I | **RXD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TXD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{INT0}$ (P3.2):** External interrupt 0 |
| | 13 | 15 | 9 | I | **$\overline{INT1}$ (P3.3):** External interrupt 1 |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input |
| | 16 | 18 | 12 | O | **$\overline{WR}$ (P3.6):** External data memory write strobe |
| | 17 | 19 | 13 | O | **$\overline{RD}$ (P3.7):** External data memory read strobe |
| Reset | 9 | 10 | 4 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC.}$ |
| ALE | 30 | 33 | 27 | O (I) | **Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. |
| $\overline{PSEN}$ | 29 | 32 | 26 | O | **Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. |
| $\overline{EA}$ | 31 | 35 | 29 | I | **External Access Enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations. |
| XTAL1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier |

# 6. TS80C31X2 Enhanced Features

In comparison to the original 80C31, the TS80C31X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- Enhanced UART

## 6.1 X2 Feature

The TS80C31X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.

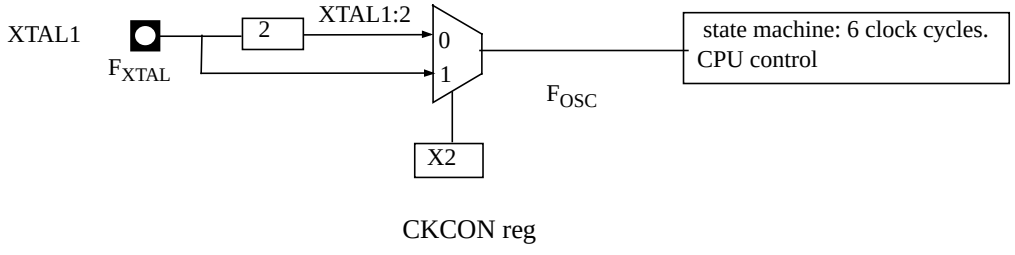



**Figure 1. Clock Generation Diagram**

**Table 3. CKCON Register**

**CKCON - Clock Control Register (8Fh)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | X2 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 0 | X2 | **CPU and peripheral clock bit**<br>Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$).<br>Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$). |

Reset Value = XXXX XXX0b
Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)

### 6.3.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

**SADEN - Slave Address Mask Register (B9h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Reset Value = 0000 0000b
Not bit addressable

**SADDR - Slave Address Register (A9h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Reset Value = 0000 0000b
Not bit addressable

**Table 5. SCON Register**

**SCON - Serial Control Register (98h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **FE/SM0** | **SM1** | **SM2** | **REN** | **TB8** | **RB8** | **TI** | **RI** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | FE | **Framing Error bit (SMOD0=1)**<br>Clear to reset the error state, not cleared by a valid stop bit.<br>Set by hardware when an invalid stop bit is detected.<br>SMOD0 must be set to enable access to the FE bit |
| | SM0 | **Serial port Mode bit 0**<br>Refer to SM1 for serial port mode selection.<br>SMOD0 must be cleared to enable access to the SM0 bit |
| 6 | SM1 | **Serial port Mode bit 1**<br>SM0 SM1 Mode Description Baud Rate<br>0 0 0 Shift Register $F_{XTAL}$/12 (/6 in X2 mode)<br>0 1 1 8-bit UART Variable<br>1 0 2 9-bit UART $F_{XTAL}$/64 or $F_{XTAL}$/32 (/32, /16 in X2 mode)<br>1 1 3 9-bit UART Variable |
| 5 | SM2 | **Serial port Mode 2 bit / Multiprocessor Communication Enable bit**<br>Clear to disable multiprocessor communication feature.<br>Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0. |
| 4 | REN | **Reception Enable bit**<br>Clear to disable serial reception.<br>Set to enable serial reception. |
| 3 | TB8 | **Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.**<br>Clear to transmit a logic 0 in the 9th bit.<br>Set to transmit a logic 1 in the 9th bit. |
| 2 | RB8 | **Receiver Bit 8 / Ninth bit received in modes 2 and 3**<br>Cleared by hardware if 9th bit received is a logic 0.<br>Set by hardware if 9th bit received is a logic 1.<br>In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used. |
| 1 | TI | **Transmit Interrupt flag**<br>Clear to acknowledge interrupt.<br>Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes. |
| 0 | RI | **Receive Interrupt flag**<br>Clear to acknowledge interrupt.<br>Set by hardware at the end of the 8th bit time in mode 0, see Figure 5. and Figure 6. in the other modes. |

Reset Value = 0000 0000b
Bit addressable

**IP - Interrupt Priority Register (B8h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | PS | PT1 | PX1 | PT0 | PX0 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | PS | **Serial port Priority bit**<br>Refer to PSH for priority level. |
| 3 | PT1 | **Timer 1 overflow interrupt Priority bit**<br>Refer to PT1H for priority level. |
| 2 | PX1 | **External interrupt 1 Priority bit**<br>Refer to PX1H for priority level. |
| 1 | PT0 | **Timer 0 overflow interrupt Priority bit**<br>Refer to PT0H for priority level. |
| 0 | PX0 | **External interrupt 0 Priority bit**<br>Refer to PX0H for priority level. |

Reset Value = XXX0 0000b
Bit addressable

**Table 10. IPH Register**

**IPH - Interrupt Priority High Register (B7h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | PSH | PT1H | PX1H | PT0H | PX0H |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | PSH | **Serial port Priority High bit**<br>PSH PS Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 3 | PT1H | **Timer 1 overflow interrupt Priority High bit**<br>PT1H PT1 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 2 | PX1H | **External interrupt 1 Priority High bit**<br>PX1H PX1 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 1 | PT0H | **Timer 0 overflow interrupt Priority High bit**<br>PT0H PT0 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 0 | PX0H | **External interrupt 0 Priority High bit**<br>PX0H PX0 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |

Reset Value = XXX0 0000b
Not bit addressable

## 6.5 Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give and indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The over way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

## 6.6 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 6., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. $V_{CC}$ can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before $V_{CC}$ is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 8. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C31X2 into power-down mode.

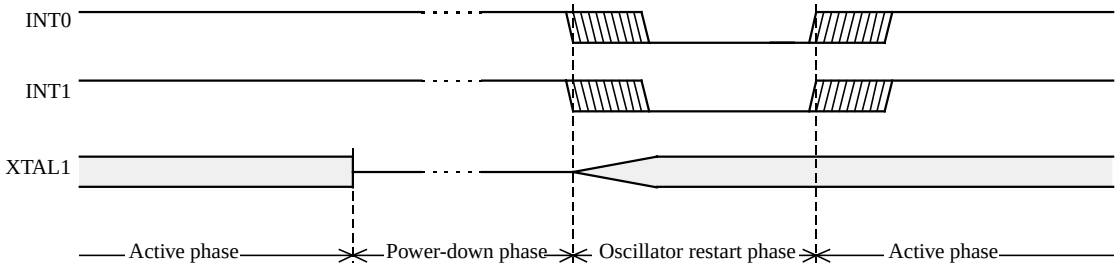



**Figure 8. Power-Down Exit Waveform**

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.
*NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.*

**Table 11. The state of ports during idle and power-down modes**

| Mode | Program Memory | ALE | $\overline{PSEN}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | External | 1 | 1 | Floating | Port Data | Address | Port Data |
| Power Down | External | 0 | 0 | Floating | Port Data | Port Data | Port Data |

## 6.8 Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by $V_{CC}$ switch-on. A warm start reset occurs while $V_{CC}$ is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 13.). POF is set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

**Table 13. PCON Register**

**PCON - Power Control Register (87h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SMOD1** | **SMOD0** | **-** | **POF** | **GF1** | **GF0** | **PD** | **IDL** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | SMOD1 | **Serial port Mode bit 1**<br>Set to select double baud rate in mode 1, 2 or 3. |
| 6 | SMOD0 | **Serial port Mode bit 0**<br>Clear to select SM0 bit in SCON register.<br>Set to to select FE bit in SCON register. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | POF | **Power-Off Flag**<br>Clear to recognize next reset type.<br>Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software. |
| 3 | GF1 | **General purpose Flag**<br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage. |
| 2 | GF0 | **General purpose Flag**<br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage. |
| 1 | PD | **Power-Down mode bit**<br>Cleared by hardware when reset occurs.<br>Set to enter power-down mode. |
| 0 | IDL | **Idle mode bit**<br>Clear by hardware when interrupt or reset occurs.<br>Set to enter idle mode. |

Reset Value = 00X1 0000b
Not bit addressable

## 7.3 DC Parameters for Standard Voltage

$T_A$ = 0°C to +70°C; $V_{SS}$ = 0 V; $V_{CC}$ = 5 V ± 10%; F = 0 to 40 MHz.
$T_A$ = -40°C to +85°C; $V_{SS}$ = 0 V; $V_{CC}$ = 5 V ± 10%; F = 0 to 40 MHz.

**Table 14. DC Parameters in Standard Voltage**

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 (6) | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 µA(4)<br>$I_{OL}$ = 1.6 mA(4)<br>$I_{OL}$ = 3.5 mA(4) |
| $V_{OL1}$ | Output Low Voltage, port 0 (6) | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 200 µA(4)<br>$I_{OL}$ = 3.2 mA(4)<br>$I_{OL}$ = 7.0 mA(4) |
| $V_{OL2}$ | Output Low Voltage, ALE, $\overline{PSEN}$ | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 µA(4)<br>$I_{OL}$ = 1.6 mA(4)<br>$I_{OL}$ = 3.5 mA(4) |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -10 µA<br>$I_{OH}$ = -30 µA<br>$I_{OH}$ = -60 µA<br>$V_{CC}$ = 5 V ± 10% |
| $V_{OH1}$ | Output High Voltage, port 0 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -200 µA<br>$I_{OH}$ = -3.2 mA<br>$I_{OH}$ = -7.0 mA<br>$V_{CC}$ = 5 V ± 10% |
| $V_{OH2}$ | Output High Voltage,ALE, $\overline{PSEN}$ | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -100 µA<br>$I_{OH}$ = -1.6 mA<br>$I_{OH}$ = -3.5 mA<br>$V_{CC}$ = 5 V ± 10% |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | | -50 | µA | Vin = 0.45 V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | | -650 | µA | Vin = 2.0 V |
| $C_{IO}$ | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power Down Current | | 20 (5) | 50 | µA | 2.0 V < $V_{CC}$ < 5.5 V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.4 Freq (MHz)<br>@12MHz 5.8<br>@16MHz 7.4 | mA | $V_{CC}$ = 5.5 V(1) |

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{CC}$ operating | Power Supply Current Maximum values, X1 mode: (7) | | | 3 + 0.6 Freq (MHz)<br>@12MHz 10.2<br>@16MHz 12.6 | mA | $V_{CC}$ = 5.5 V(8) |
| $I_{CC}$ idle | Power Supply Current Maximum values, X1 mode: (7) | | | 0.25+0.3Freq (MHz)<br>@12MHz 3.9<br>@16MHz 5.1 | mA | $V_{CC}$ = 5.5 V(2) |

## 7.4 DC Parameters for Low Voltage

$T_A$ = 0°C to +70°C; $V_{SS}$ = 0 V; $V_{CC}$ = 2.7 V to 5.5 V ± 10%; F = 0 to 30 MHz.
$T_A$ = -40°C to +85°C; $V_{SS}$ = 0 V; $V_{CC}$ = 2.7 V to 5.5 V ± 10%; F = 0 to 30 MHz.

**Table 15. DC Parameters for Low Voltage**

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 (6) | | | 0.45 | V | $I_{OL}$ = 0.8 mA(4) |
| $V_{OL1}$ | Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6) | | | 0.45 | V | $I_{OL}$ = 1.6 mA(4) |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | 0.9 $V_{CC}$ | | | V | $I_{OH}$ = -10 µA |
| $V_{OH1}$ | Output High Voltage, port 0, ALE, $\overline{PSEN}$ | 0.9 $V_{CC}$ | | | V | $I_{OH}$ = -40 µA |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | | -50 | µA | Vin = 0.45 V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | | -650 | µA | Vin = 2.0 V |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| CIO | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power Down Current | | 20 (5)<br>10 (5) | 50<br>30 | µA | $V_{CC}$ = 2.0 V to 5.5 V(3)<br>$V_{CC}$ = 2.0 V to 3.3 V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.2 Freq (MHz)<br>@12MHz 3.4<br>@16MHz 4.2 | mA | $V_{CC}$ = 3.3 V(1) |
| $I_{CC}$ operating | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.3 Freq (MHz)<br>@12MHz 4.6<br>@16MHz 5.8 | mA | $V_{CC}$ = 3.3 V(8) |

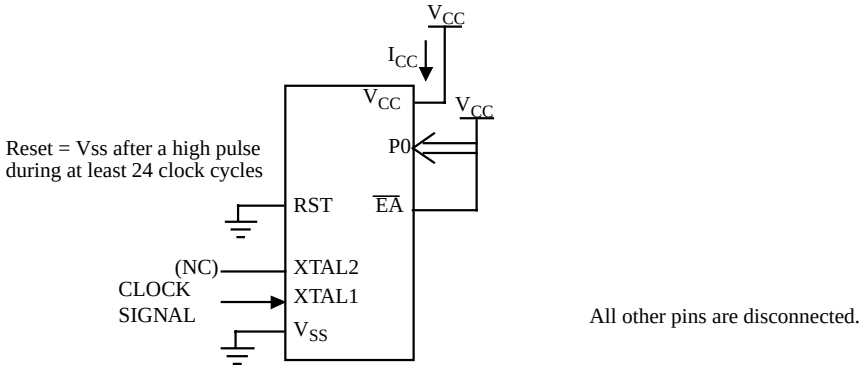



**Figure 10. Operating $I_{CC}$ Test Condition**

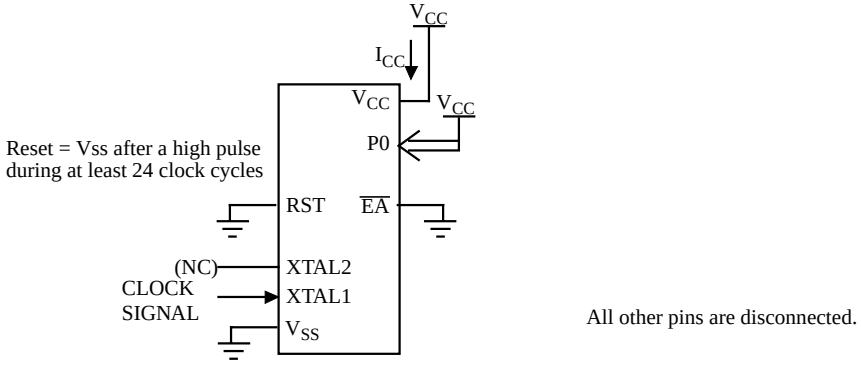



**Figure 11. $I_{CC}$ Test Condition, Idle Mode**

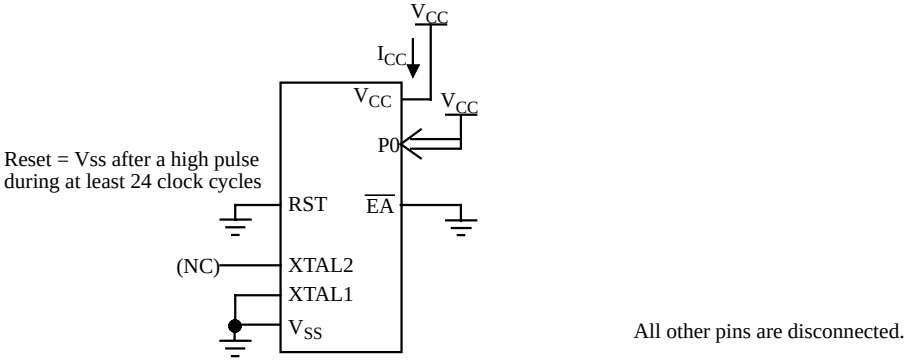



**Figure 12. $I_{CC}$ Test Condition, Power-Down Mode**

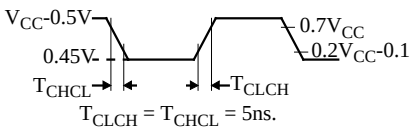



**Figure 13. Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes**

**Table 20. AC Parameters for a Variable Clock: derating formula**

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{LHLL}$ | Min | 2 T - x | T - x | 10 | 8 | 15 | ns |
| $T_{AVLL}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLAX}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLIV}$ | Max | 4 T - x | 2 T - x | 30 | 22 | 35 | ns |
| $T_{LLPL}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{PLPH}$ | Min | 3 T - x | 1.5 T - x | 20 | 15 | 25 | ns |
| $T_{PLIV}$ | Max | 3 T - x | 1.5 T - x | 40 | 25 | 45 | ns |
| $T_{PXIX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{PXIZ}$ | Max | T - x | 0.5 T - x | 7 | 5 | 15 | ns |
| $T_{AVIV}$ | Max | 5 T - x | 2.5 T - x | 40 | 30 | 45 | ns |
| $T_{PLAZ}$ | Max | x | x | 10 | 10 | 10 | ns |

### 7.5.3 External Program Memory Read Cycle

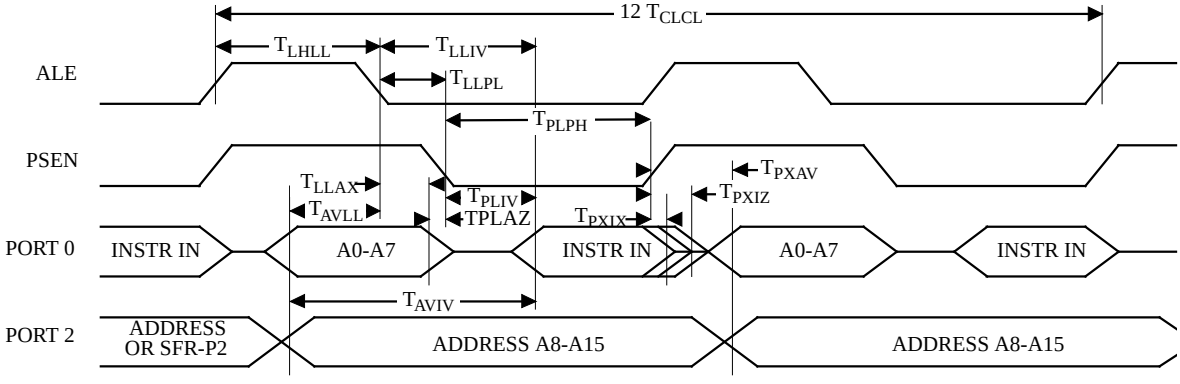



**Figure 14. External Program Memory Read Cycle**

**Table 22. AC Parameters for a Fix Clock**

| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $T_{RLRH}$ | 130 | | 85 | | 135 | | 125 | | 175 | | ns |
| $T_{WLWH}$ | 130 | | 85 | | 135 | | 125 | | 175 | | ns |
| $T_{RLDV}$ | | 100 | | 60 | | 102 | | 95 | | 137 | ns |
| $T_{RHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{RHDZ}$ | | 30 | | 18 | | 35 | | 25 | | 42 | ns |
| $T_{LLDV}$ | | 160 | | 98 | | 165 | | 155 | | 222 | ns |
| $T_{AVDV}$ | | 165 | | 100 | | 175 | | 160 | | 235 | ns |
| $T_{LLWL}$ | 50 | 100 | 30 | 70 | 55 | 95 | 45 | 105 | 70 | 130 | ns |
| $T_{AVWL}$ | 75 | | 47 | | 80 | | 70 | | 103 | | ns |
| $T_{QVWX}$ | 10 | | 7 | | 15 | | 5 | | 13 | | ns |
| $T_{QVWH}$ | 160 | | 107 | | 165 | | 155 | | 213 | | ns |
| $T_{WHQX}$ | 15 | | 9 | | 17 | | 10 | | 18 | | ns |
| $T_{RLAZ}$ | | 0 | | 0 | | 0 | | 0 | | 0 | ns |
| $T_{WHLH}$ | 10 | 40 | 7 | 27 | 15 | 35 | 5 | 45 | 13 | 53 | ns |

**Table 23. AC Parameters for a Variable Clock: derating formula**

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{RLRH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{WLWH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{RLDV}$ | Max | 5 T - x | 2.5 T - x | 25 | 23 | 30 | ns |
| $T_{RHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{RHDZ}$ | Max | 2 T - x | T - x | 20 | 15 | 25 | ns |
| $T_{LLDV}$ | Max | 8 T - x | 4T -x | 40 | 35 | 45 | ns |
| $T_{AVDV}$ | Max | 9 T - x | 4.5 T - x | 60 | 50 | 65 | ns |
| $T_{LLWL}$ | Min | 3 T - x | 1.5 T - x | 25 | 20 | 30 | ns |
| $T_{LLWL}$ | Max | 3 T + x | 1.5 T + x | 25 | 20 | 30 | ns |
| $T_{AVWL}$ | Min | 4 T - x | 2 T - x | 25 | 20 | 30 | ns |
| $T_{QVWX}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{QVWH}$ | Min | 7 T - x | 3.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHQX}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{RLAZ}$ | Max | x | x | 0 | 0 | 0 | ns |
| $T_{WHLH}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHLH}$ | Max | T + x | 0.5 T + x | 15 | 10 | 20 | ns |

### 7.5.5 External Data Memory Write Cycle

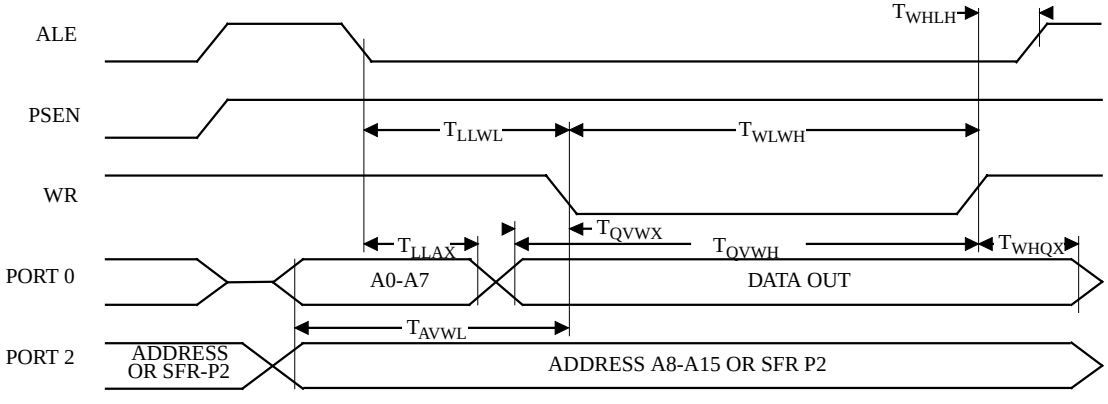



**Figure 15. External Data Memory Write Cycle**

### 7.5.6 External Data Memory Read Cycle

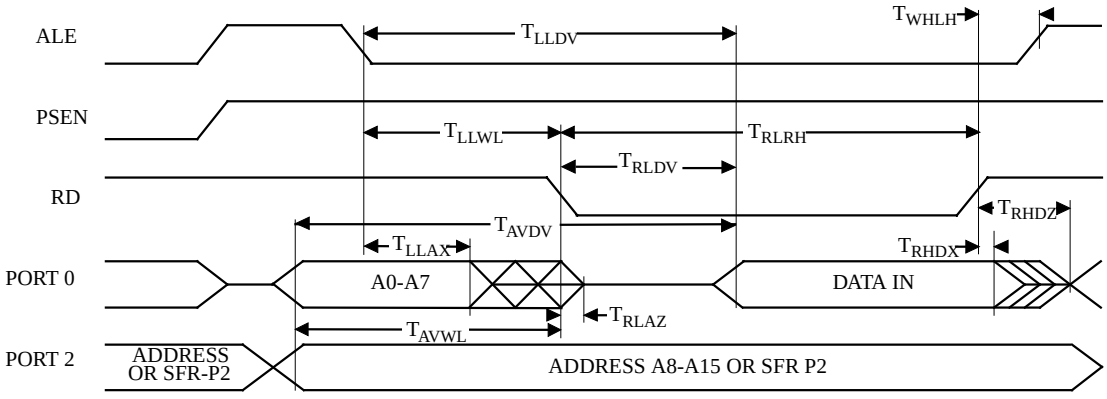



**Figure 16. External Data Memory Read Cycle**

### 7.5.7 Serial Port Timing - Shift Register Mode

**Table 24. Symbol Description**

| Symbol | Parameter |
|---|---|
| $T_{XLXL}$ | Serial port clock cycle time |
| $T_{QVHX}$ | Output data set-up to clock rising edge |
| $T_{XHQX}$ | Output data hold after clock rising edge |
| $T_{XHDX}$ | Input data hold after clock rising edge |
| $T_{XHDV}$ | Clock rising edge to input data valid |

**Table 25. AC Parameters for a Fix Clock**

| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $T_{XLXL}$ | 300 | | 200 | | 300 | | 300 | | 400 | | ns |
| $T_{QVHX}$ | 200 | | 117 | | 200 | | 200 | | 283 | | ns |
| $T_{XHQX}$ | 30 | | 13 | | 30 | | 30 | | 47 | | ns |
| $T_{XHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{XHDV}$ | | 117 | | 34 | | 117 | | 117 | | 200 | ns |

**Table 26. AC Parameters for a Variable Clock: derating formula**

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{XLXL}$ | Min | 12 T | 6 T | | | | ns |
| $T_{QVHX}$ | Min | 10 T - x | 5 T - x | 50 | 50 | 50 | ns |
| $T_{XHQX}$ | Min | 2 T - x | T - x | 20 | 20 | 20 | ns |
| $T_{XHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{XHDV}$ | Max | 10 T - x | 5 T- x | 133 | 133 | 133 | ns |

### 7.5.8 Shift Register Timing Waveforms

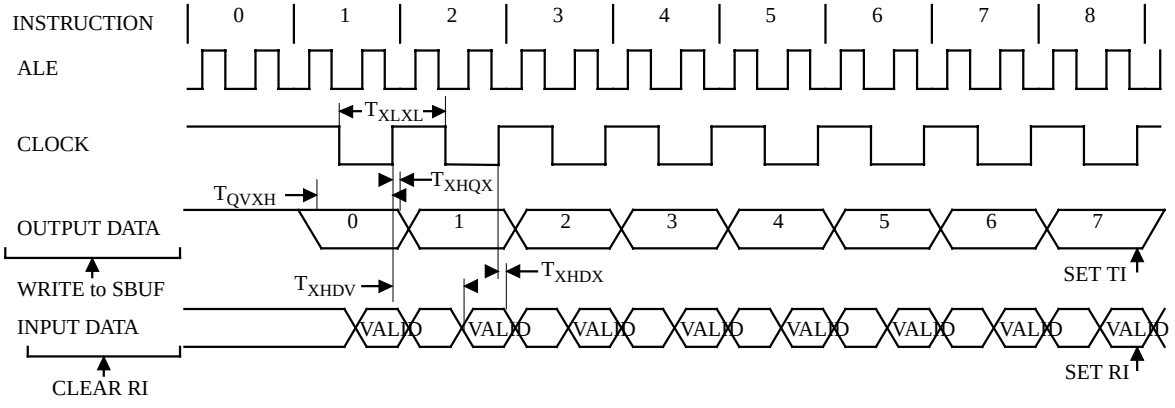



**Figure 17. Shift Register Timing Waveforms**

## 8. Ordering Information

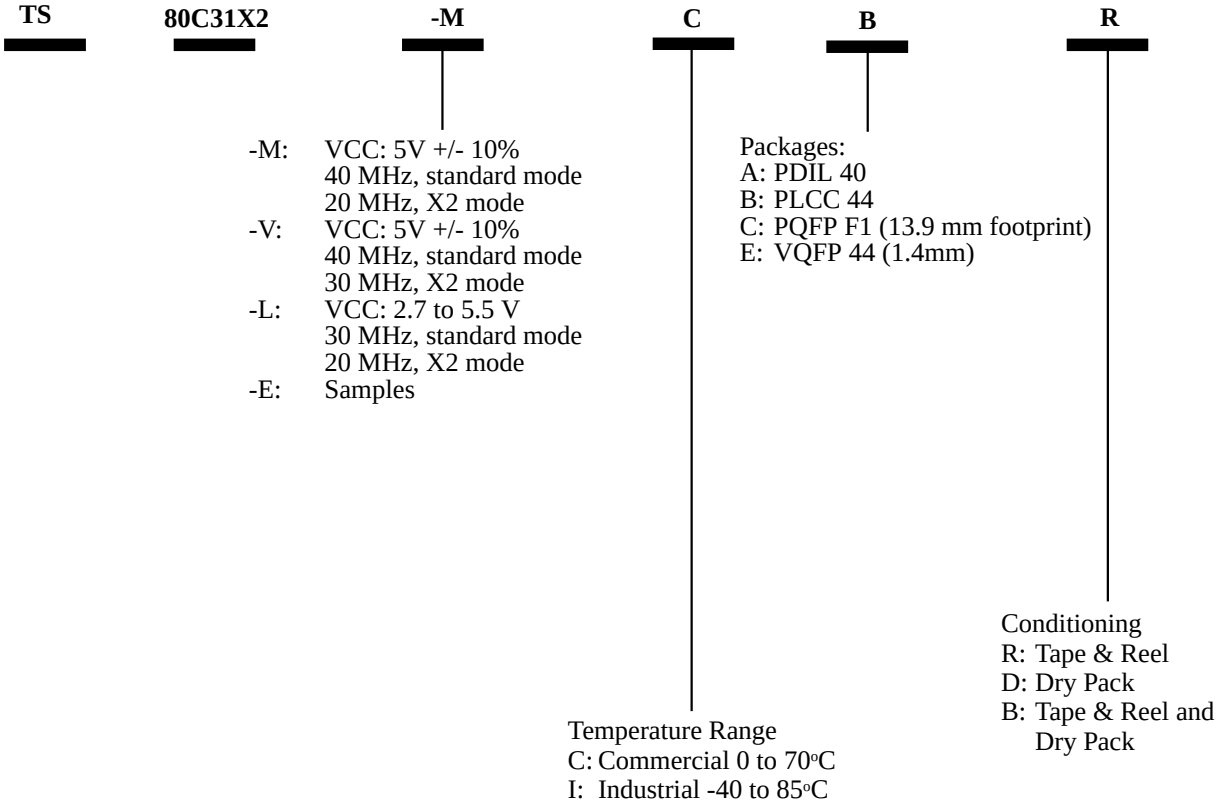



**Table 28. Maximum Clock Frequency**

| Code | -M | -V | -L | Unit |
|---|---|---|---|---|
| Standard Mode, oscillator frequency<br>Standard Mode, internal frequency | 40<br>40 | 40<br>40 | 30<br>30 | MHz |
| X2 Mode, oscillator frequency<br>X2 Mode, internal equivalent frequency | 20<br>40 | 30<br>**60** | 20<br>**40** | MHz |