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#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60/30MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c31x2-vie

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## 3. Block Diagram





## 5. Pin Configuration



\*NIC: No Internal Connection





Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

#### CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.



### Table 3. CKCON Register

#### CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)



### 6.2 Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).



Figure 3. Use of Dual Pointer



### ASSEMBLY LANGUAGE

; Block move using dual data pointers ; Destroys DPTR0, DPTR1, A and PSW ; note: DPS exits opposite of entry state ; unless an extra INC AUXR1 is added

00A2 AUXR1 EQU 0A2H 0000 909000MOV DPTR,#SOURCE : address of SOURCE 0003 05A2 INC AUXR1 ; switch data pointers 0005 90A000 MOV DPTR,#DEST ; address of DEST 0008 LOOP: 0008 05A2 INC AUXR1 ; switch data pointers ; get a byte from SOURCE 000A E0 MOVX A, @DPTR INC DPTR ; increment SOURCE address 000B A3 ; switch data pointers 000C 05A2 INC AUXR1 000E F0 MOVX @DPTR,A ; write the byte to DEST 000F A3 INC DPTR : increment DEST address 0010 70F6 JNZ LOOP ; check for 0 terminator 0012 05A2 INC AUXR1 ; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



#### 6.3.3 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b. For example:

SADDR	0101	0110b
SADEN	1111	1100b
Given	0101	01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR <u>SADEN</u> Given	1111 0001b <u>1111 1010b</u> 1111 0X0Xb
Slave B:	SADDR <u>SADEN</u> Given	1111 0011b <u>1111 1001b</u> 1111 0XX1b
Slave C:	SADDR <u>SADEN</u> Given	1111 0010b <u>1111 1101b</u> 1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

#### 6.3.4 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

0101	0110b
1111	1100b
1111	111Xb
	0101 1111 1111

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR <u>SADEN</u> Broadcast	1111 0001b <u>1111 1010b</u> 1111 1X11b,
Slave B:	SADDR <u>SADEN</u> Broadcast	1111 0011b <u>1111 1001b</u> 1111 1X11B,
Slave C:	SADDR= <u>SADEN</u> Broadcast	1111 0010b <u>1111 1101b</u> 1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.



#### Table 7. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

## Table 8. IE Register

IE - Interrupt Enable Register (A8h)								
7	6	5	4	3	2	1	0	
EA	-	-	ES	ET1	EX1	ЕТО	EX0	

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit           Clear to disable timer 1 overflow interrupt.           Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit         Clear to disable timer 0 overflow interrupt.         Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b Bit addressable



#### IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0		
-	-	-	PS	PT1	PX1	PT0	PX0		
Bit Number	Bit Mnemonic		Description						
7	-	Reserved The value read f	eserved The value read from this bit is indeterminate. Do not set this bit.						
6	-	Reserved The value read f	<b>teserved</b> The value read from this bit is indeterminate. Do not set this bit.						
5	-	Reserved The value read f	Reserved The value read from this bit is indeterminate. Do not set this bit.						
4	PS	Serial port Priority Refer to PSH fo	berial port Priority bit Refer to PSH for priority level.						
3	PT1	Timer 1 overflow in Refer to PT1H f	imer 1 overflow interrupt Priority bit Refer to PT1H for priority level.						
2	PX1	External interrupt Refer to PX1H	External interrupt 1 Priority bit Refer to PX1H for priority level.						
1	PT0	Timer 0 overflow in Refer to PT0H f	Fimer 0 overflow interrupt Priority bit Refer to PTOH for priority level.						
0	PX0	External interrupt Refer to PX0H	<b>0 Priority bit</b> for priority level.						

Reset Value = XXX0 0000b Bit addressable



### 6.5 Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give and indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The over way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

### 6.6 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 6., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 8. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C31X2 into power-down mode.



#### Figure 8. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content. NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.



Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Table 11. The state of ports during idle and power-down modes



Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
I <sub>CC</sub> idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3 V^{(2)}$

NOTES

1.  $I_{CC}$  under reset is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 13.),  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C.;  $\overline{EA} = RST = Port 0 = V_{CC}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator used.

2. Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns,  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C; Port  $0 = V_{CC}$ ;  $\overline{EA} = RST = V_{SS}$  (see Figure 11.).

3. Power Down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{EA} = V_{SS}$ , PORT  $0 = V_{CC}$ ; XTAL2 NC.; RST =  $V_{SS}$  (see Figure 12.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$ s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

6. Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:

Maximum I<sub>OL</sub> per port pin: 10 mA Maximum I<sub>OL</sub> per 8-bit port:

Port 0: 26 mA

Ports 1, 2 and 3: 15 mA Maximum total I<sub>OL</sub> for all output pins: 71 mA

If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions. 7. For other values, please contact your sales office.

8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 13.),  $V_{IL} = V_{SS} + 0.5$  V,

 $V_{IH} = V_{CC} - 0.5V$ ; XTAL2 N.C.;  $\overline{EA} = Port \ 0 = V_{CC}$ ; RST =  $V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 9. I<sub>CC</sub> Test Condition, under reset



### 7.5 AC Parameters

#### 7.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:  $T_{AVLL}$  = Time for Address Valid to ALE Low. T<sub>LLPL</sub> = Time for ALE Low to PSEN Low.

TA = 0 to +70°C (commercial temperature range);  $V_{SS} = 0$  V;  $V_{CC} = 5$  V ± 10%; -M and -V ranges. TA = -40°C to +85°C (industrial temperature range);  $V_{SS} = 0$  V;  $V_{CC} = 5$  V ± 10%; -M and -V ranges. TA = 0 to +70°C (commercial temperature range);  $V_{SS} = 0$  V; 2.7 V <  $V_{CC} < 5.5$  V; -L range. TA = -40°C to +85°C (industrial temperature range);  $V_{SS} = 0$  V; 2.7 V <  $V_{CC} < 5.5$  V; -L range.

Table 16. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and  $\overline{\text{PSEN}}$  signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table	16.	Load	Capacitance	versus	speed	range,	in	pF
					~ ~ ~ ~ ~			

Table 18., Table 21. and Table 24. give the description of each AC symbols.

Table 19., Table 22. and Table 25. give for each range the AC parameter.

Table 20., Table 23. and Table 26. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 17. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

 $T_{LLIV}$  in X2 mode for a -V part at 20 MHz (T =  $1/20^{E6}$  = 50 ns):

x= 25 (Table 20.)

T= 50ns

 $T_{LLIV} = 2T - x = 2 \times 50 - 25 = 75$ ns



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T <sub>LHLL</sub>	Min	2 T - x	T - x	10	8	15	ns
T <sub>AVLL</sub>	Min	T - x	0.5 T - x	15	13	20	ns
T <sub>LLAX</sub>	Min	T - x	0.5 T - x	15	13	20	ns
T <sub>LLIV</sub>	Max	4 T - x	2 T - x	30	22	35	ns
T <sub>LLPL</sub>	Min	T - x	0.5 T - x	10	8	15	ns
T <sub>PLPH</sub>	Min	3 T - x	1.5 T - x	20	15	25	ns
T <sub>PLIV</sub>	Max	3 T - x	1.5 T - x	40	25	45	ns
T <sub>PXIX</sub>	Min	x	х	0	0	0	ns
T <sub>PXIZ</sub>	Max	T - x	0.5 T - x	7	5	15	ns
T <sub>AVIV</sub>	Max	5 T - x	2.5 T - x	40	30	45	ns
T <sub>PLAZ</sub>	Max	x	x	10	10	10	ns

Table 20. AC Parameter	s for	a Variable	Clock:	derating	formula
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## 7.5.3 External Program Memory Read Cycle



Figure 14. External Program Memory Read Cycle



## 7.5.4 External Data Memory Characteristics

## Table 21. Symbol Description

Symbol	Parameter
T <sub>RLRH</sub>	RD Pulse Width
T <sub>WLWH</sub>	WR Pulse Width
T <sub>RLDV</sub>	RD to Valid Data In
T <sub>RHDX</sub>	Data Hold After RD
T <sub>RHDZ</sub>	Data Float After RD
T <sub>LLDV</sub>	ALE to Valid Data In
T <sub>AVDV</sub>	Address to Valid Data In
T <sub>LLWL</sub>	ALE to WR or RD
T <sub>AVWL</sub>	Address to $\overline{WR}$ or $\overline{RD}$
T <sub>QVWX</sub>	Data Valid to WR Transition
T <sub>QVWH</sub>	Data set-up to WR High
T <sub>WHQX</sub>	Data Hold After WR
T <sub>RLAZ</sub>	RD Low to Address Float
T <sub>WHLH</sub>	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE high



Speed	-1 40 N	M /IHz	- X2 r 30 N 60 MH	V node ⁄IHz z equiv.	- standar 40 N	V °d mode MHz		L node ⁄IHz z equiv.	-j standar 30 N	L ·d mode ⁄IHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T <sub>RLRH</sub>	130		85		135		125		175		ns
T <sub>WLWH</sub>	130		85		135		125		175		ns
T <sub>RLDV</sub>		100		60		102		95		137	ns
T <sub>RHDX</sub>	0		0		0		0		0		ns
T <sub>RHDZ</sub>		30		18		35		25		42	ns
T <sub>LLDV</sub>		160		98		165		155		222	ns
T <sub>AVDV</sub>		165		100		175		160		235	ns
T <sub>LLWL</sub>	50	100	30	70	55	95	45	105	70	130	ns
T <sub>AVWL</sub>	75		47		80		70		103		ns
T <sub>QVWX</sub>	10		7		15		5		13		ns
T <sub>QVWH</sub>	160		107		165		155		213		ns
T <sub>WHQX</sub>	15		9		17		10		18		ns
T <sub>RLAZ</sub>		0		0		0		0		0	ns
T <sub>WHLH</sub>	10	40	7	27	15	35	5	45	13	53	ns

Table 22. AC Parameters for a Fix Clock



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T <sub>RLRH</sub>	Min	6 T - x	3 T - x	20	15	25	ns
T <sub>WLWH</sub>	Min	6 T - x	3 T - x	20	15	25	ns
T <sub>RLDV</sub>	Max	5 T - x	2.5 T - x	25	23	30	ns
T <sub>RHDX</sub>	Min	x	x	0	0	0	ns
T <sub>RHDZ</sub>	Max	2 T - x	T - x	20	15	25	ns
T <sub>LLDV</sub>	Max	8 T - x	4T -x	40	35	45	ns
T <sub>AVDV</sub>	Max	9 T - x	4.5 T - x	60	50	65	ns
T <sub>LLWL</sub>	Min	3 T - x	1.5 T - x	25	20	30	ns
T <sub>LLWL</sub>	Max	3 T + x	1.5 T + x	25	20	30	ns
T <sub>AVWL</sub>	Min	4 T - x	2 T - x	25	20	30	ns
T <sub>QVWX</sub>	Min	T - x	0.5 T - x	15	10	20	ns
T <sub>QVWH</sub>	Min	7 T - x	3.5 T - x	15	10	20	ns
T <sub>WHQX</sub>	Min	T - x	0.5 T - x	10	8	15	ns
T <sub>RLAZ</sub>	Max	x	x	0	0	0	ns
T <sub>WHLH</sub>	Min	T - x	0.5 T - x	15	10	20	ns
T <sub>WHLH</sub>	Max	T + x	0.5 T + x	15	10	20	ns

 Table 23. AC Parameters for a Variable Clock: derating formula

## 7.5.5 External Data Memory Write Cycle



Figure 15. External Data Memory Write Cycle



Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T <sub>XLXL</sub>	Min	12 T	6 T				ns
T <sub>QVHX</sub>	Min	10 T - x	5 T - x	50	50	50	ns
T <sub>XHQX</sub>	Min	2 T - x	T - x	20	20	20	ns
T <sub>XHDX</sub>	Min	X	Х	0	0	0	ns
T <sub>XHDV</sub>	Max	10 T - x	5 T- x	133	133	133	ns

 Table 26. AC Parameters for a Variable Clock: derating formula

## 7.5.8 Shift Register Timing Waveforms



Figure 17. Shift Register Timing Waveforms



### 7.5.9 External Clock Drive Characteristics (XTAL1)

Table	27.	AC	Parameters
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Symbol	Parameter	Min	Max	Units
T <sub>CLCL</sub>	Oscillator Period	25		ns
T <sub>CHCX</sub>	High Time	5		ns
T <sub>CLCX</sub>	Low Time	5		ns
T <sub>CLCH</sub>	Rise Time		5	ns
T <sub>CHCL</sub>	Fall Time		5	ns
T <sub>CHCX</sub> /T <sub>CLCX</sub>	Cyclic ratio in X2 mode	40	60	%

### 7.5.10 External Clock Drive Waveforms



#### Figure 18. External Clock Drive Waveforms

#### 7.5.11 AC Testing Input/Output Waveforms



Figure 19. AC Testing Input/Output Waveforms

AC inputs during testing are driven at  $V_{CC}$  - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at  $V_{IH}$  min for a logic "1" and  $V_{IL}$  max for a logic "0".

#### 7.5.12 Float Waveforms



Figure 20. Float Waveforms



## 8. Ordering Information



Table 28. Maximum Clock Frequency

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	<b>60</b>	<b>40</b>	