



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                     |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                              |
| Core Processor             | PIC                                                                                                                                                                 |
| Core Size                  | 8-Bit                                                                                                                                                               |
| Speed                      | 32MHz                                                                                                                                                               |
| Connectivity               | I <sup>2</sup> C, LINbus, SPI, UART/USART                                                                                                                           |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT                                                                                                                               |
| Number of I/O              | 12                                                                                                                                                                  |
| Program Memory Size        | 14KB (8K x 14)                                                                                                                                                      |
| Program Memory Type        | FLASH                                                                                                                                                               |
| EEPROM Size                | -                                                                                                                                                                   |
| RAM Size                   | 1K x 8                                                                                                                                                              |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V                                                                                                                                                         |
| Data Converters            | A/D 8x10b; D/A 1x8b                                                                                                                                                 |
| Oscillator Type            | Internal                                                                                                                                                            |
| Operating Temperature      | -40°C ~ 125°C (TA)                                                                                                                                                  |
| Mounting Type              | Surface Mount                                                                                                                                                       |
| Package / Case             | 16-VQFN Exposed Pad                                                                                                                                                 |
| Supplier Device Package    | 16-QFN (4x4)                                                                                                                                                        |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1705-e-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1705-e-ml</a> |



# PIC16(L)F170X/171X

## Cost Effective 8-Bit Intelligent Analog Flash Microcontrollers

### Description:

PIC16F(L)170X/171X microcontrollers combine Intelligent Analog integration with low cost and extreme low power (XLP) to suit a variety of general purpose applications. These 14 to 44-pin devices deliver on-chip Op Amps, Core Independent Peripherals (CLC, NCO and COG), Peripheral Pin Select and Zero-Cross Detect, providing for increased design flexibility.

### Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - 0-32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-bit Timers
- One 16-bit Timer
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-Out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

### Memory:

- Up to 16 Kwords Flash Program Memory
- Up to 2048 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes

### Operating Characteristics:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF170X/171X)
  - 2.3V to 5.5V (PIC16F170X/171X)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Digital Peripherals:

- Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Complementary Output Generator (COG):
  - Rising/falling edge dead-band control/blanking
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0Hz < FNCO < 32 MHz
  - Resolution: FNCO/220
- Capture/Compare/PWM (CCP) module
- PWM: Two 10-bit Pulse-Width Modulators
- Serial Communications:
  - SPI, I<sup>2</sup>C™, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

### Intelligent Analog Peripherals:

- Operational Amplifiers:
  - Two configurable rail-to-rail op amps
  - Selectable internal and external channels
  - 2 MHz gain bandwidth product
- High-Speed Comparators:
  - Up to two comparators
  - 50 ns response time
  - Rail-to-rail inputs
- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 28 external channels
  - Conversion available during Sleep
  - Temperature indicator
- Zero-Cross Detector (ZCD):
  - Detect when AC signal on pin crosses ground
- 8-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Internal Voltage Reference module

# PIC16(L)F170X/171X

## Clocking Structure:

- 16 MHz Internal Oscillator Block:
  - $\pm 1\%$  at calibration
  - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Two external clock modes up to 32 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

## Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
  - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

## PIC16(L)F170X/171X FAMILY TYPES

| Device        | Program Memory Flash (words) | Data SRAM (bytes) | I/O Pins | 8-bit/16-bit Timers | High-Speed Comparators | Op Amp | 10-bit ADC (ch) | 5-/8-bit DAC | Zero Cross | CCP/PWM | COG | EUSART | I <sup>2</sup> C™/SPI | CLC | NCO | Debug <sup>(1)</sup> |
|---------------|------------------------------|-------------------|----------|---------------------|------------------------|--------|-----------------|--------------|------------|---------|-----|--------|-----------------------|-----|-----|----------------------|
| PIC16(L)F1703 | 2k                           | 256               | 12       | 2/1                 | 0                      | 2      | 8               | 0/0          | 1          | 2/0     | 0   | 0      | 1                     | 0   | 0   | I/E                  |
| PIC16(L)F1704 | 4k                           | 512               | 12       | 4/1                 | 2                      | 2      | 8               | 0/1          | 1          | 2/2     | 1   | 1      | 1                     | 3   | 0   | I/E                  |
| PIC16(L)F1705 | 8k                           | 1024              | 12       | 4/1                 | 2                      | 2      | 8               | 0/1          | 1          | 2/2     | 1   | 1      | 1                     | 3   | 0   | I/E                  |
| PIC16(L)F1707 | 2k                           | 256               | 18       | 2/1                 | 0                      | 2      | 8               | 0/0          | 1          | 2/0     | 0   | 0      | 1                     | 0   | 0   | I/E                  |
| PIC16(L)F1708 | 4k                           | 512               | 18       | 4/1                 | 2                      | 2      | 12              | 0/1          | 1          | 2/2     | 1   | 1      | 1                     | 3   | 0   | I/E                  |
| PIC16(L)F1709 | 8k                           | 1024              | 18       | 4/1                 | 2                      | 2      | 12              | 0/1          | 1          | 2/2     | 1   | 1      | 1                     | 3   | 0   | I/E                  |
| PIC16(L)F1713 | 4k                           | 512               | 25       | 4/1                 | 2                      | 2      | 17              | 1/1          | 1          | 2/2     | 1   | 1      | 1                     | 4   | 1   | I/E                  |
| PIC16(L)F1716 | 8k                           | 1024              | 25       | 4/1                 | 2                      | 2      | 17              | 1/1          | 1          | 2/2     | 1   | 1      | 1                     | 4   | 1   | I/E                  |
| PIC16(L)F1717 | 8k                           | 1024              | 36       | 4/1                 | 2                      | 2      | 28              | 1/1          | 1          | 2/2     | 1   | 1      | 1                     | 4   | 1   | I/E                  |
| PIC16(L)F1718 | 16k                          | 2048              | 25       | 4/1                 | 2                      | 2      | 17              | 1/1          | 1          | 2/2     | 1   | 1      | 1                     | 4   | 1   | I/E                  |
| PIC16(L)F1719 | 16k                          | 2048              | 36       | 4/1                 | 2                      | 2      | 28              | 1/1          | 1          | 2/2     | 1   | 1      | 1                     | 4   | 1   | I/E                  |

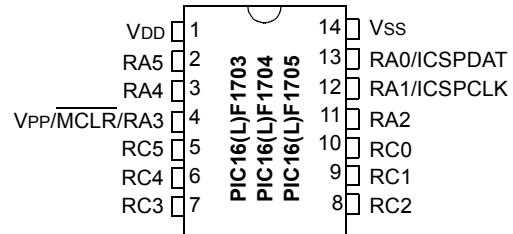
**Note 1:** I – Debugging integrated on chip; H – Debugging via ICD header; E – Debugging via Emulation header.

## PACKAGES

| Device     | PDIP | TSSOP | QFN (4x4x0.9) | SOIC | SSOP | SPDIP | QFN (6x6x0.9) | UQFN (4x4x0.5) | TQFP | UQFN (5x5x0.5) |
|------------|------|-------|---------------|------|------|-------|---------------|----------------|------|----------------|
| PIC16F1703 | x    | x     | x             | x    |      |       |               |                |      |                |
| PIC16F1704 | x    | x     | x             | x    |      |       |               |                |      |                |
| PIC16F1705 | x    | x     | x             | x    |      |       |               |                |      |                |
| PIC16F1707 | x    |       | x             | x    | x    |       |               |                |      |                |
| PIC16F1708 | x    |       | x             | x    | x    |       |               |                |      |                |
| PIC16F1709 | x    |       | x             | x    | x    |       |               |                |      |                |
| PIC16F1713 |      |       |               | x    | x    | x     | x             | x              |      |                |
| PIC16F1716 |      |       |               | x    | x    | x     | x             | x              |      |                |
| PIC16F1717 | x    |       |               |      |      |       |               |                | x    | x              |
| PIC16F1718 |      |       |               | x    | x    | x     | x             | x              |      |                |
| PIC16F1719 | x    |       |               |      |      |       |               |                | x    | x              |

# PIC16(L)F170X/171X

## PIN DIAGRAM – 14-PIN PDIP, SOIC, SSOP



**Note:** See [Table 1](#) and [Table 2](#) for the pin allocation tables.

## PIN DIAGRAM – 16-PIN QFN



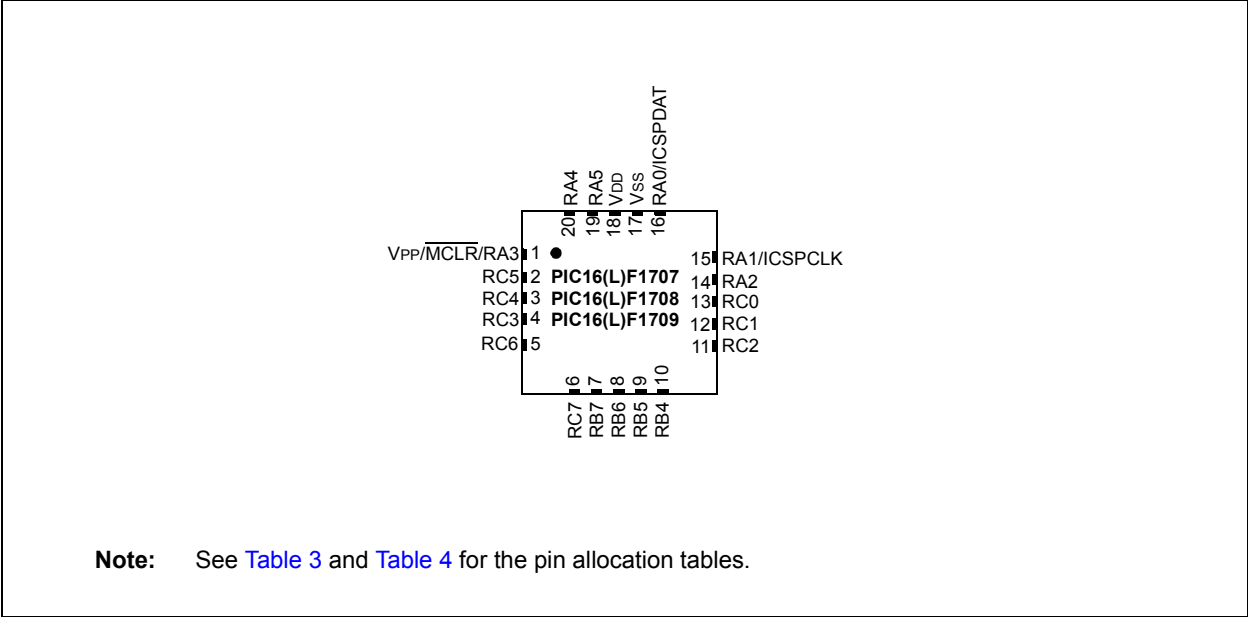
**Note:** See [Table 1](#) and [Table 2](#) or the pin allocation tables.

# PIC16(L)F170X/171X

## PIN DIAGRAM – 20-PIN PDIP, SOIC, SSOP



## PIN DIAGRAM – 20-PIN QFN



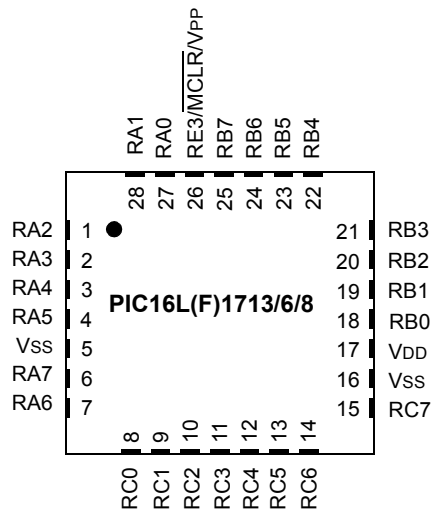
# PIC16(L)F170X/171X

## PIN DIAGRAM – 28-PIN PDIP, SOIC, SSOP



**Note:** See [Table 5](#) and [Table 6](#) for the pin allocation table.

## PIN DIAGRAM – 28-PIN (U)QFN



**Note:** See [Table 5](#) and [Table 6](#) for the pin allocation table.

# PIC16(L)F170X/171X

## PIN DIAGRAM – 40-PIN PDIP



# PIC16(L)F170X/171X

## PIN DIAGRAM – 44-PIN TQFP (10x10)



**Note:** See [Table 7](#) and [Table 8](#) for the pin allocation table.

## PIN DIAGRAM – 40-PIN UQFN (5x5)



**Note:** See [Table 7](#) and [Table 8](#) for the pin allocation table.

**TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1703)**

| (2) I/O            | PDIP/SOIC/SSOP | QFN | ADC | Reference | Op Amp  | Zero Cross | Timers               | CCP                 | MSSP                                     | CLC | Interrupt                 | Pull-up | Basic                                       |
|--------------------|----------------|-----|-----|-----------|---------|------------|----------------------|---------------------|------------------------------------------|-----|---------------------------|---------|---------------------------------------------|
| RA0                | 13             | 12  | AN0 | VREF-     | —       | —          | —                    | —                   | —                                        | —   | IOC                       | Y       | ICSPDAT                                     |
| RA1                | 12             | 11  | AN1 | VREF+     | —       | —          | —                    | —                   | —                                        | —   | IOC                       | Y       | ICSPCLK                                     |
| RA2                | 11             | 10  | AN2 | —         | —       | ZCD        | T0CKI <sup>(1)</sup> | —                   | —                                        | —   | INT <sup>(1)</sup><br>IOC | Y       | —                                           |
| RA3                | 4              | 3   | —   | —         | —       | —          | —                    | —                   | —                                        | —   | IOC                       | Y       | $\overline{\text{MCLR}}$<br>V <sub>PP</sub> |
| RA4                | 3              | 2   | AN3 | —         | —       | —          | T1G <sup>(1)</sup>   | —                   | —                                        | —   | IOC                       | Y       | CLKOUT                                      |
| RA5                | 2              | 1   | —   | —         | —       | —          | T1CKI <sup>(1)</sup> | —                   | —                                        | —   | IOC                       | Y       | CLKIN                                       |
| RC0                | 10             | 9   | AN4 | —         | OPA1IN+ | —          | —                    | —                   | SCK <sup>(1)</sup><br>SCL <sup>(3)</sup> | —   | IOC                       | Y       | —                                           |
| RC1                | 9              | 8   | AN5 | —         | OPA1IN- | —          | —                    | —                   | SDI <sup>(1)</sup><br>SDA <sup>(3)</sup> | —   | IOC                       | Y       | —                                           |
| RC2                | 8              | 7   | AN6 | —         | OPA1OUT | —          | —                    | —                   | —                                        | —   | IOC                       | Y       | —                                           |
| RC3                | 7              | 6   | AN7 | —         | OPA2OUT | —          | —                    | CCP2 <sup>(1)</sup> | $\overline{\text{SS}}$ <sup>(1)</sup>    | —   | IOC                       | Y       | —                                           |
| RC4                | 6              | 5   | —   | —         | OPA2IN- | —          | —                    | —                   | —                                        | —   | IOC                       | Y       | —                                           |
| RC5                | 5              | 4   | —   | —         | OPA2IN+ | —          | —                    | CCP1 <sup>(1)</sup> | —                                        | —   | IOC                       | Y       | —                                           |
| V <sub>DD</sub>    | 1              | 16  | —   | —         | —       | —          | —                    | —                   | —                                        | —   | —                         | —       | V <sub>DD</sub>                             |
| V <sub>SS</sub>    | 14             | 13  | —   | —         | —       | —          | —                    | —                   | —                                        | —   | —                         | —       | V <sub>SS</sub>                             |
| OUT <sup>(2)</sup> | —              | —   | —   | —         | —       | —          | —                    | CPP1                | SDA <sup>(3)</sup>                       | —   | —                         | —       | —                                           |
|                    | —              | —   | —   | —         | —       | —          | —                    | CPP2                | SCL <sup>(3)</sup><br>SCK                | —   | —                         | —       | —                                           |
|                    | —              | —   | —   | —         | —       | —          | —                    | —                   | SDO                                      | —   | —                         | —       | —                                           |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**TABLE 2: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1704/5)**

| I/O <sup>(2)</sup> | PDIP/SOIC/SSOP | QFN | ADC | Reference | Comparator       | Op Amp  | DAC      | Zero Cross | Timers                        | CCP                 | PWM     | COG                  | MSSP                                     | EUSART            | CLC                   | Interrupt                 | Pull-up | Basic                                       |
|--------------------|----------------|-----|-----|-----------|------------------|---------|----------|------------|-------------------------------|---------------------|---------|----------------------|------------------------------------------|-------------------|-----------------------|---------------------------|---------|---------------------------------------------|
| RA0                | 13             | 12  | AN0 | VREF-     | C1IN+            | —       | DAC1OUT  | —          | —                             | —                   | —       | —                    | —                                        | —                 | —                     | IOC                       | Y       | ICSPDAT                                     |
| RA1                | 12             | 11  | AN1 | VREF+     | C1IN0-<br>C2IN0- | —       | —        | —          | —                             | —                   | —       | —                    | —                                        | —                 | —                     | IOC                       | Y       | ICSPCLK                                     |
| RA2                | 11             | 10  | AN2 | —         | —                | —       | DAC1OUT2 | ZCD        | T0CKI <sup>(1)</sup>          | —                   | —       | COGIN <sup>(1)</sup> | —                                        | —                 | —                     | INT <sup>(1)</sup><br>IOC | Y       | —                                           |
| RA3                | 4              | 3   | —   | —         | —                | —       | —        | —          | —                             | —                   | —       | —                    | —                                        | —                 | —                     | IOC                       | Y       | $\overline{\text{MCLR}}$<br>V <sub>PP</sub> |
| RA4                | 3              | 2   | AN3 | —         | —                | —       | —        | —          | T1G <sup>(1)</sup><br>SOSCO   | —                   | —       | —                    | —                                        | —                 | —                     | IOC                       | Y       | CLKOUT<br>OSC2                              |
| RA5                | 2              | 1   | —   | —         | —                | —       | —        | —          | T1CKI <sup>(1)</sup><br>SOSCI | —                   | —       | —                    | —                                        | —                 | CLCIN3 <sup>(1)</sup> | IOC                       | Y       | CLKIN<br>OSC1                               |
| RC0                | 10             | 9   | AN4 | —         | C2IN+            | OPA1IN+ | —        | —          | —                             | —                   | —       | —                    | SCK <sup>(1)</sup><br>SCL <sup>(3)</sup> | —                 | —                     | IOC                       | Y       | —                                           |
| RC1                | 9              | 8   | AN5 | —         | C1IN1-<br>C2IN1- | OPA1IN- | —        | —          | —                             | —                   | —       | —                    | SDI <sup>(1)</sup><br>SDA <sup>(3)</sup> | —                 | CLCIN2 <sup>(1)</sup> | IOC                       | Y       | —                                           |
| RC2                | 8              | 7   | AN6 | —         | C1IN2-<br>C2IN2- | OPA1OUT | —        | —          | —                             | —                   | —       | —                    | —                                        | —                 | —                     | IOC                       | Y       | —                                           |
| RC3                | 7              | 6   | AN7 | —         | C1IN3-<br>C2IN3- | OPA2OUT | —        | —          | —                             | CCP2 <sup>(1)</sup> | —       | —                    | $\overline{\text{SS}}$ <sup>(1)</sup>    | —                 | CLCIN0 <sup>(1)</sup> | IOC                       | Y       | —                                           |
| RC4                | 6              | 5   | —   | —         | —                | OPA2IN- | —        | —          | —                             | —                   | —       | —                    | —                                        | CK <sup>(1)</sup> | CLCIN1 <sup>(1)</sup> | IOC                       | Y       | —                                           |
| RC5                | 5              | 4   | —   | —         | —                | OPA2IN+ | —        | —          | —                             | CCP1 <sup>(1)</sup> | —       | —                    | —                                        | RX <sup>(3)</sup> | —                     | IOC                       | Y       | —                                           |
| V <sub>DD</sub>    | 1              | 16  | —   | —         | —                | —       | —        | —          | —                             | —                   | —       | —                    | —                                        | —                 | —                     | —                         | —       | V <sub>DD</sub>                             |
| V <sub>SS</sub>    | 14             | 13  | —   | —         | —                | —       | —        | —          | —                             | —                   | —       | —                    | —                                        | —                 | —                     | —                         | —       | V <sub>SS</sub>                             |
| OUT <sup>(2)</sup> | —              | —   | —   | —         | C1OUT            | —       | —        | —          | —                             | CPP1                | PWM3OUT | COGA                 | SDA <sup>(3)</sup>                       | CK                | CLC1OUT               | —                         | —       | —                                           |
|                    | —              | —   | —   | —         | C2OUT            | —       | —        | —          | —                             | CPP2                | PWM4OUT | COGB                 | SCL <sup>(3)</sup>                       | DT <sup>(3)</sup> | CLC2OUT               | —                         | —       | —                                           |
|                    | —              | —   | —   | —         | —                | —       | —        | —          | —                             | —                   | —       | COGC                 | SDO                                      | TX                | CLC3OUT               | —                         | —       | —                                           |
|                    | —              | —   | —   | —         | —                | —       | —        | —          | —                             | —                   | —       | COGD                 | SCK                                      | —                 | —                     | —                         | —       | —                                           |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**TABLE 3: 20-PIN ALLOCATION TABLE (PIC16(L)F1707)**

| (IO/I)             | PDI/SOIC/<br>SSOP | QFN | ADC  | Reference | Op Amp  | Zero Cross | Timers               | CCP                 | MSSP                                     | Interrupt                 | Pull-up | Basic                   |
|--------------------|-------------------|-----|------|-----------|---------|------------|----------------------|---------------------|------------------------------------------|---------------------------|---------|-------------------------|
| RA0                | 19                | 16  | AN0  | VREF-     | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | ICSPDAT                 |
| RA1                | 18                | 15  | AN1  | VREF+     | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | ICSPCLK                 |
| RA2                | 17                | 14  | AN2  | —         | —       | ZCD        | T0CKI <sup>(1)</sup> | —                   | —                                        | INT <sup>(1)</sup><br>IOC | Y       | —                       |
| RA3                | 4                 | 1   | —    | —         | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4                | 3                 | 20  | AN3  | —         | —       | —          | T1G <sup>(1)</sup>   | —                   | —                                        | IOC                       | Y       | CLKOUT                  |
| RA5                | 2                 | 19  | —    | —         | —       | —          | T1CKI                | —                   | —                                        | IOC                       | Y       | CLKIN                   |
| RB4                | 13                | 10  | AN10 | —         | OPA1IN- | —          | —                    | —                   | SCK <sup>(1)</sup><br>SDA <sup>(3)</sup> | IOC                       | Y       | —                       |
| RB5                | 12                | 9   | AN11 | —         | OPA1IN+ | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| RB6                | 11                | 8   | —    | —         | —       | —          | —                    | —                   | SDI <sup>(1)</sup><br>SCL <sup>(3)</sup> | IOC                       | Y       | —                       |
| RB7                | 10                | 7   | —    | —         | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| RC0                | 16                | 13  | AN4  | —         | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| RC1                | 15                | 12  | AN5  | —         | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| RC2                | 14                | 11  | AN6  | —         | OPA1OUT | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| RC3                | 7                 | 4   | AN7  | —         | OPA2OUT | —          | —                    | CCP2 <sup>(1)</sup> | —                                        | IOC                       | Y       | —                       |
| RC4                | 6                 | 3   | —    | —         | OPA2IN- | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| RC5                | 5                 | 2   | —    | —         | OPA2IN+ | —          | —                    | CCP1 <sup>(1)</sup> | —                                        | IOC                       | Y       | —                       |
| RC6                | 8                 | 5   | AN8  | —         | —       | —          | —                    | —                   | SS <sup>(1)</sup>                        | IOC                       | Y       | —                       |
| RC7                | 9                 | 6   | AN9  | —         | —       | —          | —                    | —                   | —                                        | IOC                       | Y       | —                       |
| V <sub>DD</sub>    | 1                 | 18  | —    | —         | —       | —          | —                    | —                   | —                                        | —                         | —       | V <sub>DD</sub>         |
| V <sub>SS</sub>    | 20                | 17  | —    | —         | —       | —          | —                    | —                   | —                                        | —                         | —       | V <sub>SS</sub>         |
| OUT <sup>(2)</sup> | —                 | —   | —    | —         | —       | —          | —                    | CPP1                | SDA <sup>(3)</sup>                       | —                         | —       | —                       |
|                    | —                 | —   | —    | —         | —       | —          | —                    | CPP2                | SCL <sup>(3)</sup><br>SCK                | —                         | —       | —                       |
|                    | —                 | —   | —    | —         | —       | —          | —                    | —                   | SDO                                      | —                         | —       | —                       |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1708/9)**

|     | I/O <sup>(2)</sup> | PDIP/SOIC/<br>SSOP | QFN  | ADC   | Reference        | Comparator | Op Amp  | DAC      | Zero Cross | Timers                      | CCP                 | PWM | COG                  | MSSP                                     | EUSART                   | CLC                   | Interrupt                 | Pull-up | Basic                   |
|-----|--------------------|--------------------|------|-------|------------------|------------|---------|----------|------------|-----------------------------|---------------------|-----|----------------------|------------------------------------------|--------------------------|-----------------------|---------------------------|---------|-------------------------|
| RA0 | 19                 | 16                 | AN0  | VREF- | C1IN+            | —          | —       | DAC1OUT  | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | ICSPDAT                 |
| RA1 | 18                 | 15                 | AN1  | VREF+ | C1IN0-<br>C2IN0- | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | ICSPCLK                 |
| RA2 | 17                 | 14                 | AN2  | —     | —                | —          | —       | DAC1OUT2 | ZCD        | T0CKI <sup>(1)</sup>        | —                   | —   | COGIN <sup>(1)</sup> | —                                        | —                        | —                     | INT <sup>(1)</sup><br>IOC | Y       | —                       |
| RA3 | 4                  | 1                  | —    | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4 | 3                  | 20                 | AN3  | —     | —                | —          | —       | —        | —          | T1G <sup>(1)</sup><br>SOSCO | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | CLKOUT<br>OSC2          |
| RA5 | 2                  | 19                 | —    | —     | —                | —          | —       | —        | —          | T1CKI<br>SOSCI              | —                   | —   | —                    | —                                        | —                        | CLCIN3 <sup>(1)</sup> | IOC                       | Y       | CLKIN<br>OSC1           |
| RB4 | 13                 | 10                 | AN10 | —     | —                | —          | OPA1IN- | —        | —          | —                           | —                   | —   | —                    | SCK <sup>(1)</sup><br>SDA <sup>(3)</sup> | —                        | —                     | IOC                       | Y       | —                       |
| RB5 | 12                 | 9                  | AN11 | —     | —                | —          | OPA1IN+ | —        | —          | —                           | —                   | —   | —                    | —                                        | RX <sup>(1)</sup><br>(3) | —                     | IOC                       | Y       | —                       |
| RB6 | 11                 | 8                  | —    | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | SDI <sup>(1)</sup><br>SCL <sup>(3)</sup> | —                        | —                     | IOC                       | Y       | —                       |
| RB7 | 10                 | 7                  | —    | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | CK <sup>(1)</sup><br>(3) | —                     | IOC                       | Y       | —                       |
| RC0 | 16                 | 13                 | AN4  | —     | C2IN+            | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | —                       |
| RC1 | 15                 | 12                 | AN5  | —     | C1IN1-<br>C2IN1- | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | CLCIN2 <sup>(1)</sup> | IOC                       | Y       | —                       |
| RC2 | 14                 | 11                 | AN6  | —     | C1IN2-<br>C2IN2- | —          | OPA1OUT | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | —                       |
| RC3 | 7                  | 4                  | AN7  | —     | C1IN3-<br>C2IN3- | —          | OPA2OUT | —        | —          | —                           | CCP2 <sup>(1)</sup> | —   | —                    | —                                        | —                        | CLCIN0 <sup>(1)</sup> | IOC                       | Y       | —                       |
| RC4 | 6                  | 3                  | —    | —     | —                | —          | OPA2IN- | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | CLCIN1 <sup>(1)</sup> | IOC                       | Y       | —                       |
| RC5 | 5                  | 2                  | —    | —     | —                | —          | OPA2IN+ | —        | —          | —                           | CCP1 <sup>(1)</sup> | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | —                       |
| RC6 | 8                  | 5                  | AN8  | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | SS <sup>(1)</sup>                        | —                        | —                     | IOC                       | Y       | —                       |
| RC7 | 9                  | 6                  | AN9  | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | IOC                       | Y       | —                       |
| VDD | 1                  | 18                 | —    | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | —                         | —       | VDD                     |
| VSS | 20                 | 17                 | —    | —     | —                | —          | —       | —        | —          | —                           | —                   | —   | —                    | —                                        | —                        | —                     | —                         | —       | VSS                     |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

# PIC16(L)F170X/171X

| I/O <sup>(2)</sup> | PDIP/SOIC/<br>SSOP | QFN | ADC | Reference | Comparator | Op Amp | DAC | Zero Cross | Timers | CCP  | PWM     | COG  | MSSP               | EUSART | CLC     | Interrupt | Pull-up | Basic |
|--------------------|--------------------|-----|-----|-----------|------------|--------|-----|------------|--------|------|---------|------|--------------------|--------|---------|-----------|---------|-------|
| OUT <sup>(2)</sup> | —                  | —   | —   | —         | C1OUT      | —      | —   | —          | —      | CPP1 | PWM3OUT | COGA | SDA <sup>(3)</sup> | CK     | CLC1OUT | —         | —       | —     |
|                    | —                  | —   | —   | —         | C2OUT      | —      | —   | —          | —      | CPP2 | PWM4OUT | COGB | SCL <sup>(3)</sup> | DT     | CLC2OUT | —         | —       | —     |
|                    | —                  | —   | —   | —         | —          | —      | —   | —          | —      | —    | —       | COGC | SDO                | TX     | CLC3OUT | —         | —       | —     |
|                    | —                  | —   | —   | —         | —          | —      | —   | —          | —      | —    | —       | COGD | —                  | —      | —       | —         | —       | —     |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**TABLE 5: 28-PIN ALLOCATION TABLE (PIC16L(F)1713/6/8) (PART 1)**

| I/O <sup>(2)</sup> | PDIP, SOIC,<br>SSOP | QFN, UQFN | ADC  | Reference | Comparator       | Op Amp  | DAC                  | Zero Cross | Timers                        | CCP                 | NCO    | PWM | COG                  | MSSP               | EUSART | CLC                   | Interrupt                 | Pull-up | Basic          |
|--------------------|---------------------|-----------|------|-----------|------------------|---------|----------------------|------------|-------------------------------|---------------------|--------|-----|----------------------|--------------------|--------|-----------------------|---------------------------|---------|----------------|
| RA0                | 2                   | 27        | AN0  |           | C1IN0-<br>C2IN0- |         |                      |            |                               |                     |        |     |                      |                    |        | CLCIN0 <sup>(1)</sup> | IOC                       | Y       |                |
| RA1                | 3                   | 28        | AN1  |           | C1IN1-<br>C2IN1- | OPA1OUT |                      |            |                               |                     |        |     |                      |                    |        | CLCIN1 <sup>(1)</sup> | IOC                       | Y       |                |
| RA2                | 4                   | 1         | AN2  | Vref-     | C1IN0+<br>C2IN0+ |         | DAC1OUT1             |            |                               |                     |        |     |                      |                    |        |                       |                           | Y       |                |
| RA3                | 5                   | 2         | AN3  | Vref+     | C1IN1+           |         |                      |            |                               |                     |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RA4                | 6                   | 3         |      |           |                  | OPA1IN+ |                      |            | T0CKI <sup>(1)</sup>          |                     |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RA5                | 7                   | 4         | AN4  |           |                  | OPA1IN- | DAC2OUT1             |            |                               |                     |        |     |                      | nSS <sup>(1)</sup> |        |                       | IOC                       | Y       |                |
| RA6                | 10                  | 7         |      |           |                  |         |                      |            |                               |                     |        |     |                      |                    |        |                       | IOC                       |         | OSC2<br>CLKOUT |
| RA7                | 9                   | 6         |      |           |                  |         |                      |            |                               |                     | NCOCLK |     |                      |                    |        |                       | IOC                       |         | OSC1<br>CLKIN  |
| RB0                | 21                  | 18        | AN12 |           | C2IN1+           |         |                      | ZCD        |                               |                     |        |     | COGIN <sup>(1)</sup> |                    |        |                       | INT <sup>(1)</sup><br>IOC |         |                |
| RB1                | 22                  | 19        | AN10 |           | C1IN3-<br>C2IN3- | OPA2OUT |                      |            |                               |                     |        |     |                      |                    |        |                       | IOC                       |         |                |
| RB2                | 23                  | 20        | AN8  |           |                  | OPA2IN- |                      |            |                               |                     |        |     |                      |                    |        |                       | IOC                       |         |                |
| RB3                | 24                  | 21        | AN9  |           | C1IN2-<br>C2IN2- | OPA2IN+ |                      |            |                               |                     |        |     |                      |                    |        |                       | IOC                       |         |                |
| RB4                | 25                  | 22        | AN11 |           |                  |         |                      |            |                               |                     |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RB5                | 26                  | 23        | AN13 |           |                  |         |                      |            | T1G <sup>(1)</sup>            |                     |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RB6                | 27                  | 24        |      |           |                  |         |                      |            |                               |                     |        |     |                      | SCL <sup>(1)</sup> |        | CLCIN2 <sup>(1)</sup> | IOC                       | Y       | ICSPCLK        |
| RB7                | 28                  | 25        |      |           |                  |         | DAC1OUT2<br>DAC2OUT2 |            |                               |                     |        |     |                      |                    |        | CLCIN3 <sup>(1)</sup> | IOC                       | Y       | ICSPDAT        |
| RC0                | 11                  | 8         |      |           |                  |         |                      |            | T1CKI <sup>(1)</sup><br>SOSCO |                     |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RC1                | 12                  | 9         |      |           |                  |         |                      |            | SOSCI                         | CCP2 <sup>(1)</sup> |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RC2                | 13                  | 10        | AN14 |           |                  |         |                      |            |                               | CCP1 <sup>(1)</sup> |        |     |                      |                    |        |                       | IOC                       | Y       |                |
| RC3                | 14                  | 11        | AN15 |           |                  |         |                      |            |                               |                     |        |     |                      | SCK <sup>(1)</sup> |        |                       | IOC                       | Y       |                |

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

**TABLE 6: 28-PIN ALLOCATION TABLE (PIC16L(F)1713/6/8) (PART 2)**

| I/O <sup>(2)</sup> | PDIP, SOIC,<br>SSOP | QFN, UQFN | ADC  | Reference | Comparator     | Op Amp | DAC | Zero Cross | Timers                                | CCP          | NCO    | PWM                | COG                          | MSSP                                                | EUSART                     | CLC                                      | Interrupt | Pull-up | Basic       |
|--------------------|---------------------|-----------|------|-----------|----------------|--------|-----|------------|---------------------------------------|--------------|--------|--------------------|------------------------------|-----------------------------------------------------|----------------------------|------------------------------------------|-----------|---------|-------------|
| RC4                | 15                  | 12        | AN16 |           |                |        |     |            |                                       |              |        |                    |                              | SDI <sup>(1)</sup><br>SDA <sup>(1)</sup>            |                            |                                          | IOC       | Y       |             |
| RC5                | 16                  | 13        | AN17 |           |                |        |     |            |                                       |              |        |                    |                              |                                                     |                            |                                          | IOC       | Y       |             |
| RC6                | 17                  | 14        | AN18 |           |                |        |     |            |                                       |              |        |                    |                              |                                                     | CK <sup>(3)</sup>          |                                          | IOC       | Y       |             |
| RC7                | 18                  | 15        | AN19 |           |                |        |     |            |                                       |              |        |                    |                              |                                                     | RX <sup>(3)</sup>          |                                          | IOC       | Y       |             |
| RE3                | 1                   | 26        |      |           |                |        |     |            |                                       |              |        |                    |                              |                                                     |                            |                                          |           |         | MCLR<br>Vpp |
| Vdd                | 20                  | 17        |      |           |                |        |     |            |                                       |              |        |                    |                              |                                                     |                            |                                          |           |         | Vdd         |
| Vss                | 8<br>19             | 5<br>16   |      |           |                |        |     |            |                                       |              |        |                    |                              |                                                     |                            |                                          |           |         | Vss         |
| OUT <sup>(4)</sup> |                     |           |      |           | C1OUT<br>C2OUT |        |     |            |                                       | CCP1<br>CCP2 | NCOOUT | PWM3OUT<br>PWM4OUT | COGA<br>COGB<br>COGC<br>COGD | SDA <sup>(3)</sup><br>SCK/SCL <sup>(3)</sup><br>SDO | TX/CK<br>DT <sup>(3)</sup> | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT |           |         |             |
| IN <sup>(5)</sup>  |                     |           |      |           |                |        |     |            | T1G<br>T1CKI<br>T0CKI<br>CCP1<br>CCP2 |              | NCOCLK |                    | COGIN                        | SDI<br>SCK/SCL <sup>(3)</sup><br>SS                 | RX <sup>(3)</sup><br>CK    | CLCIN0<br>CLCIN1<br>CLCIN2<br>CLCIN3     | INT       |         |             |

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

TABLE 7: PIN ALLOCATION TABLE (PIC16L(F)1717/9) (PART 1)

| I/O <sup>(2)</sup> | PDIP | TQFP | UQFN | ADC  | Reference | Comparator       | Op Amp  | DAC                  | Zero Cross | Timers                        | CCP                 | NCO    | PWM | COG                  | MSSP                                     | EUSART             | CLC                   | Interrupt                 | Pullup | Basic          |
|--------------------|------|------|------|------|-----------|------------------|---------|----------------------|------------|-------------------------------|---------------------|--------|-----|----------------------|------------------------------------------|--------------------|-----------------------|---------------------------|--------|----------------|
| RA0                | 2    | 19   | 17   | AN0  |           | C1IN0-<br>C2IN0- |         |                      |            |                               |                     |        |     |                      |                                          |                    | CLCIN0 <sup>(1)</sup> | IOC                       | Y      |                |
| RA1                | 3    | 20   | 18   | AN1  |           | C1IN1-<br>C2IN1- | OPA1OUT |                      |            |                               |                     |        |     |                      |                                          |                    | CLCIN1 <sup>(1)</sup> | IOC                       | Y      |                |
| RA2                | 4    | 21   | 19   | AN2  | Vref-     | C1IN0+<br>C2IN0+ |         | DAC1OUT1             |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RA3                | 5    | 22   | 20   | AN3  | Vref+     | C1IN1+           |         |                      |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RA4                | 6    | 23   | 21   |      |           |                  | OPA1IN+ |                      |            | T0CKI <sup>(1)</sup>          |                     |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RA5                | 7    | 24   | 22   | AN4  |           |                  | OPA1IN- | DAC2OUT1             |            |                               |                     |        |     |                      | nSS <sup>(1)</sup>                       |                    |                       | IOC                       | Y      |                |
| RA6                | 14   | 31   | 29   |      |           |                  |         |                      |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       |        | OSC2<br>CLKOUT |
| RA7                | 13   | 30   | 28   |      |           |                  |         |                      |            |                               |                     | NCOCLK |     |                      |                                          |                    |                       | IOC                       |        | OSC1<br>CLKIN  |
| RB0                | 33   | 8    | 8    | AN12 |           | C2IN1+           |         |                      | ZCD        |                               |                     |        |     | COGIN <sup>(1)</sup> |                                          |                    |                       | INT <sup>(1)</sup><br>IOC |        |                |
| RB1                | 34   | 9    | 9    | AN10 |           | C1IN3-<br>C2IN3- | OPA2OUT |                      |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       |        |                |
| RB2                | 35   | 10   | 10   | AN8  |           |                  | OPA2IN- |                      |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       |        |                |
| RB3                | 36   | 11   | 11   | AN9  |           | C1IN2-<br>C2IN2- | OPA2IN+ |                      |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       |        |                |
| RB4                | 37   | 14   | 12   | AN11 |           |                  |         |                      |            |                               |                     |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RB5                | 38   | 15   | 13   | AN13 |           |                  |         |                      |            | T1G <sup>(1)</sup>            |                     |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RB6                | 39   | 16   | 14   |      |           |                  |         |                      |            |                               |                     |        |     |                      | SCL <sup>(1)</sup>                       |                    | CLCIN2 <sup>(1)</sup> | IOC                       | Y      | ICSPCLK        |
| RB7                | 40   | 17   | 15   |      |           |                  |         | DAC1OUT2<br>DAC2OUT2 |            |                               |                     |        |     |                      |                                          |                    | CLCIN3 <sup>(1)</sup> | IOC                       | Y      | ICSPDAT        |
| RC0                | 15   | 32   | 30   |      |           |                  |         |                      |            | T1CKI <sup>(1)</sup><br>SOSCO |                     |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RC1                | 16   | 35   | 31   |      |           |                  |         |                      |            | SOSCI                         | CCP2 <sup>(1)</sup> |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RC2                | 17   | 36   | 32   | AN14 |           |                  |         |                      |            |                               | CCP1 <sup>(1)</sup> |        |     |                      |                                          |                    |                       | IOC                       | Y      |                |
| RC3                | 18   | 37   | 33   | AN15 |           |                  |         |                      |            |                               |                     |        |     |                      |                                          | SCK <sup>(1)</sup> |                       | IOC                       | Y      |                |
| RC4                | 23   | 42   | 38   | AN16 |           |                  |         |                      |            |                               |                     |        |     |                      | SDI <sup>(1)</sup><br>SDA <sup>(1)</sup> |                    |                       | IOC                       | Y      |                |

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

**TABLE 8: PIN ALLOCATION TABLE (PIC16L(F)1717/9) (PART 2)**

| I/O <sup>(2)</sup> | PDIP | TQFP | UQFN | ADC  | Reference | Comparator     | Op Amp | DAC | Zero Cross | Timers                                          | CCP          | NCO    | PWM                | COG                          | MSSP                                                | EUSART                               | CLC                                      | Interrupt | Pullup | Basic       |
|--------------------|------|------|------|------|-----------|----------------|--------|-----|------------|-------------------------------------------------|--------------|--------|--------------------|------------------------------|-----------------------------------------------------|--------------------------------------|------------------------------------------|-----------|--------|-------------|
| RC5                | 24   | 43   | 39   | AN17 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          | IOC       | Y      |             |
| RC6                | 25   | 44   | 40   | AN18 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     | CK <sup>(3)</sup>                    |                                          | IOC       | Y      |             |
| RC7                | 26   | 1    | 1    | AN19 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     | RX <sup>(3)</sup>                    |                                          | IOC       | Y      |             |
| RD0                | 19   | 38   | 34   | AN20 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD1                | 20   | 39   | 35   | AN21 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD2                | 21   | 40   | 36   | AN22 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD3                | 22   | 41   | 37   | AN23 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD4                | 27   | 2    | 2    | AN24 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD5                | 28   | 3    | 3    | AN25 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD6                | 29   | 4    | 4    | AN26 |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RD7                | 30   | 5    | 5    |      |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RE0                | 8    | 25   | 23   | AN5  |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RE1                | 9    | 26   | 24   | AN6  |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RE2                | 10   | 27   | 25   | AN7  |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| RE3                | 1    | 18   | 16   |      |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        | MCLR<br>Vpp |
| Vdd                | 11   | 7    | 7    |      |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        | Vdd         |
|                    | 32   | 28   | 26   |      |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| Vss                | 12   | 6    | 6    |      |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        | Vss         |
|                    | 31   | 29   | 27   |      |           |                |        |     |            |                                                 |              |        |                    |                              |                                                     |                                      |                                          |           |        |             |
| OUT <sup>(4)</sup> |      |      |      |      |           | C1OUT<br>C2OUT |        |     |            |                                                 | CCP1<br>CCP2 | NCOOUT | PWM3OUT<br>PWM4OUT | COGA<br>COGB<br>COGC<br>COGD | SDA <sup>(3)</sup><br>SCK/SCL <sup>(3)</sup>        | SDO<br>TX/CK<br>DT (3)               | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT |           |        |             |
| IN <sup>(5)</sup>  |      |      |      |      |           |                |        |     |            | T1G<br>T1CKI<br>T0CKI<br>CCP1<br>CCP2<br>NCOCLK |              |        |                    | COGIN                        | SDI<br>SCK/SCL <sup>(3)</sup><br>SS<br>RX (3)<br>CK | CLCIN0<br>CLCIN1<br>CLCIN2<br>CLCIN3 | INT                                      |           |        |             |

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.



Printed on recycled paper.

ISBN: 9781620772942

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949 ==**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**Santa Clara**  
Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

**Toronto**  
Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hangzhou**  
Tel: 86-571-2819-3187  
Fax: 86-571-2819-3189

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7828  
Fax: 886-7-330-9305

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**UK - Wokingham**  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820