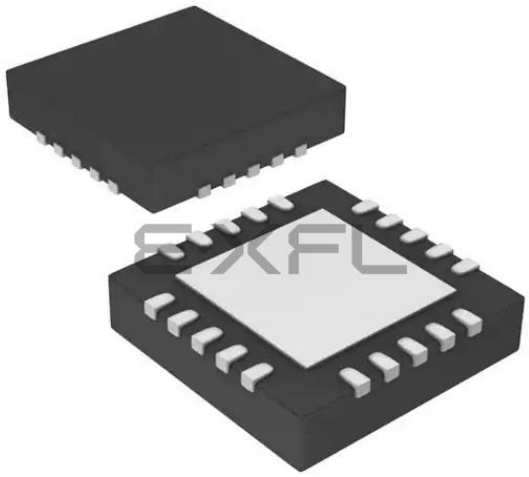


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1709-e-ml

PIC16(L)F170X/171X

Cost Effective 8-Bit Intelligent Analog Flash Microcontrollers

Description:

PIC16F(L)170X/171X microcontrollers combine Intelligent Analog integration with low cost and extreme low power (XLP) to suit a variety of general purpose applications. These 14 to 44-pin devices deliver on-chip Op Amps, Core Independent Peripherals (CLC, NCO and COG), Peripheral Pin Select and Zero-Cross Detect, providing for increased design flexibility.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - 0-32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-bit Timers
- One 16-bit Timer
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-Out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

Memory:

- Up to 16 Kwords Flash Program Memory
- Up to 2048 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes

Operating Characteristics:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF170X/171X)
  - 2.3V to 5.5V (PIC16F170X/171X)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals:

- Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Complementary Output Generator (COG):
  - Rising/falling edge dead-band control/blanking
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0Hz < FNCO < 32 MHz
  - Resolution: FNCO/220
- Capture/Compare/PWM (CCP) module
- PWM: Two 10-bit Pulse-Width Modulators
- Serial Communications:
  - SPI, I^2C™, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, auto-wake-up on start
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Intelligent Analog Peripherals:

- Operational Amplifiers:
  - Two configurable rail-to-rail op amps
  - Selectable internal and external channels
  - 2 MHz gain bandwidth product
- High-Speed Comparators:
  - Up to two comparators
  - 50 ns response time
  - Rail-to-rail inputs
- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 28 external channels
  - Conversion available during Sleep
  - Temperature indicator
- Zero-Cross Detector (ZCD):
  - Detect when AC signal on pin crosses ground
- 8-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Internal Voltage Reference module

Clocking Structure:

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Two external clock modes up to 32 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
  - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC16(L)F170X/171X FAMILY TYPES

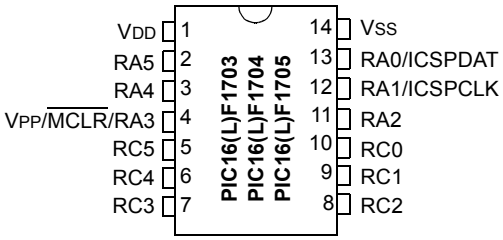
Device	Program Memory Flash (words)	Data SRAM (bytes)	I/O Pins	8-bit/16-bit Timers	High-Speed Comparators	Op Amp	10-bit ADC (ch)	5-/8-bit DAC	Zero Cross	CCP/PWM	COG	EUSART	I^2C™/SPI	CLC	NCO	Debug(1)
PIC16(L)F1703	2k	256	12	2/1	0	2	8	0/0	1	2/0	0	0	1	0	0	I/E
PIC16(L)F1704	4k	512	12	4/1	2	2	8	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1705	8k	1024	12	4/1	2	2	8	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1707	2k	256	18	2/1	0	2	8	0/0	1	2/0	0	0	1	0	0	I/E
PIC16(L)F1708	4k	512	18	4/1	2	2	12	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1709	8k	1024	18	4/1	2	2	12	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1713	4k	512	25	4/1	2	2	17	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1716	8k	1024	25	4/1	2	2	17	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1717	8k	1024	36	4/1	2	2	28	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1718	16k	2048	25	4/1	2	2	17	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1719	16k	2048	36	4/1	2	2	28	1/1	1	2/2	1	1	1	4	1	I/E

Note 1: I – Debugging integrated on chip; H – Debugging via ICD header; E – Debugging via Emulation header.

PACKAGES

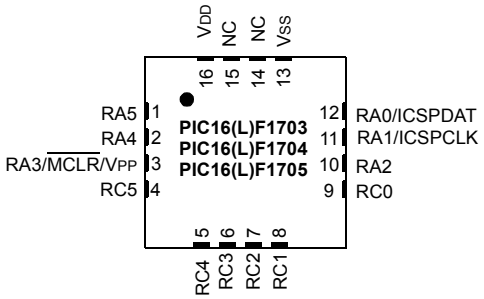
Device	PDIP	TSSOP	QFN (4x4x0.9)	SOIC	SSOP	SPDIP	QFN (6x6x0.9)	UQFN (4x4x0.5)	TQFP	UQFN (5x5x0.5)
PIC16F1703	x	x	x	x						
PIC16F1704	x	x	x	x						
PIC16F1705	x	x	x	x						
PIC16F1707	x		x	x	x					
PIC16F1708	x		x	x	x					
PIC16F1709	x		x	x	x					
PIC16F1713				x	x	x	x	x		
PIC16F1716				x	x	x	x	x		
PIC16F1717	x								x	x
PIC16F1718				x	x	x	x	x		
PIC16F1719	x								x	x

PIN DIAGRAM – 14-PIN PDIP, SOIC, SSOP



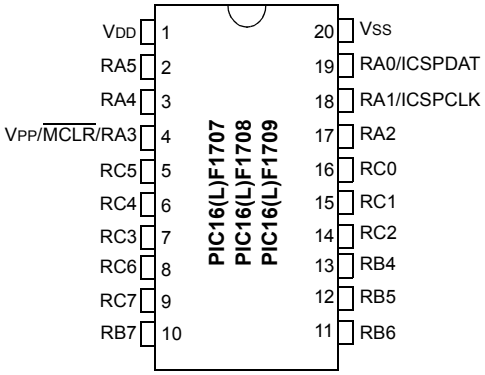
Note: See Table 1 and Table 2 for the pin allocation tables.

PIN DIAGRAM – 16-PIN QFN



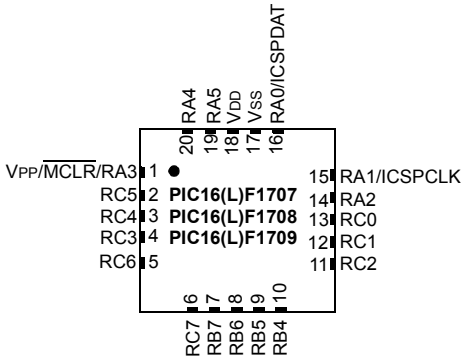
Note: See Table 1 and Table 2 or the pin allocation tables.

PIN DIAGRAM – 20-PIN PDIP, SOIC, SSOP



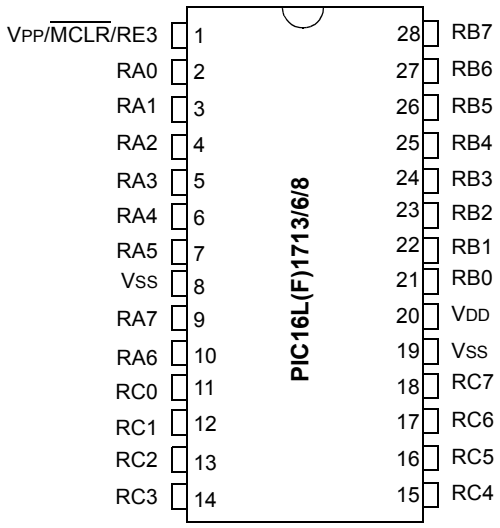
Note: See Table 3 and Table 4 for the pin allocation tables.

PIN DIAGRAM – 20-PIN QFN



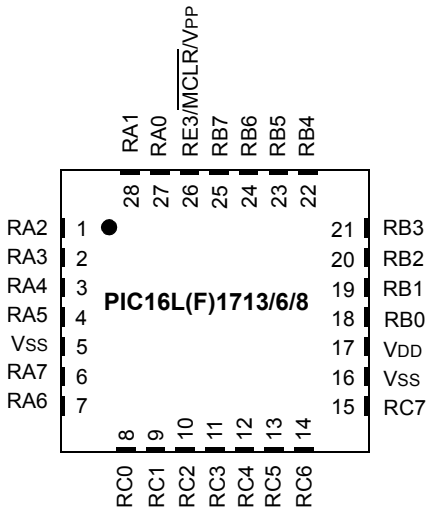
Note: See Table 3 and Table 4 for the pin allocation tables.

PIN DIAGRAM – 28-PIN PDIP, SOIC, SSOP



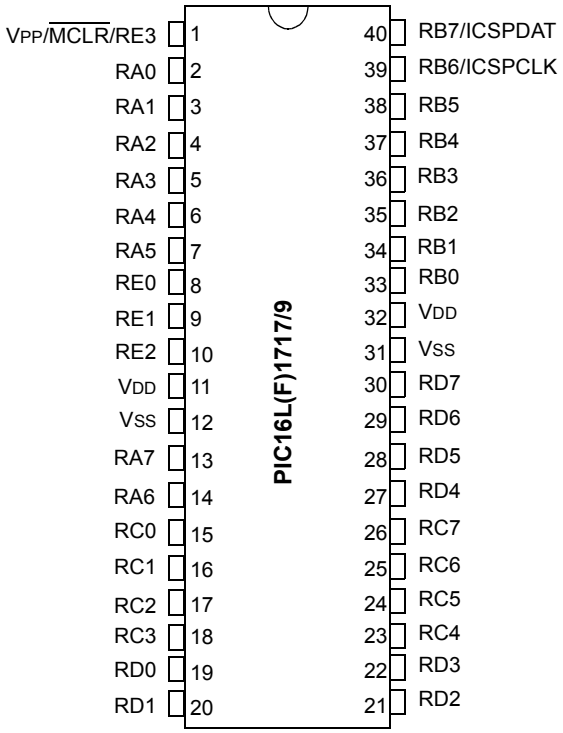
Note: See Table 5 and Table 6 for the pin allocation table.

PIN DIAGRAM – 28-PIN (U)QFN



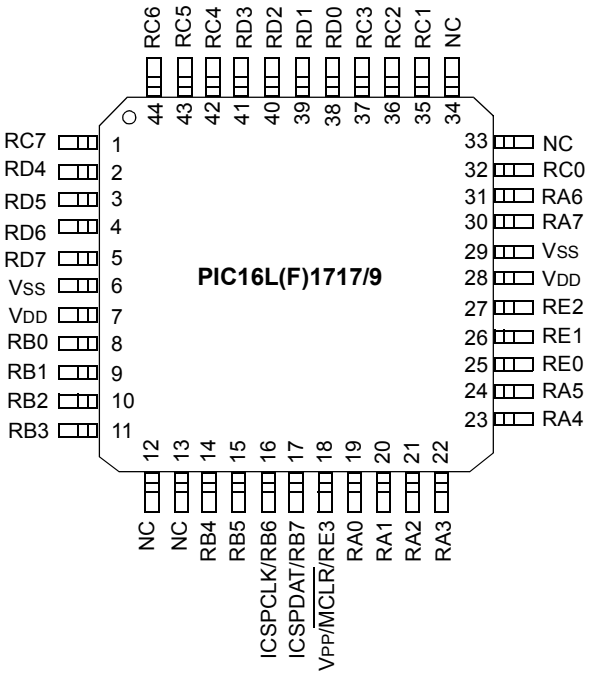
Note: See Table 5 and Table 6 for the pin allocation table.

PIN DIAGRAM – 40-PIN PDIP



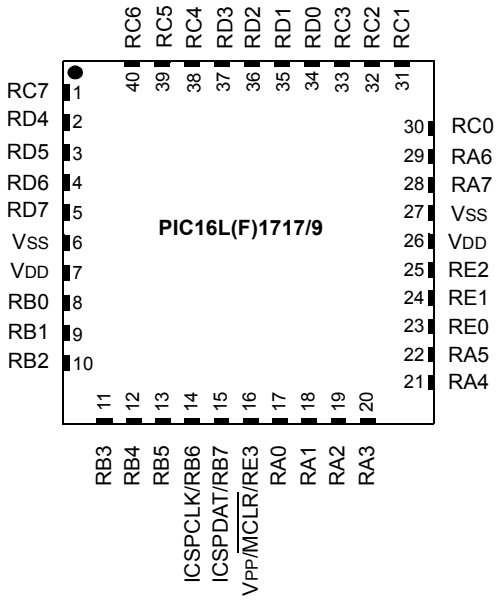
Note: See Table 7 and Table 8 for the pin allocation table.

PIN DIAGRAM – 44-PIN TQFP (10x10)



Note: See Table 7 and Table 8 for the pin allocation table.

PIN DIAGRAM – 40-PIN UQFN (5x5)



Note: See Table 7 and Table 8 for the pin allocation table.

TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1703)

I/O(2)	PDIP/SOIC/SSOP	QFN	ADC	Reference	Op Amp	Zero Cross	Timers	CCP	MSSP	CLC	Interrupt	Pull-up	Basic
RA0	13	12	AN0	VREF-	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	ZCD	T0CKI(1)	—	—	—	INT(1) IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	AN3	—	—	—	T1G(1)	—	—	—	IOC	Y	CLKOUT
RA5	2	1	—	—	—	—	T1CKI(1)	—	—	—	IOC	Y	CLKIN
RC0	10	9	AN4	—	OPA1IN+	—	—	—	SCK(1) SCL(3)	—	IOC	Y	—
RC1	9	8	AN5	—	OPA1IN-	—	—	—	SDI(1) SDA(3)	—	IOC	Y	—
RC2	8	7	AN6	—	OPA1OUT	—	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	OPA2OUT	—	—	CCP2(1)	$\overline{\text{SS}}$(1)	—	IOC	Y	—
RC4	6	5	—	—	OPA2IN-	—	—	—	—	—	IOC	Y	—
RC5	5	4	—	—	OPA2IN+	—	—	CCP1(1)	—	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	—	—	—	CPP1	SDA(3)	—	—	—	—
	—	—	—	—	—	—	—	CPP2	SCL(3) SCK	—	—	—	—
	—	—	—	—	—	—	—	—	SDO	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 2: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1704/5)

I/O(2)	PDIP/SOIC/SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	13	12	AN0	VREF-	C1IN+	—	DAC1OUT	—	—	—		—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—		—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	—	DAC1OUT2	ZCD	T0CKI(1)	—		COGIN(1)	—	—	—	INT(1) IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—		—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	AN3	—	—	—	—	—	T1G(1) SOSCO	—		—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	1	—	—	—	—	—	—	T1CKI(1) SOSCI	—		—	—	—	CLCIN3(1)	IOC	Y	CLKIN OSC1
RC0	10	9	AN4	—	C2IN+	OPA1IN+	—	—	—	—		—	SCK(1) SCL(3)	—	—	IOC	Y	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	OPA1IN-	—	—	—	—		—	SDI(1) SDA(3)	—	CLCIN2(1)	IOC	Y	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	OPA1OUT	—	—	—	—		—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	OPA2OUT	—	—	—	CCP2(1)		—	$\overline{\text{SS}}$(1)	—	CLCIN0(1)	IOC	Y	—
RC4	6	5	—	—	—	OPA2IN-	—	—	—	—		—	—	CK(1)	CLCIN1(1)	IOC	Y	—
RC5	5	4	—	—	—	OPA2IN+	—	—	—	CCP1(1)		—	—	RX(3)	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—		—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—		—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	—	—	—	—	CPP1	PWM3OUT	COGA	SDA(3)	CK	CLC1OUT	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CPP2	PWM4OUT	COGB	SCL(3)	DT(3)	CLC2OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGC	SDO	TX	CLC3OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGD	SCK	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3: 20-PIN ALLOCATION TABLE (PIC16(L)F1707)

I/O(2)	PDIP/SOIC/SSOP	QFN	ADC	Reference	Op Amp	Zero Cross	Timers	CCP	MSSP	Interrupt	Pull-up	Basic
RA0	19	16	AN0	VREF-	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	15	AN1	VREF+	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	14	AN2	—	—	ZCD	T0CKI(1)	—	—	INT(1) IOC	Y	—
RA3	4	1	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$ VPP
RA4	3	20	AN3	—	—	—	T1G(1)	—	—	IOC	Y	CLKOUT
RA5	2	19	—	—	—	—	T1CKI	—	—	IOC	Y	CLKIN
RB4	13	10	AN10	—	OPA1IN-	—	—	—	SCK(1) SDA(3)	IOC	Y	—
RB5	12	9	AN11	—	OPA1IN+	—	—	—	—	IOC	Y	—
RB6	11	8	—	—	—	—	—	—	SDI(1) SCL(3)	IOC	Y	—
RB7	10	7	—	—	—	—	—	—	—	IOC	Y	—
RC0	16	13	AN4	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	—	—	—	—	—	IOC	Y	—
RC2	14	11	AN6	—	OPA1OUT	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	OPA2OUT	—	—	CCP2(1)	—	IOC	Y	—
RC4	6	3	—	—	OPA2IN-	—	—	—	—	IOC	Y	—
RC5	5	2	—	—	OPA2IN+	—	—	CCP1(1)	—	IOC	Y	—
RC6	8	5	AN8	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—
RC7	9	6	AN9	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	—	—	—	CPP1	SDA(3)	—	—	—
	—	—	—	—	—	—	—	CPP2	SCL(3) SCK	—	—	—
	—	—	—	—	—	—	—	—	SDO	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1708/9)

I/O(2)	PDIP/SOIC/SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	19	16	AN0	VREF-	C1IN+	—	DAC1OUT	—	—	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	15	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	14	AN2	—	—	—	DAC1OUT2	ZCD	T0CKI(1)	—	—	COGIN(1)	—	—	—	INT(1) IOC	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	20	AN3	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	19	—	—	—	—	—	—	T1CKI SOSCI	—	—	—	—	—	CLCIN3(1)	IOC	Y	CLKIN OSC1
RB4	13	10	AN10	—	—	OPA1IN-	—	—	—	—	—	—	SCK(1) SDA(3)	—	—	IOC	Y	—
RB5	12	9	AN11	—	—	OPA1IN+	—	—	—	—	—	—	—	RX(1) (3)		IOC	Y	—
RB6	11	8	—	—	—	—	—	—	—	—	—	—	SDI(1) SCL(3)	—	—	IOC	Y	—
RB7	10	7	—	—	—	—	—	—	—	—	—	—	—	CK(1) (3)	—	IOC	Y	—
RC0	16	13	AN4	—	C2IN+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLCIN2(1)	IOC	Y	—
RC2	14	11	AN6	—	C1IN2- C2IN2-	OPA1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	C1IN3- C2IN3-	OPA2OUT	—	—	—	CCP2(1)	—	—	—	—	CLCIN0(1)	IOC	Y	—
RC4	6	3	—	—	—	OPA2IN-	—	—	—	—	—	—	—	—	CLCIN1(1)	IOC	Y	—
RC5	5	2	—	—	—	OPA2IN+	—	—	—	CCP1(1)	—	—	—	—	—	IOC	Y	—
RC6	8	5	AN8	—	—	—	—	—	—	—	—	—	$\overline{\text{SS}}$(1)	—	—	IOC	Y	—
RC7	9	6	AN9	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

I/O[2]	PDIP/SOIC/SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
OUT[2]	—	—	—	—	C1OUT	—	—	—	—	CPP1	PWM3OUT	COGA	SDA[3]	CK	CLC1OUT	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CPP2	PWM4OUT	COGB	SCL[3]	DT	CLC2OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGC	SDO	TX	CLC3OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGD	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 5: 28-PIN ALLOCATION TABLE (PIC16L(F)1713/6/8) (PART 1)

I/O(2)	PDIP,SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	2	27	AN0		C1IN0- C2IN0-											CLCIN0(1)	IOC	Y	
RA1	3	28	AN1		C1IN1- C2IN1-	OPA1OUT										CLCIN1(1)	IOC	Y	
RA2	4	1	AN2	Vref-	C1IN0+ C2IN0+		DAC1OUT1										IOC	Y	
RA3	5	2	AN3	Vref+	C1IN1+												IOC	Y	
RA4	6	3				OPA1IN+			T0CKI(1)								IOC	Y	
RA5	7	4	AN4			OPA1IN-	DAC2OUT1							nSS(1)			IOC	Y	
RA6	10	7															IOC		OSC2 CLKOUT
RA7	9	6									NCOCLK						IOC		OSC1 CLKIN
RB0	21	18	AN12		C2IN1+			ZCD					COGIN(1)				INT(1) IOC		
RB1	22	19	AN10		C1IN3- C2IN3-	OPA2OUT											IOC		
RB2	23	20	AN8			OPA2IN-											IOC		
RB3	24	21	AN9		C1IN2- C2IN2-	OPA2IN+											IOC		
RB4	25	22	AN11														IOC	Y	
RB5	26	23	AN13						T1G(1)								IOC	Y	
RB6	27	24												SCL(1)		CLCIN2(1)	IOC	Y	ICSPCLK
RB7	28	25					DAC1OUT2 DAC2OUT2									CLCIN3(1)	IOC	Y	ICSPDAT
RC0	11	8							T1CKI(1) SOSCO								IOC	Y	
RC1	12	9							SOSCI	CCP2(1)							IOC	Y	
RC2	13	10	AN14							CCP1(1)							IOC	Y	
RC3	14	11	AN15											SCK(1)			IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

TABLE 6: 28-PIN ALLOCATION TABLE (PIC16L(F)1713/6/8) (PART 2)

I/O(2)	PDIP,SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pull-up	Basic
RC4	15	12	AN16																			SDI(1)									IOC	Y	
																						SDA(1)											
RC5	16	13	AN17																												IOC	Y	
RC6	17	14	AN18																						CK(3)						IOC	Y	
RC7	18	15	AN19																						RX(3)						IOC	Y	
RE3	1	26																															MCLR Vpp
Vdd	20	17																															Vdd
Vss	8	5																															Vss
	19	16																															
OUT(4)					C1OUT	C2OUT							CCP1	CCP2	NCOOUT	PWM3OUT	PWM4OUT	COGA	COGB	COGC	COGD	SDA(3)	SCK/SCL(3)	SDO	TX/CK	DT(3)	CLC1OUT	CLC2OUT	CLC3OUT	CLC4OUT			
IN(5)										T1G	T1CKI	T0CKI	CCP1	CCP2	NCOCLK			COGIN				SDI	SCK/SCL(3)	SS	RX(3)	CK	CLCIN0	CLCIN1	CLCIN2	CLCIN3	INT		

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

TABLE 7: PIN ALLOCATION TABLE (PIC16L(F)1717/9) (PART 1)

I/O(2)	PDIP	TQFP	UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pullup	Basic
RA0	2	19	17	AN0		C1IN0- C2IN0-											CLCIN0(1)	IOC	Y	
RA1	3	20	18	AN1		C1IN1- C2IN1-	OPA1OUT										CLCIN1(1)	IOC	Y	
RA2	4	21	19	AN2	Vref-	C1IN0+ C2IN0+		DAC1OUT1										IOC	Y	
RA3	5	22	20	AN3	Vref+	C1IN1+												IOC	Y	
RA4	6	23	21				OPA1IN+			T0CKI(1)								IOC	Y	
RA5	7	24	22	AN4			OPA1IN-	DAC2OUT1							nSS(1)			IOC	Y	
RA6	14	31	29															IOC		OSC2 CLKOUT
RA7	13	30	28									NCOCLK						IOC		OSC1 CLKIN
RB0	33	8	8	AN12		C2IN1+			ZCD					COGIN(1)				INT(1) IOC		
RB1	34	9	9	AN10		C1IN3- C2IN3-	OPA2OUT											IOC		
RB2	35	10	10	AN8			OPA2IN-											IOC		
RB3	36	11	11	AN9		C1IN2- C2IN2-	OPA2IN+											IOC		
RB4	37	14	12	AN11														IOC	Y	
RB5	38	15	13	AN13						T1G(1)								IOC	Y	
RB6	39	16	14												SCL(1)		CLCIN2(1)	IOC	Y	ICSPCLK
RB7	40	17	15					DAC1OUT2 DAC2OUT2									CLCIN3(1)	IOC	Y	ICSPDAT
RC0	15	32	30							T1CKI(1) SOSCO								IOC	Y	
RC1	16	35	31							SOSCI	CCP2(1)							IOC	Y	
RC2	17	36	32	AN14							CCP1(1)							IOC	Y	
RC3	18	37	33	AN15											SCK(1)			IOC	Y	
RC4	23	42	38	AN16											SDI(1) SDA(1)			IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

TABLE 8: PIN ALLOCATION TABLE (PIC16L(F)1717/9) (PART 2

I/O(2)	PDIP	TQFP	UQFN	ADC	Reference	Comparator		Op Amp	DAC	Zero Cross	Timers			CCP		NCO	PWM		COG				MSSP			EUSART		CLC				Interrupt	Pullup	Basic
RC5	24	43	39	AN17																												IOC	Y	
RC6	25	44	40	AN18																						CK(3)						IOC	Y	
RC7	26	1	1	AN19																						RX(3)						IOC	Y	
RD0	19	38	34	AN20																														
RD1	20	39	35	AN21																														
RD2	21	40	36	AN22																														
RD3	22	41	37	AN23																														
RD4	27	2	2	AN24																														
RD5	28	3	3	AN25																														
RD6	29	4	4	AN26																														
RD7	30	5	5																															
RE0	8	25	23	AN5																														
RE1	9	26	24	AN6																														
RE2	10	27	25	AN7																														
RE3	1	18	16																															MCLR Vpp
Vdd	11	7	7																															Vdd
	32	28	26																															
Vss	12	6	6																															Vss
	31	29	27																															
OUT(4)						C1OUT	C2OUT							CCP1	CCP2	NCOOUT	PWM3OUT	PWM4OUT	COGA	COGB	COGC	COGD	SDA(3)	SCK/SCL(3)	SDO	TX/CK	DT (3)	CLC1OUT	CLC2OUT	CLC3OUT	CLC4OUT			
IN(5)											T1G	T1CKI	T0CKI	CCP1	CCP2	NCOCLK			COGIN				SDI	SCK/SCL(3)	SS	RX (3)	CK	CLCIN0	CLCIN1	CLCIN2	CLCIN3	INT		

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

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