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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8147vpye

- Two Serial Communication Interfaces (SCIs), each with two pins (or four additional GPIO lines)
- Up to two Serial Peripheral Interfaces (SPIs), both with configurable 4-pin port (or eight additional GPIO lines)
  - In the 56F8347, SPI1 can also be used as Quadrature Decoder 1 or Quad Timer B
  - In the 56F8147, SPI1 can alternately be used only as GPIO
- Computer Operating Properly (COP) / Watchdog timer
- Two dedicated external interrupt pins
- Up to 76 General Purpose I/O (GPIO) pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop (PLL)-based frequency synthesizer for the core clock

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories; can be disabled
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 Device Description

The 56F8347 and 56F8147 are members of the 56800E core-based family of controllers. Each combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8347 and 56F8147 are well-suited for many applications. The device includes many peripherals that are especially useful for motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, *automotive* control (56F8347 only), engine management, noise suppression, remote utility metering, industrial control for power, lighting, and automation applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The 56F8347 and 56F8147 support program execution from internal or external memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. These devices also provide two external dedicated interrupt lines and up to 76 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
GPIOD0 **($\overline{\text{CS2}}$)**	55	P6	Input/ Output Output	Input, pull-up enabled	**Port D GPIO** — These six GPIO pins can be individually programmed as input or output pins. **Chip Select** — $\overline{\text{CS2}}$ - $\overline{\text{CS7}}$ may be programmed within the EMI module to act as chip selects for specific areas of the external memory map. Depending upon the state of the DRV bit in the EMI Bus Control Register (BCR), $\overline{\text{CS2}}$ - $\overline{\text{CS7}}$ are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. At reset, these pins are configured as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOD_PUR register. Example: GPIOD0, clear bit 0 in the GPIOD_PUR register.
GPIOD1 ($\overline{\text{CS3}}$)	56	L6			
GPIOD2 ($\overline{\text{CS4}}$)	57	K6			
GPIOD3 ($\overline{\text{CS5}}$)	58	N7			
GPIOD4 ($\overline{\text{CS6}}$)	59	P7			
GPIOD5 ($\overline{\text{CS7}}$)	60	L7			
TXD0 **(GPIOE0)**	4	B1	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI0 transmit data output **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOE_PUR register.
RXD0 **(GPIOE1)**	5	D2	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI0 receive data input **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
$\overline{\text{TRST}}$	136	D9	Schmitt Input	Input, pulled high internally	**Test Reset** — As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and the JTAG/EOnCE module must not be reset. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
PHASEA0 **(TA0)** **(GPIOC4)**	155	A2	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Phase A** — Quadrature Decoder 0, PHASEA input **TA0** — Timer A, Channel 0 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is PHASEA0. To deactivate the internal pull-up resistor, clear bit 4 of the GPIOC_PUR register.
PHASEB0 **(TA1)** **(GPIOC5)**	156	B4	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Phase B** — Quadrature Decoder 0, PHASEB input **TA1** — Timer A, Channel **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is PHASEB0. To deactivate the internal pull-up resistor, clear bit 5 of the GPIOC_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
INDEX0 **(TA2)** **(GPOPC6)**	157	A1	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Index** — Quadrature Decoder 0, INDEX input **TA2** — Timer A, Channel 2 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is INDEX0. To deactivate the internal pull-up resistor, clear bit 6 of the GPIOC_PUR register.
HOME0 **(TA3)** **(GPIOC7)**	158	B3	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input **TA3** — Timer A, Channel 3 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is HOME0. To deactivate the internal pull-up resistor, clear bit 7 of the GPIOC_PUR register.
SCLK0 **(GPIOE4)**	146	A6	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOE_PUR register.

parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

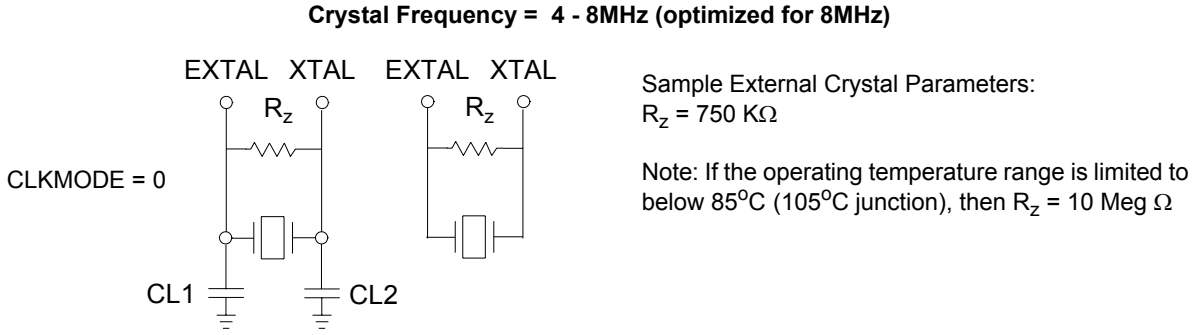

Figure 3-2 Connecting to a Crystal Oscillator

Note: The OCCS_COHL bit must be set to 1 when a crystal oscillator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User's Manual**.

3.2.2 Ceramic Resonator (Default)

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-3**. Refer to the supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as near as possible to the EXTAL and XTAL pins.

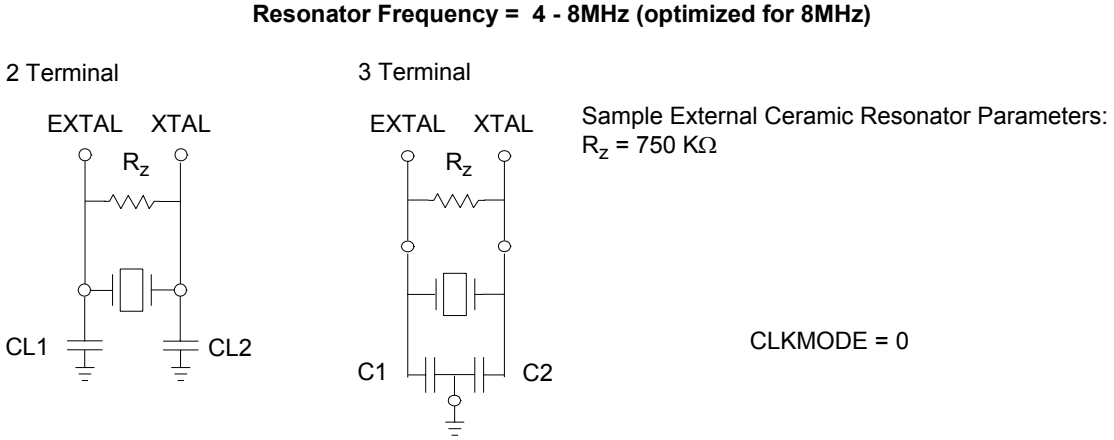

Figure 3-3 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a ceramic resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User's Manual**.

Table 4-5 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
GPIOD	32	0-2	P:$40	GPIOD
GPIOC	33	0-2	P:$42	GPIOC
GPIOB	34	0-2	P:$44	GPIOB
GPIOA	35	0-2	P:$46	GPIOA
				Reserved
SPI1	38	0-2	P:$4C	SPI 1 Receiver Full
SPI1	39	0-2	P:$4E	SPI 1 Transmitter Empty
SPI0	40	0-2	P:$50	SPI 0 Receiver Full
SPI0	41	0-2	P:$52	SPI 0 Transmitter Empty
SCI1	42	0-2	P:$54	SCI 1 Transmitter Empty
SCI1	43	0-2	P:$56	SCI 1 Transmitter Idle
				Reserved
SCI1	45	0-2	P:$5A	SCI 1 Receiver Error
SCI1	46	0-2	P:$5C	SCI 1 Receiver Full
DEC1	47	0-2	P:$5E	Quadrature Decoder #1 Home Switch or Watchdog
DEC1	48	0-2	P:$60	Quadrature Decoder #1 INDEX Pulse
DEC0	49	0-2	P:$62	Quadrature Decoder #0 Home Switch or Watchdog
DEC0	50	0-2	P:$64	Quadrature Decoder #0 INDEX Pulse
				Reserved
TMRD	52	0-2	P:$68	Timer D, Channel 0
TMRD	53	0-2	P:$6A	Timer D, Channel 1
TMRD	54	0-2	P:$6C	Timer D, Channel 2
TMRD	55	0-2	P:$6E	Timer D, Channel 3
TMRC	56	0-2	P:$70	Timer C, Channel 0
TMRC	57	0-2	P:$72	Timer C, Channel 1
TMRC	58	0-2	P:$74	Timer C, Channel 2
TMRC	59	0-2	P:$76	Timer C, Channel 3
TMRB	60	0-2	P:$78	Timer B, Channel 0
TMRB	61	0-2	P:$7A	Timer B, Channel 1
TMRB	62	0-2	P:$7C	Timer B, Channel 2
TMRB	63	0-2	P:$7E	Timer B, Channel 3
TMRA	64	0-2	P:$80	Timer A, Channel 0
TMRA	65	0-2	P:$82	Timer A, Channel 1
TMRA	66	0-2	P:$84	Timer A, Channel 2
TMRA	67	0-2	P:$86	Timer A, Channel 3

Table 4-10 External Memory Integration Registers Address Map (Continued) (EMI_BASE = $00 F020)

Register Acronym	Address Offset	Register Description	Reset Value
CSOR 4	$C	Chip Select Option Register 4	
CSOR 5	$D	Chip Select Option Register 5	
CSOR 6	$E	Chip Select Option Register 6	
CSOR 7	$F	Chip Select Option Register 7	
CSTC 0	$10	Chip Select Timing Control Register 0	
CSTC 1	$11	Chip Select Timing Control Register 1	
CSTC 2	$12	Chip Select Timing Control Register 2	
CSTC 3	$13	Chip Select Timing Control Register 3	
CSTC 4	$14	Chip Select Timing Control Register 4	
CSTC 5	$15	Chip Select Timing Control Register 5	
CSTC 6	$16	Chip Select Timing Control Register 6	
CSTC 7	$17	Chip Select Timing Control Register 7	
BCR	$18	Bus Control Register	0x016B sets the default number of wait states to 11 for both read and write accesses

Table 4-11 Quad Timer A Registers Address Map (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMP1	$0	Compare Register 1
TMRA0_CMP2	$1	Compare Register 2
TMRA0_CAP	$2	Capture Register
TMRA0_LOAD	$3	Load Register
TMRA0_HOLD	$4	Hold Register
TMRA0_CNTR	$5	Counter Register
TMRA0_CTRL	$6	Control Register
TMRA0_SCR	$7	Status and Control Register
TMRA0_CMPLD1	$8	Comparator Load Register 1
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_COMSCR	$A	Comparator Status and Control Register
		Reserve
TMRA1_CMP1	$10	Compare Register 1
TMRA1_CMP2	$11	Compare Register 2
TMRA1_CAP	$12	Capture Register
TMRA1_LOAD	$13	Load Register

Table 4-17 Quadrature Decoder 0 Registers Address Map (DEC0_BASE = $00 F180)

Register Acronym	Address Offset	Register Description
DEC0_DECCR	$0	Decoder Control Register
DEC0_FIR	$1	Filter Interval Register
DEC0_WTR	$2	Watchdog Time-out Register
DEC0_POSD	$3	Position Difference Counter Register
DEC0_POSDH	$4	Position Difference Counter Hold Register
DEC0_REV	$5	Revolution Counter Register
DEC0_REVH	$6	Revolution Hold Register
DEC0_UPOS	$7	Upper Position Counter Register
DEC0_LPOS	$8	Lower Position Counter Register
DEC0_UPOSH	$9	Upper Position Hold Register
DEC0_LPOSH	$A	Lower Position Hold Register
DEC0_UIR	$B	Upper Initialization Register
DEC0_LIR	$C	Lower Initialization Register
DEC0_IMR	$D	Input Monitor Register

Table 4-18 Quadrature Decoder 1 Registers Address Map (DEC1_BASE = $00 190)

Quadrature Decoder 1 is NOT available in the 56F8147 device

Register Acronym	Address Offset	Register Description
DEC1_DECCR	$0	Decoder Control Register
DEC1_FIR	$1	Filter Interval Register
DEC1_WTR	$2	Watchdog Time-out Register
DEC1_POSD	$3	Position Difference Counter Register
DEC1_POSDH	$4	Position Difference Counter Hold Register
DEC1_REV	$5	Revolution Counter Register
DEC1_REVH	$6	Revolution Hold Register
DEC1_UPOS	$7	Upper Position Counter Register
DEC1_LPOS	$8	Lower Position Counter Register
DEC1_UPOSH	$9	Upper Position Hold Register
DEC1_LPOSH	$A	Lower Position Hold Register
DEC1_UIR	$B	Upper Initialization Register
DEC1_LIR	$C	Lower Initialization Register
DEC1_IMR	$D	Input Monitor Register

Table 4-19 Interrupt Control Registers Address Map (ITCN_BASE = $00 F1A0)

Register Acronym	Address Offset	Register Description
IPR 0	$0	Interrupt Priority Register 0
IPR 1	$1	Interrupt Priority Register 1
IPR 2	$2	Interrupt Priority Register 2
IPR 3	$3	Interrupt Priority Register 3
IPR 4	$4	Interrupt Priority Register 4
IPR 5	$5	Interrupt Priority Register 5
IPR 6	$6	Interrupt Priority Register 6
IPR 7	$7	Interrupt Priority Register 7
IPR 8	$8	Interrupt Priority Register 8
IPR 9	$9	Interrupt Priority Register 9
VBA	$A	Vector Base Address Register
FIM0	$B	Fast Interrupt Match Register 0
FIVAL0	$C	Fast Interrupt Vector Address Low 0 Register
FIVAH0	$D	Fast Interrupt Vector Address High 0 Register
FIM1	$E	Fast Interrupt Match Register 1
FIVAL1	$F	Fast Interrupt Vector Address Low 1 Register
FIVAH1	$10	Fast Interrupt Vector Address High 1 Register
IRQP 0	$11	IRQ Pending Register 0
IRQP 1	$12	IRQ Pending Register 1
IRQP 2	$13	IRQ Pending Register 2
IRQP 3	$14	IRQ Pending Register 3
IRQP 4	$15	IRQ Pending Register 4
IRQP 5	$16	IRQ Pending Register 5
		Reserved
ICTL	$1D	Interrupt Control Register

Table 4-20 Analog-to-Digital Converter Registers Address Map (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_CR 1	$0	Control Register 1
ADCA_CR 2	$1	Control Register 2
ADCA_ZCC	$2	Zero Crossing Control Register

Table 4-24 Serial Communication Interface 1 Registers Address Map (SCI1_BASE = $00 F290)

Register Acronym	Address Offset	Register Description
SCI1_SCIBR	$0	Baud Rate Register
SCI1_SCICR	$1	Control Register
		Reserved
SCI1_SCISR	$3	Status Register
SCI1_SCIDR	$4	Data Register

Table 4-25 Serial Peripheral Interface 0 Registers Address Map (SPI0_BASE = $00 F2A0)

Register Acronym	Address Offset	Register Description
SPI0_SPSCR	$0	Status and Control Register
SPI0_SPDSR	$1	Data Size Register
SPI0_SPDRR	$2	Data Receive Register
SPI0_SPDTR	$3	Data Transmitter Register

Table 4-26 Serial Peripheral Interface 1 Registers Address Map (SPI1_BASE = $00 F2B0)

Register Acronym	Address Offset	Register Description
SPI1_SPSCR	$0	Status and Control Register
SPI1_SPDSR	$1	Data Size Register
SPI1_SPDRR	$2	Data Receive Register
SPI1_SPDTR	$3	Data Transmitter Register

Table 4-27 Computer Operating Properly Registers Address Map (COP_BASE = $00 F2C0)

Register Acronym	Address Offset	Register Description
COPCTL	$0	Control Register
COPTO	$1	Time Out Register
COPCTR	$2	Counter Register

Table 4-32 GPIOD Registers Address Map (GPIOD_BASE = $00 F320)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOD_PUR	$0	Pull-up Enable Register	0 x 1FFF
GPIOD_DR	$1	Data Register	0 x 0000
GPIOD_DDR	$2	Data Direction Register	0 x 0000
GPIOD_PER	$3	Peripheral Enable Register	0 x 1FC0
GPIOD_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOD_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOD_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOD_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOD_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOD_PPMODE	$9	Push-Pull Mode Register	0 x 1FFF
GPIOD_RAWDATA	$A	Raw Data Input Register	—

Table 4-33 GPIOE Registers Address Map (GPIOE_BASE = $00 F330)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOE_PUR	$0	Pull-up Enable Register	0 x 3FFF
GPIOE_DR	$1	Data Register	0 x 0000
GPIOE_DDR	$2	Data Direction Register	0 x 0000
GPIOE_PER	$3	Peripheral Enable Register	0 x 3FFF
GPIOE_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOE_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOE_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOE_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOE_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOE_PPMODE	$9	Push-Pull Mode Register	0 x 3FFF
GPIOE_RAWDATA	$A	Raw Data Input Register	—

5.6.10.3 Reload PWM A Interrupt Priority Level (PWMA_RL IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.4 Reload PWM B Interrupt Priority Level (PWMB_RL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.5 ADC A Zero Crossing or Limit Error Interrupt Priority Level (ADCA_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.6 ADC B Zero Crossing or Limit Error Interrupt Priority Level (ADCB_ZC IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.7
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.8
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.9
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_ CONTROL	R	0	0	0	0	0	0	0	0	0	EMI_ MODE	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
		W																
$1	SIM_ RSTSTS	R	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
		W																
$2	SIM_SCR0	R	FIELD															
		W																
$3	SIM_SCR1	R	FIELD															
		W																
$4	SIM_SCR2	R	FIELD															
		W																
$5	SIM_SCR3	R	FIELD															
		W																
$6	SIM_MSH_ ID	R	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
		W																
$7	SIM_LSH_ID	R	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PUDR	R	0	PWMA 1	CAN	EMI_ MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA 0	DATA	CTRL	ADR	JTAG	TMRD	TMRC	TMRA
		W																
	Reserved																	
$A	SIM_ CLKOSR	R	0	0	0	0	0	0	$\overline{\text{A23}}$	$\overline{\text{A22}}$	$\overline{\text{A21}}$	$\overline{\text{A20}}$	CLKDIS	CLKOSEL				
		W																
$B	SIM_GPS	R	0	0	0	0	0	0	0	0	0	0	0	0	C3	C2	C1	C0
		W																
$C	SIM_PCE	R	EMI	ADCB	ADCA	CAN	DEC1	DEC0	TMRD	TMRC	TMRB	TMRA	SCI1	SCI0	SPI1	SPI0	PWM B	PWM A
		W																
$D	SIM_ISALH	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
		W																
$E	SIM_ISALL	R	ISAL[21:6]															
		W																

= Reserved

Figure 6-2 SIM Register Map Summary

6.5.1 SIM Control Register (SIM_CONTROL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	EMI_ MODE	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-3 SIM Control Register (SIM_CONTROL)

6.5.1.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.10 I/O Short Address Location Register (SIM_ISALH and SIM_ISALL)

The I/O Short Address Location registers are used to specify the memory referenced via the I/O short address mode. The I/O short address mode allows the instruction to specify the lower six bits of address; the upper address bits are not directly controllable. This register set allows limited control of the full address, as shown in Figure 6-13.

Note: If this register is set to something other than the top of memory (EOnCE register space) and the EX bit in the OMR is set to 1, the JTAG port cannot access the on-chip EOnCE registers, and debug functions will be affected.

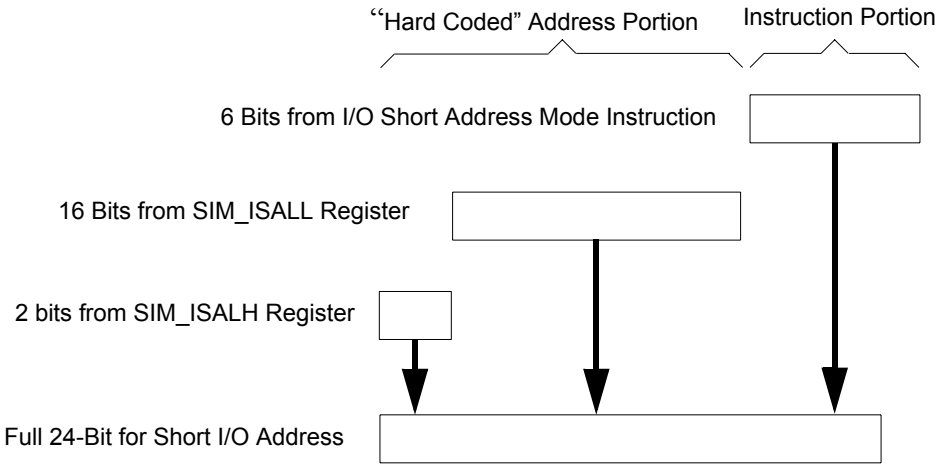

Figure 6-13 I/O Short Address Determination

With this register set, an interrupt driver can set the SIM_ISALL register pair to point to its peripheral registers and then use the I/O Short addressing mode to reference them. The ISR should restore this register to its previous contents prior to returning from interrupt.

Note: The default value of this register set points to the EOnCE registers.

Note: The pipeline delay between setting this register set and using short I/O addressing with the new value is three cycles.

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-14 I/O Short Address Location High Register (SIM_ISALH)

6.5.10.1 Input/Output Short Address Low (ISAL[23:22])—Bit 1–0

This field represents the upper two address bits of the "hard coded" I/O short address.

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

6.8 Stop and Wait Mode Disable Function

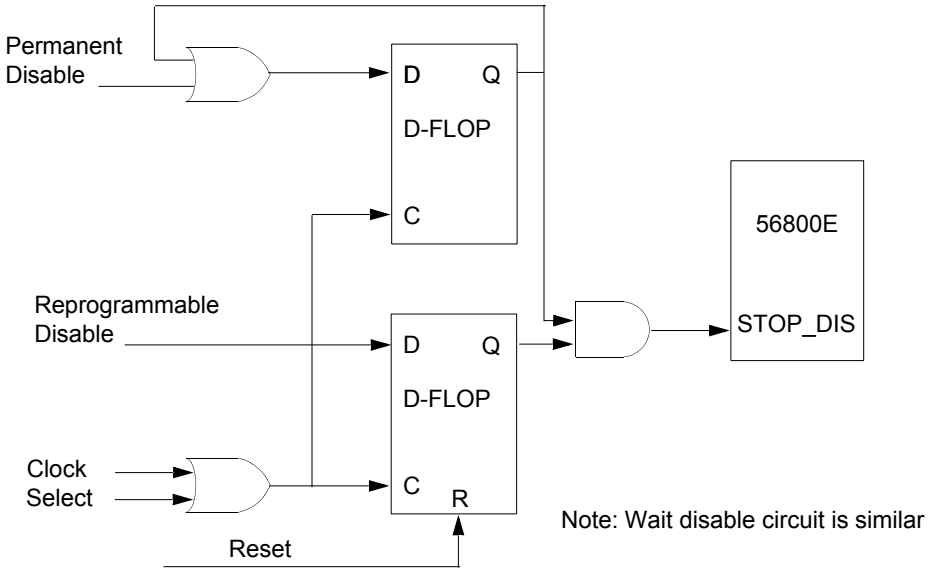

Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the oscillator output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL), described in **Part 6.5.1**. This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing to the SIM_CONTROL register and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is first extended for 2^{21} clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and,

Table 8-1 56F8347 GPIO Ports Configuration (Continued)

GPIO Port	Port Width	Available Pins in 56F8347	Peripheral Function	Reset Function
D	13	13	6 pins - EMI $\overline{CSn}$ 2 pins - SCI1___ 2 pins - EMI $\overline{CSn}$ 3 pins -PWMB current sense	EMI Chip Selects SCI1 EMI Chip Selects PWMB current sense
E	14	14	2 pins - SCI0 2 pins - EMI Address pins 4 pins - SPI0 2 pins - TMRC 4 pins - TMRD	SCI0 EMI Address SPI0 TMRC TMRD
F	16	16	16 pins - EMI Data	EMI Data

Table 8-2 56F8147 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8147	Peripheral Function	Reset Function
A	14	14	14 pins - EMI Address pins	EMI Address
B	8	8	8 pins - EMI Address pins	EMI Address
C	11	11	4 pins - SPI1 4 pins - DEC0 / TMRA 3 pins - Dedicated GPIO	SPI1 DEC0 / TMRA GPIO
D	13	13	6 pins - EMI $\overline{CSn}$ 2 pins - SCI1___ 2 pins - EMI $\overline{CSn}$ 3 pins -PWMB current sense	EMI Chip Selects SCI1 EMI Chip Selects PWMB current sense
E	14	14	2 pins - SCI0 2 pins - EMI Address pins 4 pins - SPI0 2 pins - TMRC 4 pins - Dedicated GPIO	SCI0 EMI Address SPI0 TMRC GPIO
F	16	16	16 pins - EMI Data	EMI Data

Note: *The 56F8147 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8147 device.*

Table 10-1 Absolute Maximum Ratings

(V_{SS} = V_{SSA_ADC} = 0)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage	V_{DD_IO}		-0.3	4.0	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	-0.3	4.0	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		-0.3	4.0	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	-0.3	3.0	V
Input Voltage (digital)	V_{IN}	Pin Groups 1, 2, 5, 6, 9, 10	-0.3	6.0	V
Input Voltage (analog)	V_{INA}	Pin Groups 11, 12, 13	-0.3	4.0	V
Output Voltage	V_{OUT}	Pin Groups 1, 2, 3, 5, 6, 7, 8	-0.3	4.0 6.0[1]	V
Output Voltage (open drain)	V_{OD}	Pin Group 4	-0.3	6.0	V
Ambient Temperature (Automotive)	T_A		-40	125	°C
Ambient Temperature (Industrial)	T_A		-40	105	°C
Junction Temperature (Automotive)	T_J		-40	150	°C
Junction Temperature (Industrial)	T_J		-40	125	°C
Storage Temperature (Automotive)	T_{STG}		-55	150	°C
Storage Temperature (Industrial)	T_{STG}		-55	150	°C

1. If corresponding GPIO pin is configured as open drain.

Note: *Pins in italics are NOT available in the 56F8147 device.*

Pin Group 1: TXD0-1, RXD0-1, $\overline{SS0}$, MISO0, MOSI0
Pin Group 2: PHASEA0, *PHASEA1*, PHASEB0, *PHASEB1*, INDEX0, *INDEX1*, HOME0, *HOME1*, ISB0-2, *ISA0-2*, *TD2-3*, TC0-1, SCLK0
Pin Group 3: $\overline{RSTO}$, TDO
Pin Group 4: *CAN_TX*
Pin Group 5: A0-5, D0-15, GPIOD0-5, $\overline{PS}$, $\overline{DS}$
Pin Group 6: A6-15, GPIOB0-7, *TD0-1*
Pin Group 7: CLKO, $\overline{WR}$, $\overline{RD}$
Pin Group 8: *PWMA0-5*, PWMB0-5
Pin Group 9: $\overline{IRQA}$, $\overline{IRQB}$, $\overline{RESET}$, EXTBOOT, $\overline{TRST}$, TMS, TDI, *CAN_RX*, EMI_MODE, *FAULTA0-3*, FAULTB0-3
Pin Group 10: TCK
Pin Group 11: XTAL, EXTAL
Pin Group 12: ANA0-7, ANB0-7
Pin Group 13: OCR_DIS, CLKMODE

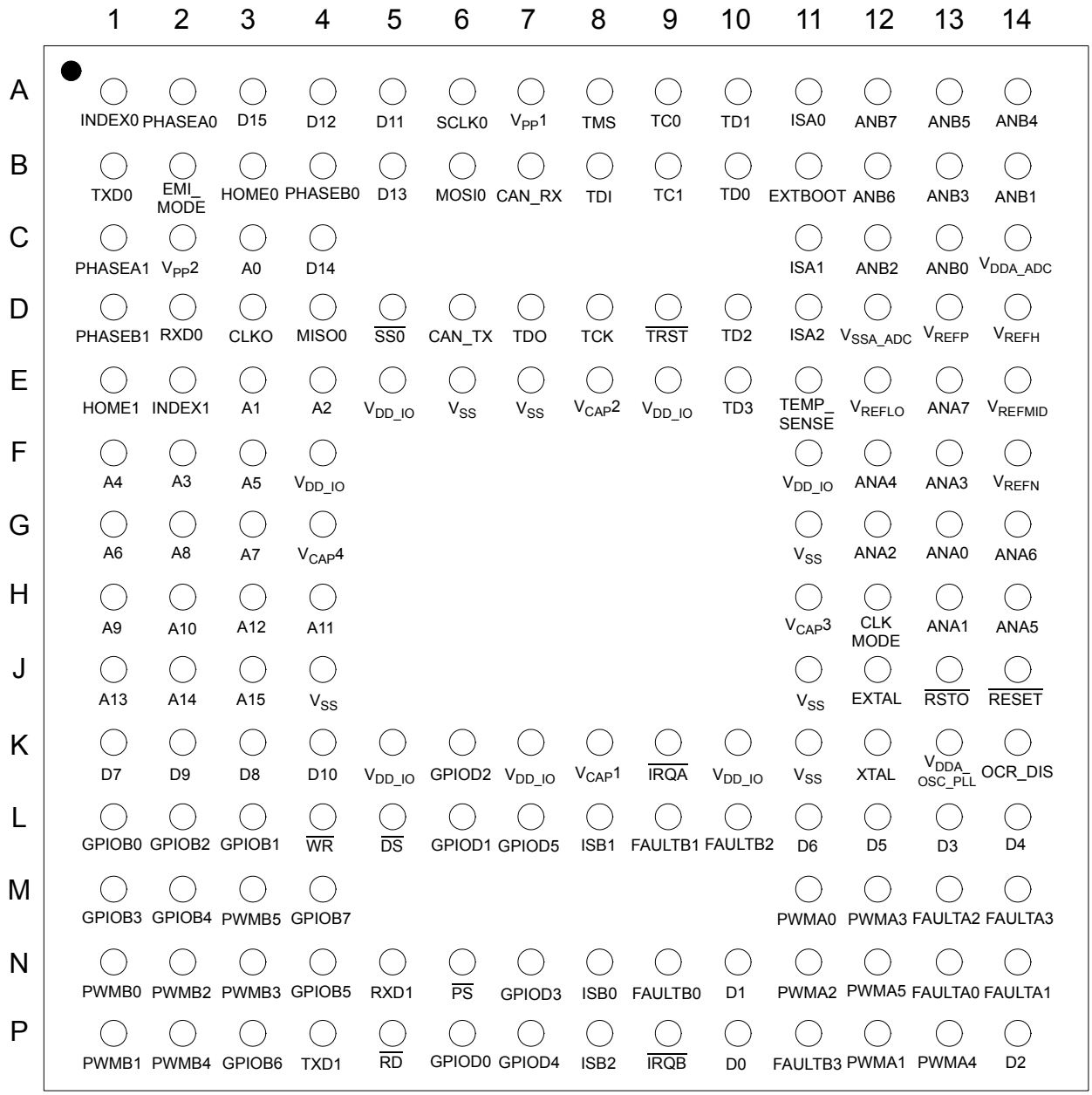

Figure 11-2 Top View, 56F8347 160-Pin MAPBGA Package

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = Package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = Package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)