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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8147vvfe

bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot Flash page erase size is 512 bytes and the Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8147 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and can also support six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8147 incorporates a Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8147.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8147 device and are shaded in the following figures.*

The 56F8347/56F8147 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories, the external memory interface and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User's Manual** for clarification on the operation of all three of these peripherals.

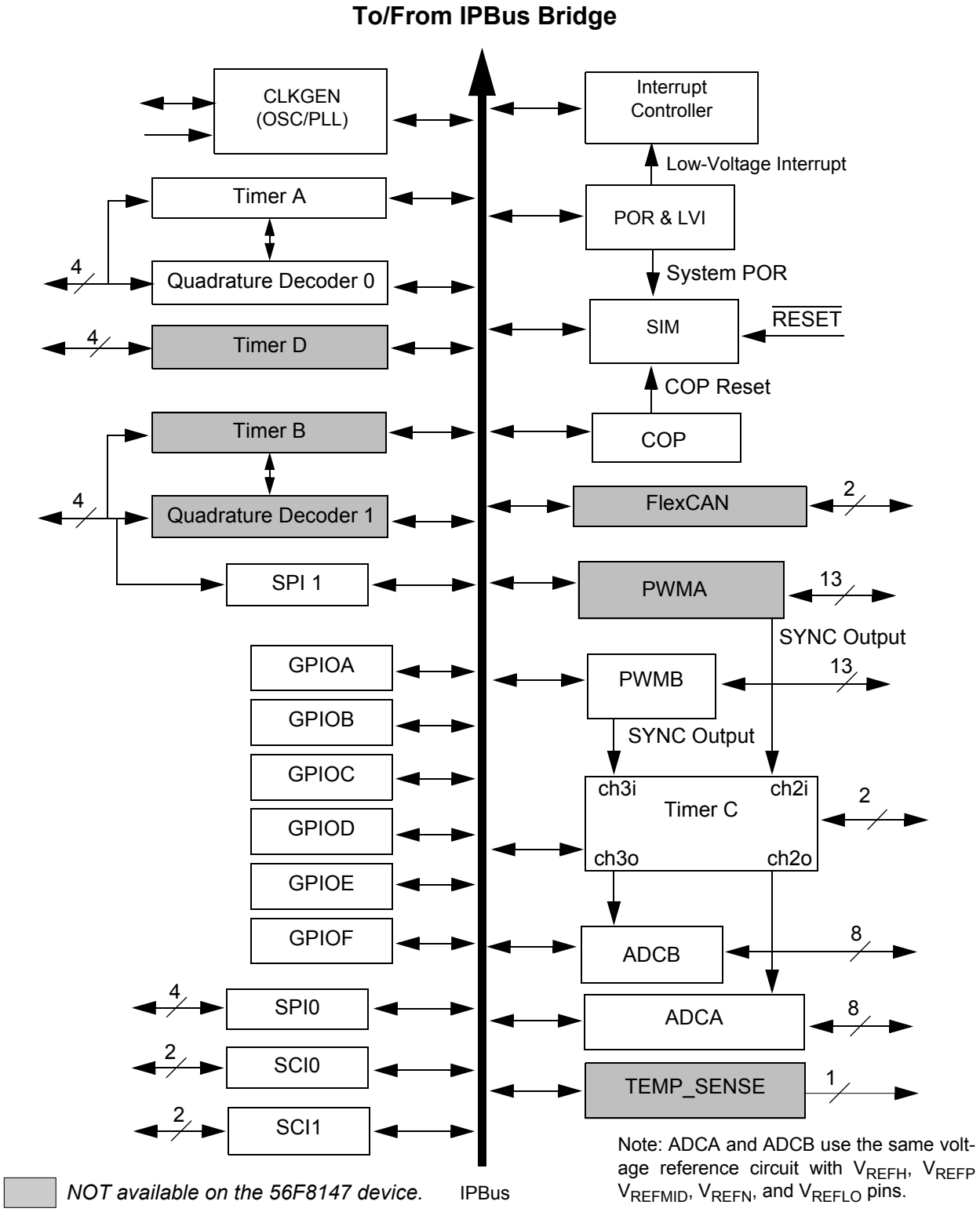


Figure 1-2 Peripheral Subsystem

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
GPIOB0 **(A16)**	33	L1	Schmitt Input/ Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be programmed as input or output pins. **Address Bus** — A16 - A19 specify one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A16 - A19 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. After reset, the startup state of GPIOB0 - GPIOB3 (GPIO or address) is determined as a function of EXTBOOT, EMI_MODE and the Flash security setting. See **Table 4-4** for further information on when this pin is configured as an address pin at reset. In all cases, this state may be changed by writing to GPIOB_PER. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOB_PUR register.
GPIOB1 **(A17)**	34	L3			
GPIOB2 **(A18)**	35	L2			
GPIOB3 **(A19)**	36	M1			
GPIOB4 **(A20)** **(prescaler_ clock)**	37	M2	Schmitt Input/ Output Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be programmed as input or output pins. **Address Bus** — A20 - A23 specify one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A20–A23 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Clock Outputs** — can be used to monitor the prescaler_clock, SYS_CLK, SYS_CLK2 or oscillator-clock on GPIOB4 through GPIOB7, respectively. After reset, the default state is GPIO. These pins can also be used to extend the external address bus to its full length or to view any of several system clocks. In these cases, the GPIO_B_PER can be used to individually disable the GPIO. The CLKOSR register in the SIM (see **Part 6.5.7**) can then be used to choose between address and clock functions.
GPIOB5 **(A21)** **(SYS_CLK)**	46	N4			
GPIOB6 **(A22)** **(SYS_CLK2)**	47	P3			
GPIOB7 **(A23)** **(oscillator_ Clock)**	48	M4			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
INDEX0 **(TA2)** **(GPOPC6)**	157	A1	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Index** — Quadrature Decoder 0, INDEX input **TA2** — Timer A, Channel 2 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is INDEX0. To deactivate the internal pull-up resistor, clear bit 6 of the GPIOC_PUR register.
HOME0 **(TA3)** **(GPIOC7)**	158	B3	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input **TA3** — Timer A, Channel 3 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is HOME0. To deactivate the internal pull-up resistor, clear bit 7 of the GPIOC_PUR register.
SCLK0 **(GPIOE4)**	146	A6	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
TD0 **(GPIOE10)**	129	B10	Schmitt Input/ Output	Input, pull-up enabled	**TD0 - 3** — Timer D, Channels 0, 1, 2 and 3 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOE_PUR register. See **Part 6.5.6** for details.
TD1 **(GPIOE11)**	130	A10	Schmitt Input/ Output		
TD2 **(GPIOE12)**	131	D10			
TD3 **(GPIOE13)**	132	E10			
$\overline{\text{IRQA}}$	65	K9	Schmitt Input	Input, pull-up enabled	**External Interrupt Request A and B** — The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests during Stop and Wait mode operation. During other operating modes, they are synchronized external interrupt requests, which indicate an external device is requesting service. They can be programmed to be level-sensitive or negative-edge triggered. To deactivate the internal pull-up resistor, set the IRQ bit in the SIM_PUDR register. See **Part 6.5.6** for details.
$\overline{\text{IRQB}}$	66	P9			
$\overline{\text{RESET}}$	98	J14	Schmitt Input	Input, pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and the JTAG/EOnCE module must not be reset. In this case, assert $\overline{\text{RESET}}$ but do not assert $\overline{\text{TRST}}$. **Note:** The internal Power-On Reset will assert on initial power-up. To deactivate the internal pull-up resistor, set the $\overline{\text{RESET}}$ bit in the SIM_PUDR register. See **Part 6.5.6** for details.
$\overline{\text{RSTO}}$	97	J13	Output	Output	**Reset Output** — This output reflects the internal reset state of the chip.

Table 4-9 Data Memory Peripheral Base Address Map Summary (Continued)

Peripheral	Prefix	Base Address	Table Number
GPIO Port F	GPIOF	X:$00 F340	4-34
SIM	SIM	X:$00 F350	4-35
Power Supervisor	LVI	X:$00 F360	4-36
FM	FM	X:$00 F400	4-37
FlexCAN	FC	X:$00 F800	4-38

Table 4-10 External Memory Integration Registers Address Map (EMI_BASE = $00 F020)

Register Acronym	Address Offset	Register Description	Reset Value
CSBAR 0	$0	Chip Select Base Address Register 0	0x0004 = 64K when EXT_BOOT = 0 or EMI_MODE = 0 0x0008 = 1M when EMI_MODE = 1 (Selects entire program space for CS0)
CSBAR 1	$1	Chip Select Base Address Register 1	0x0004 = 64K when EXT_BOOT = 0 0x0008 = 1M when EMI_MODE = 1 (Selects A0 - A19 addressable data space for CS1)
CSBAR 2	$2	Chip Select Base Address Register 2	
CSBAR 3	$3	Chip Select Base Address Register 3	
CSBAR 4	$4	Chip Select Base Address Register 4	
CSBAR 5	$5	Chip Select Base Address Register 5	
CSBAR 6	$6	Chip Select Base Address Register 6	
CSBAR 7	$7	Chip Select Base Address Register 7	
CSOR 0	$8	Chip Select Option Register 0	0x5FCB programmed for chip select for program space, word wide, read and write, 11 waits
CSOR 1	$9	Chip Select Option Register 1	0x5FAB programmed for chip select for data space, word wide, read and write, 11 waits
CSOR 2	$A	Chip Select Option Register 2	
CSOR 3	$B	Chip Select Option Register 3	

Table 4-32 GPIOD Registers Address Map (GPIOD_BASE = $00 F320)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOD_PUR	$0	Pull-up Enable Register	0 x 1FFF
GPIOD_DR	$1	Data Register	0 x 0000
GPIOD_DDR	$2	Data Direction Register	0 x 0000
GPIOD_PER	$3	Peripheral Enable Register	0 x 1FC0
GPIOD_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOD_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOD_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOD_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOD_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOD_PPMODE	$9	Push-Pull Mode Register	0 x 1FFF
GPIOD_RAWDATA	$A	Raw Data Input Register	—

Table 4-33 GPIOE Registers Address Map (GPIOE_BASE = $00 F330)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOE_PUR	$0	Pull-up Enable Register	0 x 3FFF
GPIOE_DR	$1	Data Register	0 x 0000
GPIOE_DDR	$2	Data Direction Register	0 x 0000
GPIOE_PER	$3	Peripheral Enable Register	0 x 3FFF
GPIOE_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOE_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOE_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOE_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOE_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOE_PPMODE	$9	Push-Pull Mode Register	0 x 3FFF
GPIOE_RAWDATA	$A	Raw Data Input Register	—

5.6.4.2 GPIOE Interrupt Priority Level (GPIOE IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.3 GPIOF Interrupt Priority Level (GPIOF IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.4 FlexCAN Message Buffer Interrupt Priority Level (FCMSGBUF IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.5 FlexCAN Wake Up Interrupt Priority Level (FCWKUP IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.6 FlexCAN Error Interrupt Priority Level (FCERR IPL)— Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7 Interrupt Priority Register 6 (IPR6)

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-9 Interrupt Priority Register 6 (IPR6)

5.6.7.1 Timer C, Channel 0 Interrupt Priority Level (TMRC0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.2 Timer D, Channel 3 Interrupt Priority Level (TMRD3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.3 Timer D, Channel 2 Interrupt Priority Level (TMRD2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 Timer D, Channel 1 Interrupt Priority Level (TMRD1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.2 SCI0 Receiver Error Interrupt Priority Level (SCI0_RERR IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.3 Reserved—Bits 11–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.9.4 SCI0 Transmitter Idle Interrupt Priority Level (SCI0_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.5 SCI0 Transmitter Empty Interrupt Priority Level (SCI0_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.6 Timer A, Channel 3 Interrupt Priority Level (TMRA3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant unspecified latencies at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, [A23:20], or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between [A23:20] and additional clock outputs is done here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as [A23:20]. This can be changed by altering [A23:20] as shown in **Figure 6-9**.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	A23	A22	A21	A20	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 Alternate GPIOB Peripheral Function for A23 (A23)—Bit 9

- 0 = Peripheral output function of GPIOB7 is defined to be A23
- 1 = Peripheral output function of GPIOB7 is defined to be the oscillator_clock (MSTR_OSC, see **Figure 3-4**)

6.5.7.3 Alternate GPIOB Peripheral Function for A22 (A22)—Bit 8

- 0 = Peripheral output function of GPIOB6 is defined to be A22
- 1 = Peripheral output function of GPIOB6 is defined to be SYS_CLK2

6.5.7.4 Alternate GPIOB Peripheral Function for A21 (A21)—Bit 7

- 0 = Peripheral output function of GPIOB5 is defined to be A21
- 1 = Peripheral output function of GPIOB5 is defined to be SYS_CLK

6.5.7.5 Alternate GPIOB Peripheral Function for A20 (A20)—Bit 6

- 0 = Peripheral output function of GPIOB4 is defined to be A20
- 1 = Peripheral output function of GPIOB4 is defined to be the prescaler_clock (FREF in **Figure 3-4**)

6.5.7.6 Clockout Disable (CLKDIS)—Bit 5

- 0 = CLKOUT output is enabled and will output the signal indicated by CLKOSEL
- 1 = CLKOUT is tri-stated

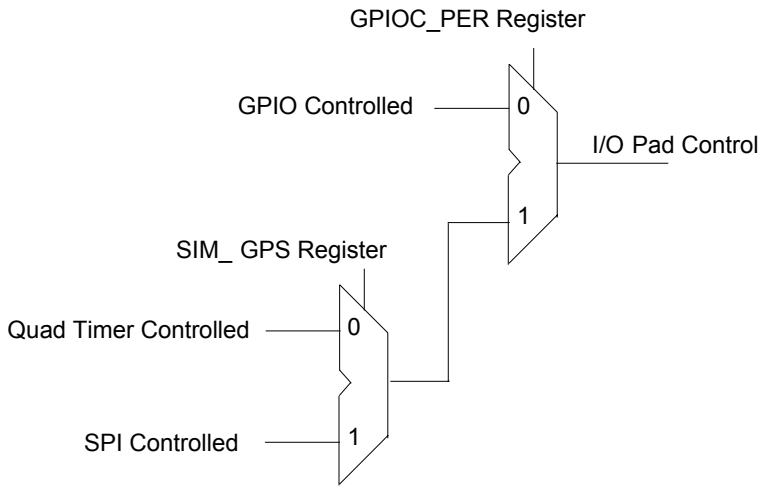


Figure 6-10 Overall Control of Pads Using SIM_GPS Control

Table 6-2 Control of Pads Using SIM_GPS Control [1]

Pin Function	Control Registers				Comments
	GPIOC_PER	GPIOC_DTR	SIM_GPS	Quad Timer SCR Register OEN bits	
GPIO Input	0	0	—	—	
GPIO Output	0	1	—	—	
Quad Timer Input / Quad Decoder Input [2]	1	—	0	0	See the “Switch Matrix for Inputs to the Timer” table in the **56F8300 Peripheral User’s Manual** for the definition of the timer inputs based on the Quad Decoder Mode configuration.
Quad Timer Output / Quad Decoder Input [3]	1	—	0	1	
SPI input	1	—	1	—	See SPI controls for determining the direction of each of the SPI pins.
SPI output	1	—	1	—	

1. This applies to the four pins that serve as Quad Decoder / Quad Timer / SPI / GPIOC functions. A separate set of control bits is used for each pin.
2. Reset configuration
3. Quad Decoder pins are always inputs and function in conjunction with the Quad Timer pins.

This security affords protection only to applications in which the device operates in internal Flash security mode. Therefore, the security feature cannot be used unless all executing code resides on-chip.

When security is enabled, any attempt to override the default internal operating mode by asserting the EXTBOOT pin in conjunction with reset will be ignored.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The $\overline{\text{TRST}}$, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register.

Proper implementation of Flash security requires that no access to the EOnCE port is provided when security is enabled. The 56800E core has an input which disables reading of internal memory via the JTAG/EOnCE. The FM sets this input at reset to a value determined by the contents of the FM security bytes.

7.2.3 Flash Lockout Recovery

If a user inadvertently enables Flash security on the device, a built-in lockout recovery mechanism can be used to reenable access to the device. This mechanism completely reases all on-chip Flash, thus disabling Flash security. Access to this recovery mechanism is built into CodeWarrior via an instruction in memory configuration (*.cfg*) files. Add, or uncomment the following configuration command:

unlock_flash_on_connect 1

For more information, please see **CodeWarrior MC56F83xx/DSP5685x Family Targeting Manual**.

The LOCKOUT_RECOVERY instruction will have an associated 7-bit Data Register (DR) that is used to control the clock divider circuit within the FM module. This divider, FM_CLKDIV[6:0], is used to control the period of the clock used for timed events in the FM erase algorithm. This register must be set with appropriate values before the lockout sequence can begin. Refer to the JTAG section of the **56F8300 Peripheral User Manual** for more details on setting this register value.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register**" section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

10.7 Crystal Oscillator Timing

Table 10-15 Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal Start-up time	T_{CS}	4	5	10	ms
Resonator Start-up time	T_{RS}	0.1	0.18	1	ms
Crystal ESR	R_{ESR}	—	—	120	ohms
Crystal Peak-to-Peak Jitter	T_D	70	—	250	ps
Crystal Min-Max Period Variation	T_{PV}	0.12	—	1.5	ns
Resonator Peak-to-Peak Jitter	T_{RJ}	—	—	300	ps
Resonator Min-Max Period Variation	T_{RP}	—	—	300	ps
Bias Current, high-drive mode	I_{BIASH}	—	250	290	µA
Bias Current, low-drive mode	I_{BIASL}	—	80	110	µA
Quiescent Current, power-down mode	I_{PD}	—	0	1	µA

10.8 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 10-4** shows sample timing and parameters that are detailed in **Table 10-16**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion, as well as user controlled wait states. The equation:

$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in this equation are defined as:

- t = Parameter delay time
- D = Fixed portion of the delay, due to on-chip path delays
- P = Period of the system clock, which determines the execution rate of the part (i.e., when the device is operating at 60MHz, P = 16.67 ns)
- M = Fixed portion of a clock period inherent in the design; this number is adjusted to account for possible derating of clock duty cycle
- W = Sum of the applicable wait state controls. The "Wait State Controls" column of **Table 10-16** shows the applicable controls for each parameter and the EMI chapter of the **56F8300 Peripheral User Manual** details what each wait state field controls.

When using the XTAL clock input directly as the chip clock without prescaling (ZSRC selects prescaler clock and prescaler set to ÷ 1), the EMI quadrature clock is generated using both edges of the EXTAL clock input. In this situation only, parameter values must be adjusted for the duty cycle at XTAL. DCAOE and DCAEO are used to make this duty cycle adjustment where needed.

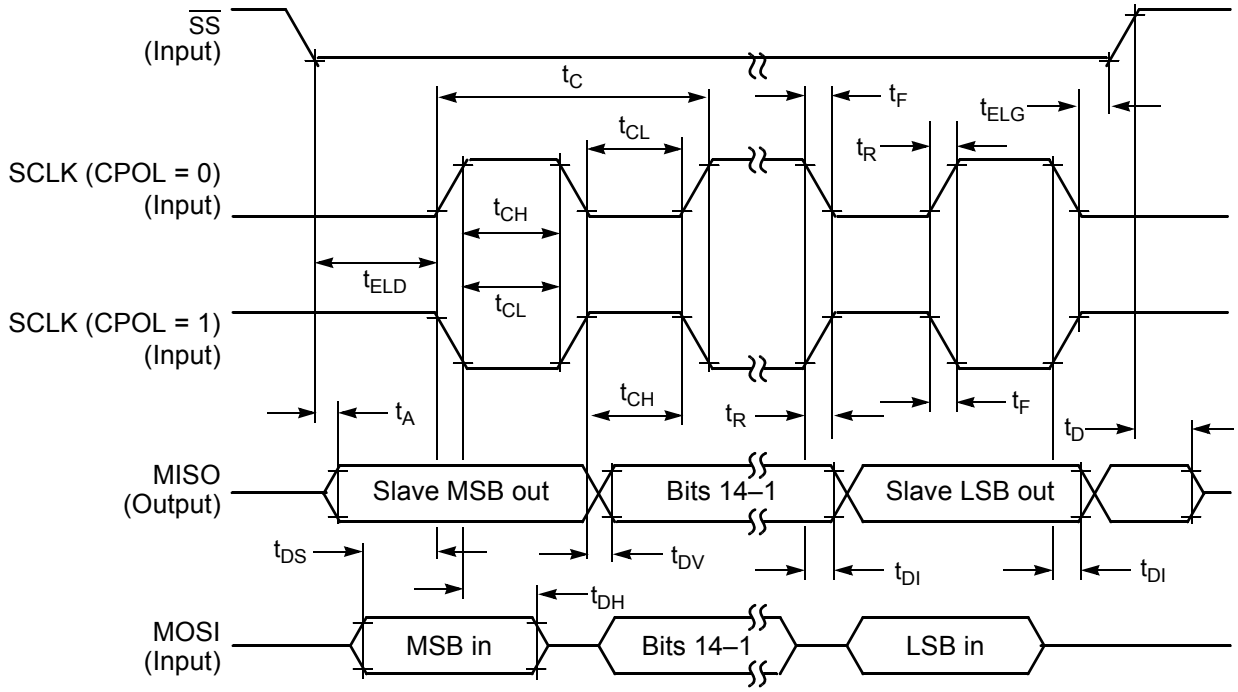


Figure 10-12 SPI Slave Timing (CPHA = 0)

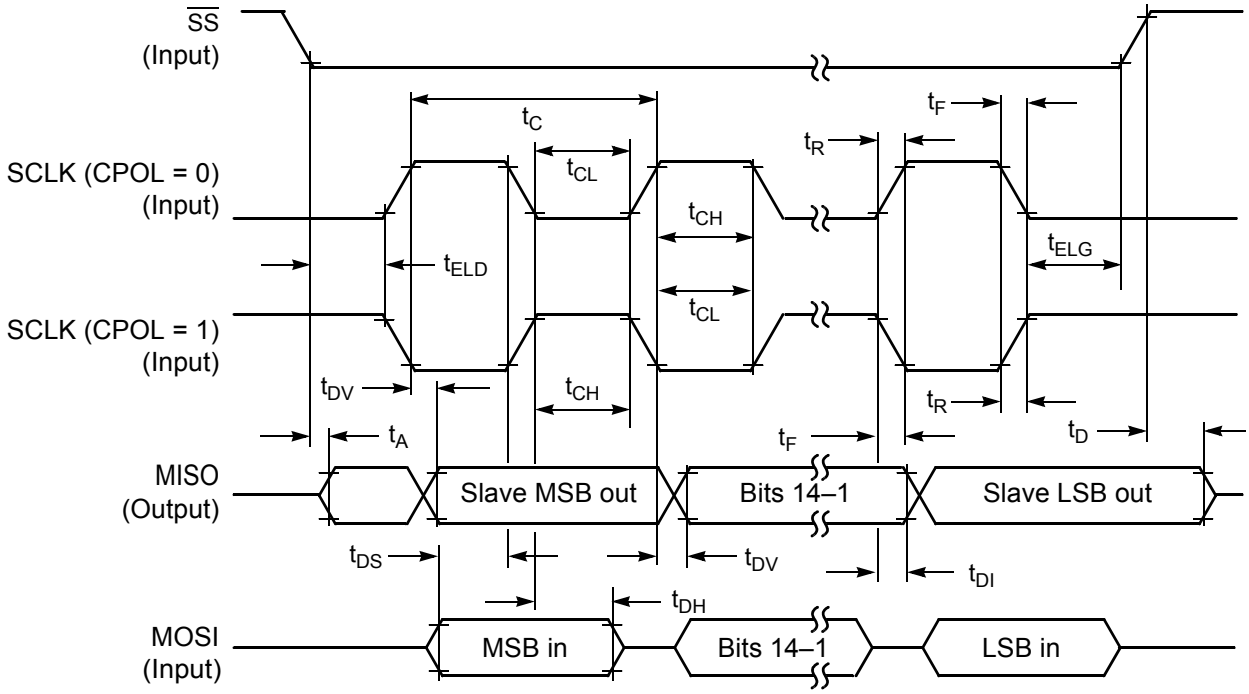


Figure 10-13 SPI Slave Timing (CPHA = 1)

10.16 Analog-to-Digital Converter (ADC) Parameters

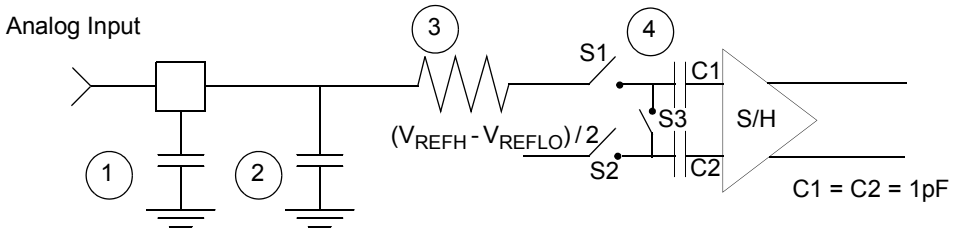
Table 10-24 ADC Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[1]	INL	—	+/- 2.4	+/- 3.2	LSB[2]
Differential Non-Linearity	DNL	—	+/- 0.7	< +1	LSB[2]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC channel power-up time	t_{ADPU}	5	6	16	t_{AIC} cycles[3]
ADC reference circuit power-up time[4]	t_{VREF}	—	—	25	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Input capacitance	C_{ADI}	—	5	—	pF
Input injection current[5], per pin	I_{ADI}	—	—	3	mA
Input injection current, total	I_{ADIT}	—	—	20	mA
V_{REFH} current	I_{VREFH}	—	1.2	3	mA
ADC A current	I_{ADCA}	—	25	—	mA
ADC B current	I_{ADCB}	—	25	—	mA
Quiescent current	I_{ADCQ}	—	0	10	μA
Uncalibrated Gain Error (ideal = 1)	E_{GAIN}	—	.+/- .004	+/- .015	—
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 18	+/- 46	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-22**	—	LSBs
Calibration Factor 1[7]	CF1	—	-0.003141	—	—
Calibration Factor 2[7]	CF2	—	-17.6	—	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db
Signal-to-noise plus distortion ratio	SINAD	—	59.1	—	db

10.17 Equivalent Circuit for ADC Inputs

Figure 10-23 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to V_{REFH} - V_{REFH} / 2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about V_{REFH} - V_{REFH} / 2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-23 Equivalent Circuit for A/D Loading

10.18 Power Consumption

This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the IO cell types used on the device reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-25 I/O Loading Coefficients at 10MHz

	Intercept	Slope
PDU08DGZ_ME	1.3	0.11mW / pF
PDU04DGZ_ME	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-25** provides coefficients for calculating power dissipated in the IO cells as a function of capacitive load. In these cases:

TotalPower = Σ((Intercept +Slope*Cload)*frequency/10MHz)

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

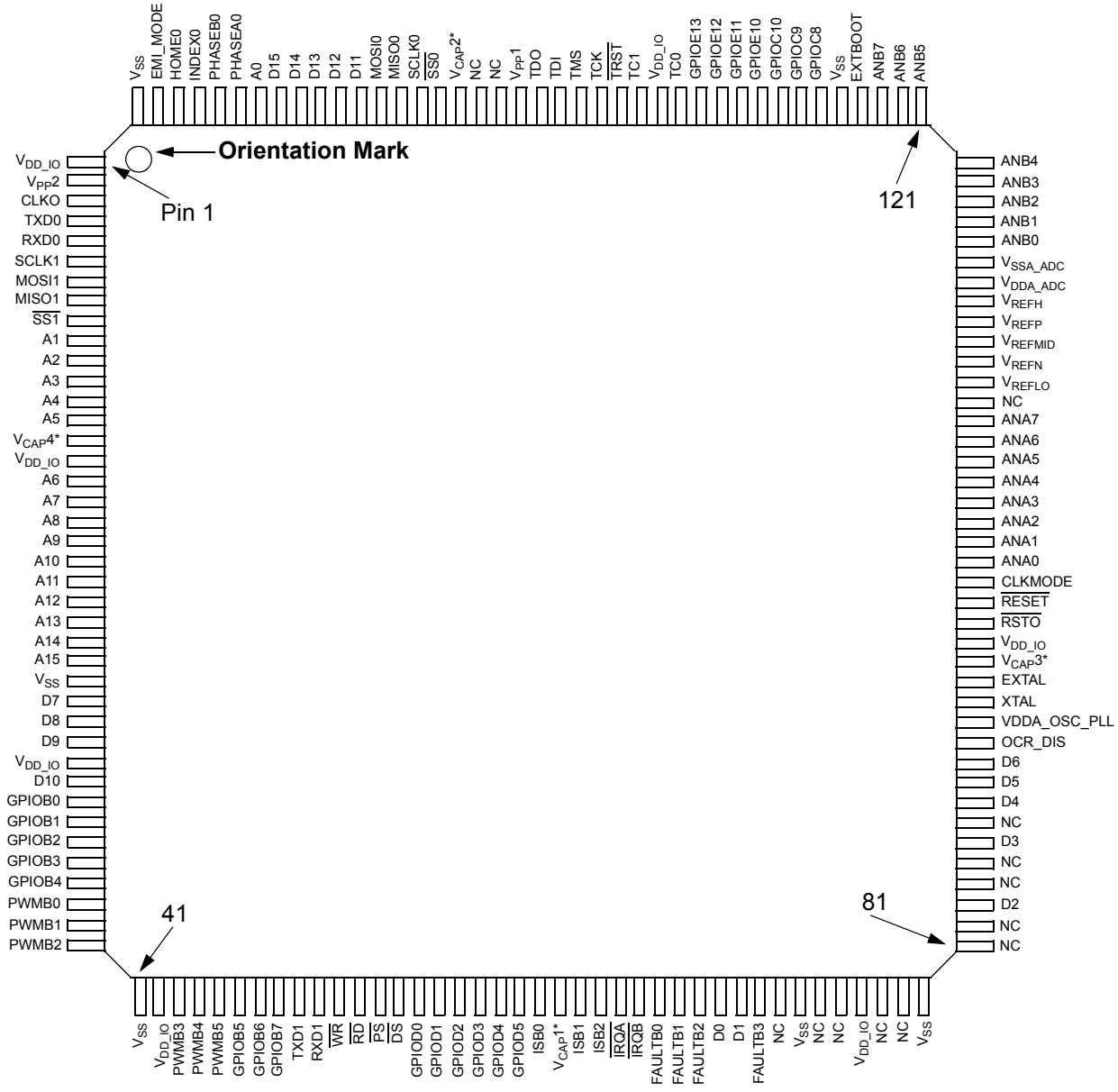
Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time. The one possible exception to this is if the chip is using the external address and data buses at a rate approaching the maximum system rate. In this case, power from these buses can be significant.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of 8 PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

11.2 56F8147 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8147. This device comes in a 160-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-4** shows the package outline for the 160-pin LQFP, **Figure 11-5** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 160-pin LQFP.



* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

Figure 11-4 Top View, 56F8147 160-Pin LQFP Package