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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8347mpye

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8147 device and are shaded in the following figures.*

The 56F8347/56F8147 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories, the external memory interface and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User's Manual** for clarification on the operation of all three of these peripherals.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
D7 **(GPIOF0)**	28	K1	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D7 - D15 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D7 - D15 are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — These nine GPIO pins can be individually programmed as input or output pins. At reset, these pins default to data bus functionality. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF0, clear bit 0 in the GPIOF_PUR register.
D8 (GPIOF1)	29	K3			
D9 (GPIOF2)	30	K2			
D10 (GPIOF3)	32	K4			
D11 (GPIOF4)	149	A5			
D12 (GPIOF5)	150	A4			
D13 (GPIOF6)	151	B5			
D14 (GPIOF7)	152	C4			
D15 (GPIOF8)	153	A3			
$\overline{\text{RD}}$	52	P5	Output	In reset, output is disabled, pull-up is enabled	**Read Enable** — $\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0 - D15 become inputs and an external device is enabled onto the data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the device. When $\overline{\text{RD}}$ is asserted, it qualifies the A0 - A16, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a static RAM or ROM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{RD}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
TXD1 **(GPIOD6)**	49	P4	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI1 transmit data output **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOD_PUR register.
RXD1 **(GPIOD7)**	50	N5	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI1 receive data input **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI input. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOD_PUR register.
TCK	137	D8	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor.
TMS	138	A8	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	139	B8	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register.
TDO	140	D7	Output	In reset, output is disabled, pull-up is enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
PHASEA1	6	C1	Schmitt Input	Input, pull-up enabled	**Phase A1** — Quadrature Decoder 1, PHASEA input for decoder 1.
(TB0)			Schmitt Input/ Output		**TB0** — Timer B, Channel 0
(SCLK1)			Schmitt Input/ Output		**SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. To activate the SPI function, set the PHSA_ALT bit in the SIM_GPS register. For details, see Part 6.5.8.
(GPIOC0)			Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8347, the default state after reset is PHASEA1. In the 56F8147, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOC_PUR register.
PHASEB1	7	D1	Schmitt Input	Input, pull-up enabled	**Phase B1** — Quadrature Decoder 1, PHASEB input for decoder 1.
(TB1)			Schmitt Input/ Output		**TB1** — Timer B, Channel 1
(MOSI1)			Schmitt Input/ Output		**SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. To activate the SPI function, set the PHSB_ALT bit in the SIM_GPS register. For details, see Part 6.5.8.
(GPIOC1)			Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8347, the default state after reset is PHASEB1. In the 56F8147, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOC_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
INDEX1	8	E2	Schmitt Input	Input, pull-up enabled	**Index1** — Quadrature Decoder 1, INDEX input
(TB2)			Schmitt Input/ Output		**TB2** — Timer B, Channel 2
(MISO1)			Schmitt Input/ Output		**SPI 1 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. To activate the SPI function, set the INDEX_ALT bit in the SIM_GPS register. For details, see Part 6.5.8.
(GPIOC2)			Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8347, the default state after reset is INDEX1. In the 56F8147, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 2 in the GPIOC_PUR register.
HOME1	9	E1	Schmitt Input	Input, pull-up enabled	**Home** — Quadrature Decoder 1, HOME input
(TB3)			Schmitt Input/ Output		**TB3** — Timer B, Channel 3
($\overline{\text{SS1}}$)			Schmitt Input		**SPI 1 Slave Select** — In the master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. To activate the SPI function, set the HOME_ALT bit in the SIM_GPS register. For details, see Part 6.5.8.
(GPIOC3)			Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8347, the default state after reset is HOME1. In the 56F8147, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 3 in the GPIOC_PUR register.

Part 3 On-Chip Clock Synthesis (OCCS)

3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design. **Figure 3-1** shows the specific OCCS block diagram to reference in the OCCS chapter of the **56F8300 Peripheral User Manual**.

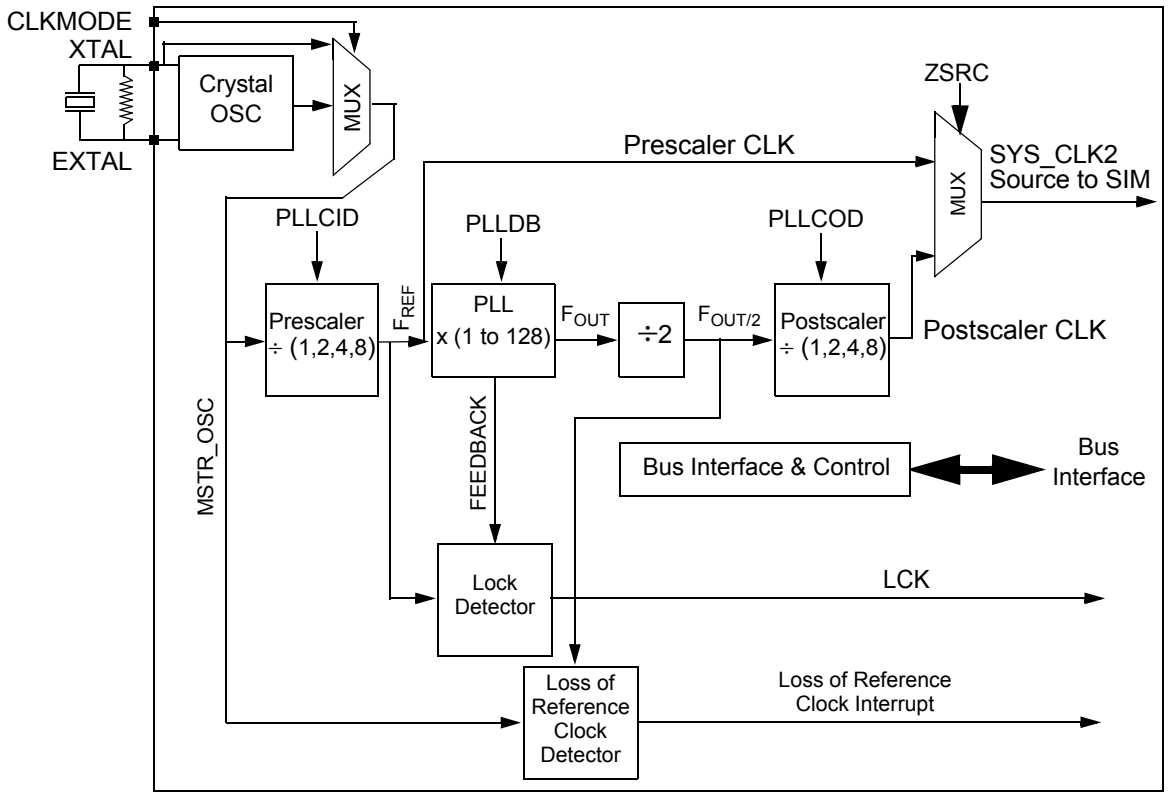


Figure 3-1 OCCS Block Diagram

3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator, or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator must be connected between the EXTAL and XTAL pins.

3.2.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-15**. A recommended crystal oscillator circuit is shown in **Figure 3-2**. Follow the crystal supplier's recommendations when selecting a crystal, since crystal

Table 4-10 External Memory Integration Registers Address Map (Continued) (EMI_BASE = $00 F020)

Register Acronym	Address Offset	Register Description	Reset Value
CSOR 4	$C	Chip Select Option Register 4	
CSOR 5	$D	Chip Select Option Register 5	
CSOR 6	$E	Chip Select Option Register 6	
CSOR 7	$F	Chip Select Option Register 7	
CSTC 0	$10	Chip Select Timing Control Register 0	
CSTC 1	$11	Chip Select Timing Control Register 1	
CSTC 2	$12	Chip Select Timing Control Register 2	
CSTC 3	$13	Chip Select Timing Control Register 3	
CSTC 4	$14	Chip Select Timing Control Register 4	
CSTC 5	$15	Chip Select Timing Control Register 5	
CSTC 6	$16	Chip Select Timing Control Register 6	
CSTC 7	$17	Chip Select Timing Control Register 7	
BCR	$18	Bus Control Register	0x016B sets the default number of wait states to 11 for both read and write accesses

Table 4-11 Quad Timer A Registers Address Map (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMP1	$0	Compare Register 1
TMRA0_CMP2	$1	Compare Register 2
TMRA0_CAP	$2	Capture Register
TMRA0_LOAD	$3	Load Register
TMRA0_HOLD	$4	Hold Register
TMRA0_CNTR	$5	Counter Register
TMRA0_CTRL	$6	Control Register
TMRA0_SCR	$7	Status and Control Register
TMRA0_CMPLD1	$8	Comparator Load Register 1
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_COMSCR	$A	Comparator Status and Control Register
		Reserve
TMRA1_CMP1	$10	Compare Register 1
TMRA1_CMP2	$11	Compare Register 2
TMRA1_CAP	$12	Capture Register
TMRA1_LOAD	$13	Load Register

Table 4-30 GPIOB Registers Address Map (GPIOB_BASE = $00 F300)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOB_PUR	$0	Pull-up Enable Register	0 x 3FFF
GPIOB_DR	$1	Data Register	0 x 0000
GPIOB_DDR	$2	Data Direction Register	0 x 0000
GPIOB_PER	$3	Peripheral Enable Register	0 x 000F for 20-bit EMI addresss at reset. 0 x 0000 for all other cases. See Table 4-4 for details.
GPIOB_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOB_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOB_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOB_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOB_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOB_PPMODE	$9	Push-Pull Mode Register	0 x 3FFF
GPIOB_RAWDATA	$A	Raw Data Input Register	—

Table 4-31 GPIOC Registers Address Map (GPIOC_BASE = $00 F310)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOC_PUR	$0	Pull-up Enable Register	0 x 07FF
GPIOC_DR	$1	Data Register	0 x 0000
GPIOC_DDR	$2	Data Direction Register	0 x 0000
GPIOC_PER	$3	Peripheral Enable Register	0 x 07FF
GPIOC_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOC_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOC_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOC_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOC_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOC_PPMODE	$9	Push-Pull Mode Register	0 x 07FF
GPIOC_RAWDATA	$A	Raw Data Input Register	—

5.6.1 Interrupt Priority Register 0 (IPR0)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-3 Interrupt Priority Register 0 (IPR0)

5.6.1.1 Reserved—Bits 15–14

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.1.2 EOnCE Breakpoint Unit 0 Interrupt Priority Level (BKPT_U0 IPL)—Bits13–12

This field is used to set the interrupt priority levels for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.3 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.4 Reserved—Bits 9–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2 Interrupt Priority Register 1 (IPR1)

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-4 Interrupt Priority Register 1 (IPR1)

5.6.9.7 Timer A, Channel 2 Interrupt Priority Level (TMRA2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.8 Timer A, Channel 1 Interrupt Priority Level (TMRA1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10 Interrupt Priority Register 9 (IPR9)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PWMA_F IPL		PWMB_F IPL		PWMA_RL IPL		PWM_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Interrupt Priority Register 9 (IPR9)

5.6.10.1 PWM A Fault Interrupt Priority Level (PWMA_F IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.2 PWM B Fault Interrupt Priority Level (PWMB_F IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.30.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

5.6.30.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[7:1]) used at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.30.6 $\overline{\text{IRQB}}$ State Pin ($\overline{\text{IRQB}}$ STATE)—Bit 3

This *read-only* bit reflects the state of the external $\overline{\text{IRQB}}$ pin.

5.6.30.7 $\overline{\text{IRQA}}$ State Pin ($\overline{\text{IRQA}}$ STATE)—Bit 2

This *read-only* bit reflects the state of the external $\overline{\text{IRQA}}$ pin.

5.6.30.8 $\overline{\text{IRQB}}$ Edge Pin ($\overline{\text{IRQB}}$ Edg)—Bit 1

This bit controls whether the external $\overline{\text{IRQB}}$ interrupt is edge- or level-sensitive. During Stop and Wait modes, it is automatically level-sensitive.

- 0 = $\overline{\text{IRQB}}$ interrupt is a low-level sensitive (default)
- 1 = $\overline{\text{IRQB}}$ interrupt is falling-edge sensitive

6.5.7.7 CLockout Select (CLKOSEL)—Bits 4–0

Selects clock to be muxed out on the CLKO pin.

- 00000 = SYS_CLK (from OCCS - DEFAULT)
- 00001 = Reserved for factory test—56800E clock
- 00010 = Reserved for factory test—XRAM clock
- 00011 = Reserved for factory test—PFLASH odd clock
- 00100 = Reserved for factory test—PFLASH even clock
- 00101 = Reserved for factory test—BFLASH clock
- 00110 = Reserved for factory test—DFLASH clock
- 00111 = Oscillator output
- 01000 = F_{out} (from OCCS)
- 01001 = Reserved for factory test—IPB clock
- 01010 = Reserved for factory test—Feedback (from OCCS, this is path to PLL)
- 01011 = Reserved for factory test—Prescaler clock (from OCCS)
- 01100 = Reserved for factory test—Postscaler clock (from OCCS)
- 01101 = Reserved for factory test—SYS_CLK2 (from OCCS)
- 01110 = Reserved for factory test—SYS_CLK_DIV2
- 01111 = Reserved for factory test—SYS_CLK_D
- 10000 = ADCA clock
- 10001 = ADCB clock

6.5.8 GPIO Peripheral Select Register (SIM_GPS)

The GPIO Peripheral Select register can be used to multiplex out any one of the three alternate peripherals for GPIOC. The default peripheral is *Quad Decoder 1* and *Quad Timer B* (*NOT available in the 56F8147 device*); these peripherals work together.

The four I/O pins associated with GPIOC can function as GPIO, *Quad Decoder 1/Quad Timer B*, or as SPI 1 signals. GPIO is not the default and is enabled/disabled via the GPIOC_PER, as shown in **Figure 6-10** and **Table 6-2**. When GPIOC[3:0] are programmed to operate as peripheral I/O, then the choice between decoder/timer and SPI inputs/outputs is made in the SIM_GPS register and in conjunction with the Quad Timer Status and Control Registers (SCR). The default state is for the peripheral function of GPIOC[3:0] to be programmed as decoder functions. This can be changed by altering the appropriate controls in the indicated registers.

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	ISAL[21:6]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-15 I/O Short Address Location Low Register (SIM_ISAL)

6.5.10.2 Input/Output Short Address Low (ISAL[21:6])—Bit 15–0

This field represents the lower 16 address bits of the “hard coded” I/O short address.

6.6 Clock Generation Overview

The SIM uses an internal master clock from the OCCS (CLKGEN) module to produce the peripheral and system (core and memory) clocks. The maximum master clock frequency is 120MHz. Peripheral and system clocks are generated at half the master clock frequency and therefore at a maximum 60MHz. The SIM provides power modes (Stop, Wait) and clock enables (SIM_PCE register, CLK_DIS, ONCE_EBL) to control which clocks are in operation. The OCCS, power modes, and clock enables provide a flexible means to manage power consumption.

Power utilization can be minimized in several ways. In the OCCS, crystal oscillator, and PLL may be shut down when not in use. When the PLL is in use, its prescaler and postscaler can be used to limit PLL and master clock frequency. Power modes permit system and/or peripheral clocks to be disabled when unused. Clock enables provide the means to disable individual clocks. Some peripherals provide further controls to disable unused subfunctions. Refer to **Part 3 On-Chip Clock Synthesis (OCCS)**, and the **56F8300 Peripheral User Manual** for further details.

6.7 Power-Down Modes Overview

The 56F8347/56F8147 operate in one of three power-down modes, as shown in **Table 6-3**.

Table 6-3 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can produce interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.
Stop	System clocks continue to be generated in the SIM, but most are gated prior to reaching memory, core and peripherals.		The only possible recoveries from Stop mode are: 1. CAN traffic (1st message will be lost) 2. Non-clocked interrupts 3. COP reset 4. External reset 5. Power-on reset

7.2.4 Product Analysis

The recommended method of unsecuring a programmed device for product analysis of field failures is via the backdoor key access. The customer would need to supply Technical Support with the backdoor key and the protocol to access the backdoor routine in the Flash. Additionally, the KEYEN bit that allows backdoor key access must be set.

An alternative method for performing analysis on a secured microcontroller would be to mass-erase and reprogram the Flash with the original code, but modify the security bytes.

To insure that a customer does not inadvertently lock himself out of the device during programming, it is recommended that he program the backdoor access key first, his application code second, and the security bytes within the FM configuration field last.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F8300 Peripheral User Manual** and contains only chip-specific information. This information supercedes the generic information in the **56F8300 Peripheral User Manual**.

8.2 Memory Maps

The width of the GPIO port defines how many bits are implemented in each of the GPIO registers. Based on this and the default function of each of the GPIO pins, the reset values of the GPIOx_PUR and GPIOx_PER registers change from port to port. Tables 4-29 through 4-34 define the actual reset values of these registers.

8.3 Configuration

There are six GPIO ports defined on the 56F8347/56F8147. The width of each port and the associated peripheral function is shown in Table 8-1 and Table 8-2. The specific mapping of GPIO port pins is shown in Table 8-3.

Table 8-1 56F8347 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8347	Peripheral Function	Reset Function
A	14	14	14 pins - EMI Address pins	EMI Address
B	8	8	8 pins - EMI Address pins	EMI Address
C	11	11	4 pins -DEC1 / TMRB / SPI1 4 pins -DEC0 / TMRA 3 pins -PWMA current sense	DEC1 / TMRB DEC0 / TMRA PWMA current sense

10.2 DC Electrical Characteristics

Note: *The 56F8147 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8147 device.*

Table 10-5 DC Electrical Characteristics

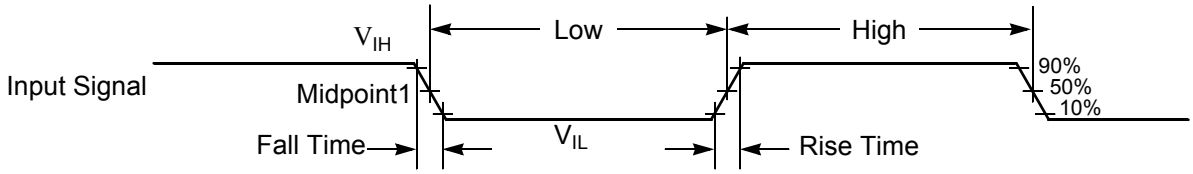
At Recommended Operating Conditions; see Table 10-4

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}		2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Low Voltage	V_{OL}		—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2, 5, 6, 9	—	0	+/- 2.5	µA	V_{IN} = 3.0V to 5.5V
Digital Input Current High with pull-down	I_{IH}	Pin Group 10	40	80	160	µA	V_{IN} = 3.0V to 5.5V
Analog Input Current High	I_{IHA}	Pin Group 13	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$
ADC Input Current High	I_{IHADC}	Pin Group 12	—	0	+/- 10	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low pull-up enabled	I_{IL}	Pin Groups 1, 2, 5, 6, 9	-200	-100	-50	µA	V_{IN} = 0V
Digital Input Current Low pull-up disabled	I_{IL}	Pin Groups 1, 2, 5, 6, 9	—	0	+/- 2.5	µA	V_{IN} = 0V
Digital Input Current Low with pull-down	I_{IL}	Pin Group 10	—	0	+/- 2.5	µA	V_{IN} = 0V
Analog Input Current Low	I_{ILA}	Pin Group 13	—	0	+/- 2.5	µA	V_{IN} = 0V
ADC Input Current Low	I_{ILADC}	Pin Group 12	—	0	+/- 10	µA	V_{IN} = 0V
EXTAL Input Current Low clock input	I_{EXTAL}		—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
XTAL Input Current Low clock input	I_{XTAL}	CLKMODE = High	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
		CLKMODE = Low	—	—	200	µA	$V_{IN} = V_{DDA}$ or 0V
Output Current High Impedance State	I_{OZ}	Pin Groups 1, 2, 3, 4, 5, 6, 7, 8	—	0	+/- 2.5	µA	V_{OUT} = 3.0V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 2, 6, 9, 10	—	0.3	—	V	—
Input Capacitance (EXTAL/XTAL)	C_{INC}		—	4.5	—	pF	—
Output Capacitance (EXTAL/XTAL)	C_{OUTC}		—	5.5	—	pF	—
Input Capacitance	C_{IN}		—	6	—	pF	—
Output Capacitance	C_{OUT}		—	6	—	pF	—

See Pin Groups in Table 10-1

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 10-5. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 10-1.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 10-1 Input Signal Measurement References

Figure 10-2 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

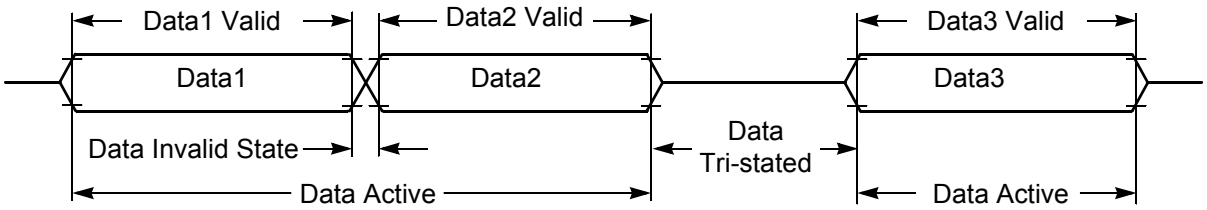


Figure 10-2 Signal States

10.4 Flash Memory Characteristics

Table 10-12 Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	Tprog	20	—	—	µs
Erase time[2]	Terase	20	—	—	ms
Mass erase time	Tme	100	—	—	ms

1. There is additional overhead which is part of the programming sequence. See the **56F8300 Peripheral User Manual** for details. Program time is per 16-bit word in Flash memory. Two words at a time can be programmed within the Program Flash module, as it contains two interleaved memories.
2. Specifies page erase time. There are 512 bytes per page in the Data and Boot Flash memories. The Program Flash module uses two interleaved Flash memories, increasing the effective page size to 1024 bytes.

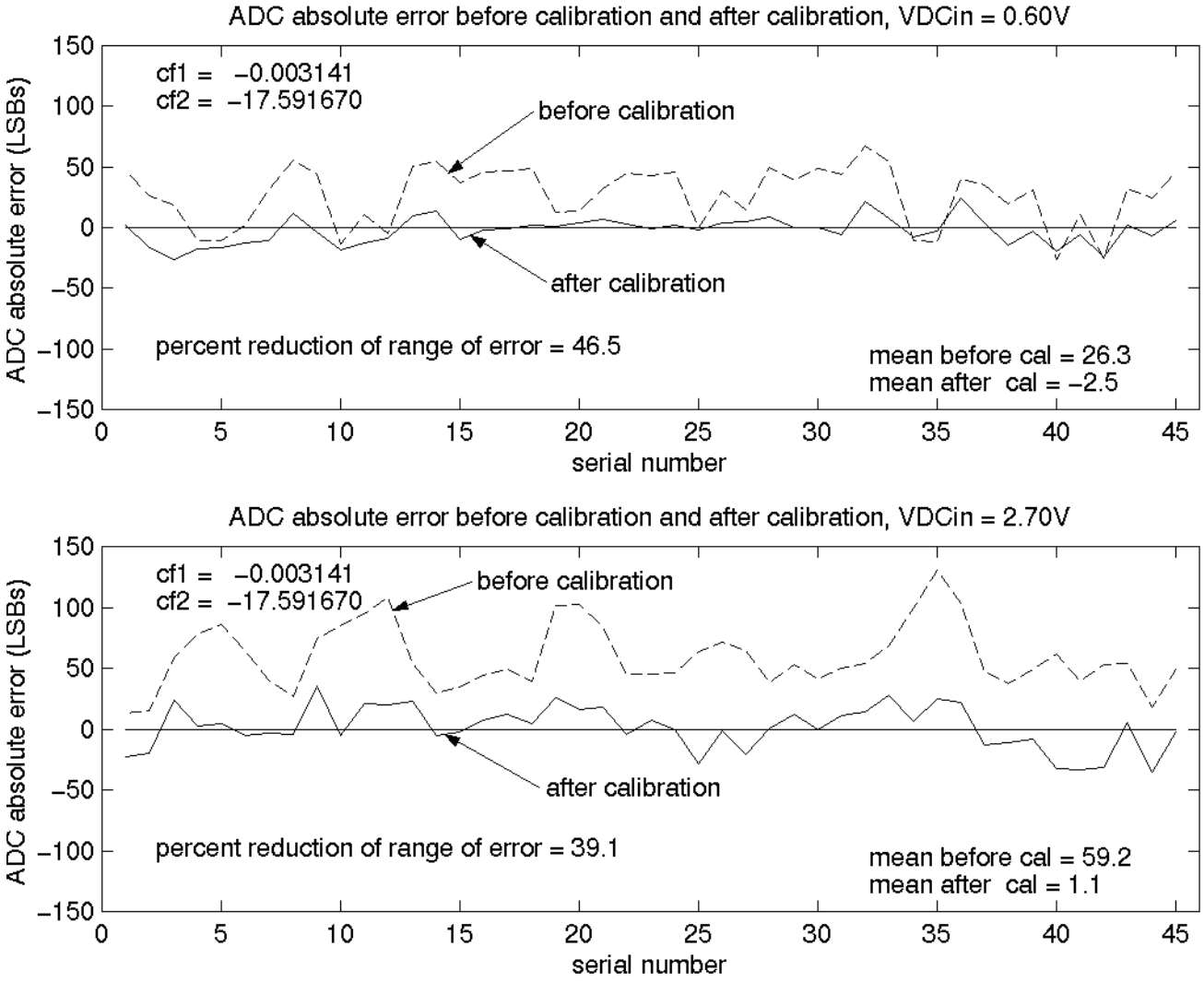


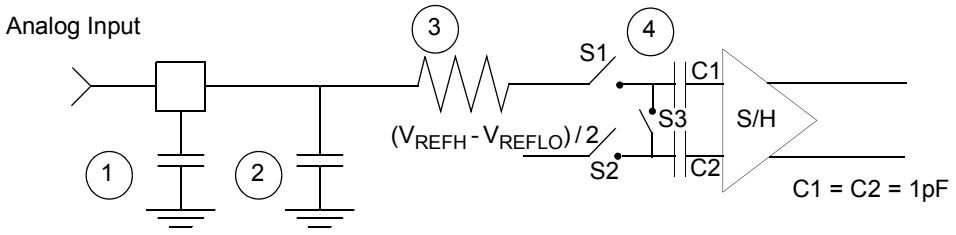
Figure 10-22 ADC Absolute Error Over Processing and Temperature Extremes Before and After Calibration for VDC_{in} = 0.60V and 2.70V

Note: The absolute error data shown in the graphs above reflects the effects of both gain error and offset error. The data was taken on 15 parts: five each from four processing corner lots as well as five from one nominally processed lot, each at three temperatures: -40°C, 27°C, and 150°C (giving the 75 data points shown above), for two input DC voltages: 0.60V and 2.70V. The data indicates that for the given population of parts, calibration significantly reduced (by as much as 24%) the collective variation (spread) of the absolute error of the population. It also significantly reduced (by as much as 38%) the mean (average) of the absolute error and thereby brought it significantly closer to the ideal value of zero. Although not guaranteed, it is believed that calibration will produce results similar to those shown above for any population of parts including those which represent processing and temperature extremes.

10.17 Equivalent Circuit for ADC Inputs

Figure 10-23 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to V_{REFH} - V_{REFH} / 2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about V_{REFH} - V_{REFH} / 2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-23 Equivalent Circuit for A/D Loading

10.18 Power Consumption

This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the IO cell types used on the device reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-25 I/O Loading Coefficients at 10MHz

	Intercept	Slope
PDU08DGZ_ME	1.3	0.11mW / pF
PDU04DGZ_ME	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-25** provides coefficients for calculating power dissipated in the IO cells as a function of capacitive load. In these cases:

TotalPower = Σ((Intercept +Slope*Cload)*frequency/10MHz)

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time. The one possible exception to this is if the chip is using the external address and data buses at a rate approaching the maximum system rate. In this case, power from these buses can be significant.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of 8 PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

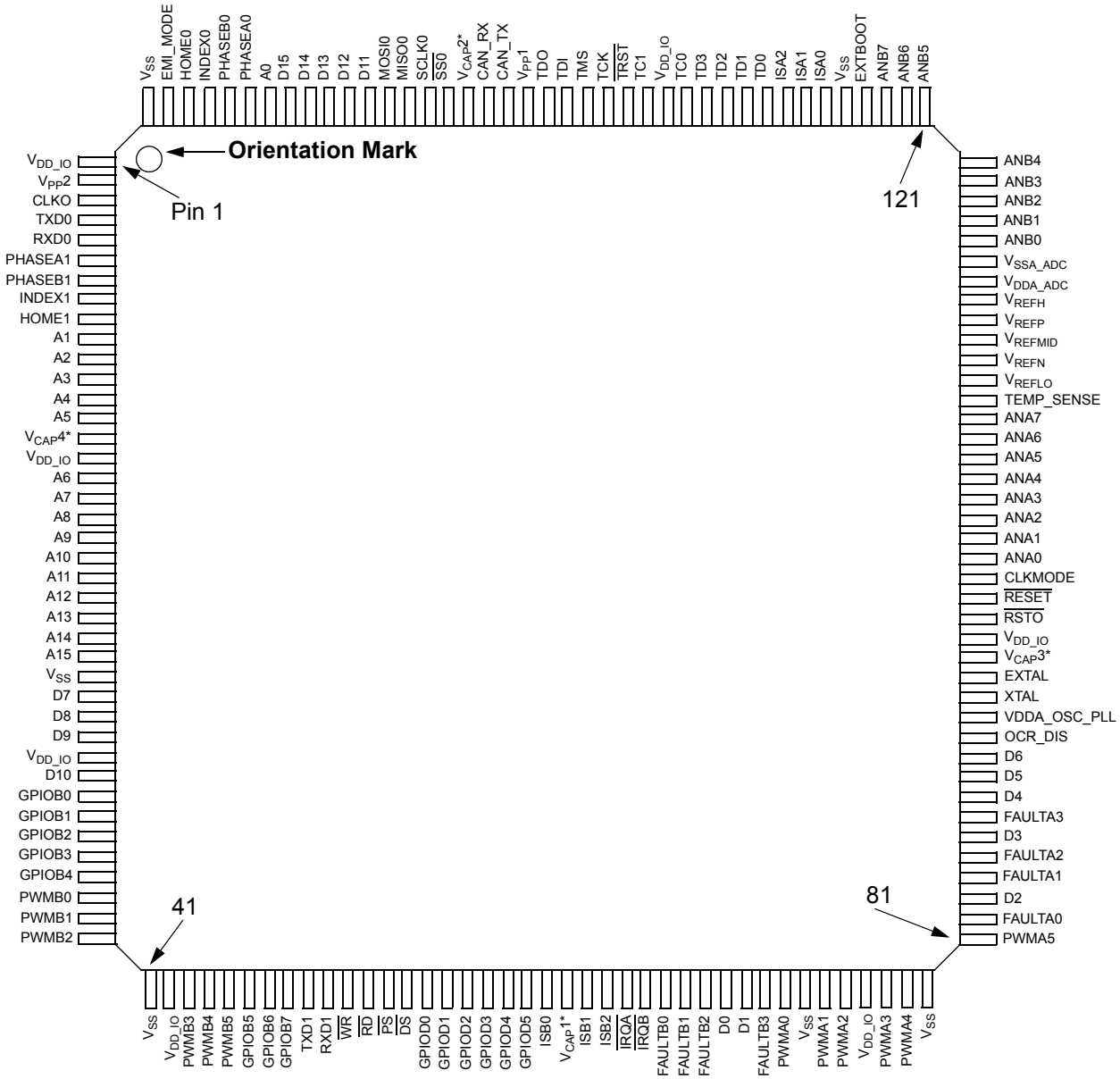
In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

Part 11 Packaging

Note: *The 160 Map Ball Grid Array is not available in the 56F8147 device.*

11.1 56F8347 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8347. This device comes in a 160-pin Low-profile Quad Flat Pack (LQFP) and *160 Map Ball Grid Array*. **Figure 11-1** shows the package lay-out for the 160-pin LQFP, and **Figure 11-2** for the160 Map Ball Grid Array. **Figure 11-5** for the shows the mechanical parameters for the LQFP package and **Figure 11-3** for the MBGA. **Table 11-1** lists the pin-out for the 160-pin LQFP and **Table 11-2** lists the pin-out for the 160 MBGA.



* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

Figure 11-1 Top View, 56F8347 160-Pin LQFP Package