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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8347vpye

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8147 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection feature
- On-chip memory, including a low-cost, high-volume Flash solution
  - 128KB of Program Flash
  - *4KB of Program RAM*
  - *8KB of Data Flash*
  - 8KB of Data RAM
  - 8KB of Boot Flash
- Off-chip memory expansion capabilities provide a simple method for interfacing additional external memory and/or peripheral devices
  - Access up to 4MB of external program memory or 32MB of external data memory
  - External accesses supported at up to 60MHz (zero wait states)
- *EEPROM emulation capability*

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8147 device.*

- Pulse Width Modulator:
  - In the 56F8347, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
  - In the 56F8147, one Pulse Width Modulator module, with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
  - In the 56F8347, two four-input Quadrature Decoders or two additional Quad Timers
  - In the 56F8147, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor diode can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
  - In the 56F8347, four dedicated general-purpose Quad Timers totaling six dedicated pins: Timer C with two pins and Timer D with four pins
  - In the 56F8147, two general-purpose Quad Timers; Timer A works in conjunction with Quadrature Decoder 0 or GPIO and Timer C works in conjunction with GPIO
- *FlexCAN (CAN Version 2.0 B-compliant) module with 2-pin port for transmit and receive*

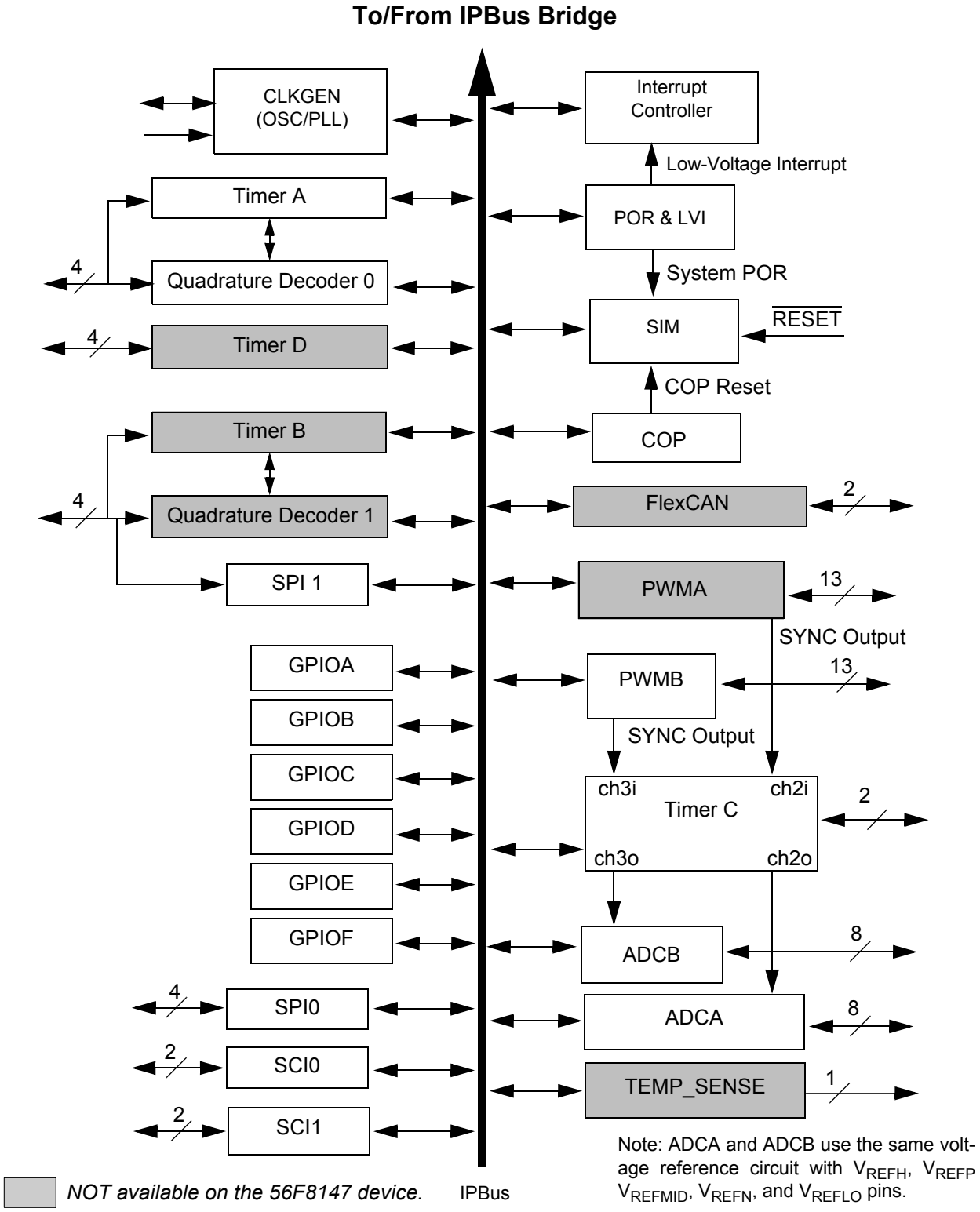


Figure 1-2 Peripheral Subsystem

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
ISB0 **(GPIOD10)**	61	N8	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISB0 - 2** — These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB. **Port D GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to ISB functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOD_PUR register. For details, see Part 6.5.8.
ISB1 (GPIOD11)	63	L8			
ISB2 (GPIOD12)	64	P8			
FAULTB0	67	N9	Schmitt Input	Input, pull-up enabled	**FAULTB0 - 3** — These four fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMB bit in the SIM_PUDR register. For details, see Part 6.5.8.
FAULTB1	68	L9			
FAULTB2	69	L10			
FAULTB3	72	P11			
ANA0	100	G13	Input	Analog Input	**ANA0 - 3** — Analog inputs to ADC A, channel 0
ANA1	101	H13			
ANA2	102	G12			
ANA3	103	F13			
ANA4	104	F12	Input	Analog Input	**ANA4 - 7** — Analog inputs to ADC A, channel 1
ANA5	105	H14			
ANA6	106	G14			
ANA7	107	E13			
V_{REFH}	113	D14	Input	Analog Input	**V_{REFH}** — Analog Reference Voltage High. V_{REFH} must be less than or equal to V_{DDA_ADC}.
V_{REFP}	112	D13	Input/ Output	Analog Input/ Output	**V_{REFP}, V_{REFMID} & V_{REFN}** — Internal pins for voltage reference which are brought off-chip so they can be bypassed. Connect to a 0.1μF low ESR capacitor.
V_{REFMID}	111	E14			
V_{REFN}	110	F14			
V_{REFLO}	109	E12	Input	Analog Input	**V_{REFLO}** — Analog Reference Voltage Low. This should normally be connected to a low-noise V_{SS}.

Table 4-5 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
SCI0	68	0-2	P:$88	SCI 0 Transmitter Empty
SCI0	69	0-2	P:$8A	SCI 0 Transmitter Idle
				Reserved
SCI0	71	0-2	P:$8E	SCI 0 Receiver Error
SCI0	72	0-2	P:$90	SCI 0 Receiver Full
ADCB	73	0-2	P:$92	ADC B Conversion Compete / End of Scan
ADCA	74	0-2	P:$94	ADC A Conversion Complete / End of Scan
ADCB	75	0-2	P:$96	ADC B Zero Crossing or Limit Error
ADCA	76	0-2	P:$98	ADC A Zero Crossing or Limit Error
PWMB	77	0-2	P:$9A	Reload PWM B
PWMA	78	0-2	P:$9C	Reload PWM A
PWMB	79	0-2	P:$9E	PWM B Fault
PWMA	80	0-2	P:$A0	PWM A Fault
core	81	- 1	P:$A2	SW Interrupt LP

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to 0200 (or VBA = 0000 for Mode 1, EMI_MODE = 0), the first two locations of the vector table are the chip reset addresses; therefore, these locations are not interrupt vectors.

4.4 Data Map

Note: *Data Flash is NOT available on the 56F8147 device.*

Table 4-6 Data Memory Map[1]

Begin/End Address	EX = 0[2]	EX = 1
X:$FF FFFF X:$FF 0000	EOnCE 256 locations allocated	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	External Memory	External Memory
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 2000	External Memory	External Memory
X:$00 1FFF X:$00 1000	*On-Chip Data Flash* 8KB	
X:$00 0FFF X:$00 0000	On-Chip Data RAM 8KB[3]	

1. All addresses are 16-bit Word addresses, not byte addresses.
2. In the Operating Mode Register (OMR).
3. The Data RAM is organized as a 2K x 32-bit memory to allow single-cycle long-word operations.

Table 4-14 Quad Timer D Registers Address Map (Continued) (TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8147 device

Register Acronym	Address Offset	Register Description
TMRD2_CMPLD1	$28	Comparator Load Register 1
TMRD2_CMPLD2	$29	Comparator Load Register 2
TMRD2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRD3_CMP1	$30	Compare Register 1
TMRD3_CMP2	$31	Compare Register 2
TMRD3_CAP	$32	Capture Register
TMRD3_LOAD	$33	Load Register
TMRD3_HOLD	$34	Hold Register
TMRD3_CNTR	$35	Counter Register
TMRD3_CTRL	$36	Control Register
TMRD3_SCR	$37	Status and Control Register
TMRD3_CMPLD1	$38	Comparator Load Register 1
TMRD3_CMPLD2	$39	Comparator Load Register 2
TMRD3_COMSCR	$3A	Comparator Status and Control Register

Table 4-15 Pulse Width Modulator A Registers Address Map (PWMA_BASE = $00 F140)
PWMA is NOT available in the 56F8147 device

Register Acronym	Address Offset	Register Description
PWMA_PMCTL	$0	Control Register
PWMA_PMFCTL	$1	Fault Control Register
PWMA_PMFSA	$2	Fault Status Acknowledge Register
PWMA_PMOUT	$3	Output Control Register
PWMA_PMCNT	$4	Counter Register
PWMA_PWMCM	$5	Counter Modulo Register
PWMA_PWMVAL0	$6	Value Register 0
PWMA_PWMVAL1	$7	Value Register 1
PWMA_PWMVAL2	$8	Value Register 2
PWMA_PWMVAL3	$9	Value Register 3
PWMA_PWMVAL4	$A	Value Register 4
PWMA_PWMVAL5	$B	Value Register 5
PWMA_PMDEADTM	$C	Dead Time Register

Table 4-20 Analog-to-Digital Converter Registers Address Map (Continued) (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_OFS 5	$26	Offset Register 5
ADCA_OFS 6	$27	Offset Register 6
ADCA_OFS 7	$28	Offset Register 7
ADCA_POWER	$29	Power Control Register
ADCA_CAL	$2A	ADC Calibration Register

Table 4-21 Analog-to-Digital Converter Registers Address Map (ADCB_BASE = $00 F240)

Register Acronym	Address Offset	Register Description
ADCB_CR 1	$0	Control Register 1
ADCB_CR 2	$1	Control Register 2
ADCB_ZCC	$2	Zero Crossing Control Register
ADCB_LST 1	$3	Channel List Register 1
ADCB_LST 2	$4	Channel List Register 2
ADCB_SDIS	$5	Sample Disable Register
ADCB_STAT	$6	Status Register
ADCB_LSTAT	$7	Limit Status Register
ADCB_ZCSTAT	$8	Zero Crossing Status Register
ADCB_RSLT 0	$9	Result Register 0
ADCB_RSLT 1	$A	Result Register 1
ADCB_RSLT 2	$B	Result Register 2
ADCB_RSLT 3	$C	Result Register 3
ADCB_RSLT 4	$D	Result Register 4
ADCB_RSLT 5	$E	Result Register 5
ADCB_RSLT 6	$F	Result Register 6
ADCB_RSLT 7	$10	Result Register 7
ADCB_LLMT 0	$11	Low Limit Register 0
ADCB_LLMT 1	$12	Low Limit Register 1
ADCB_LLMT 2	$13	Low Limit Register 2
ADCB_LLMT 3	$14	Low Limit Register 3
ADCB_LLMT 4	$15	Low Limit Register 4
ADCB_LLMT 5	$16	Low Limit Register 5
ADCB_LLMT 6	$17	Low Limit Register 6
ADCB_LLMT 7	$18	Low Limit Register 7
ADCB_HLMT 0	$19	High Limit Register 0

Table 4-21 Analog-to-Digital Converter Registers Address Map (Continued) (ADCB_BASE = $00 F240)

Register Acronym	Address Offset	Register Description
ADCB_HLMT 1	$1A	High Limit Register 1
ADCB_HLMT 2	$1B	High Limit Register 2
ADCB_HLMT 3	$1C	High Limit Register 3
ADCB_HLMT 4	$1D	High Limit Register 4
ADCB_HLMT 5	$1E	High Limit Register 5
ADCB_HLMT 6	$1F	High Limit Register 6
ADCB_HLMT 7	$20	High Limit Register 7
ADCB_OFS 0	$21	Offset Register 0
ADCB_OFS 1	$22	Offset Register 1
ADCB_OFS 2	$23	Offset Register 2
ADCB_OFS 3	$24	Offset Register 3
ADCB_OFS 4	$25	Offset Register 4
ADCB_OFS 5	$26	Offset Register 5
ADCB_OFS 6	$27	Offset Register 6
ADCB_OFS 7	$28	Offset Register 7
ADCB_POWER	$29	Power Control Register
ADCB_CAL	$2A	ADC Calibration Register

Table 4-22 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270)

Temperature Sensor is NOT available in the 56F8147 device

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-23 Serial Communication Interface 0 Registers Address Map (SCI0_BASE = $00 F280)

Register Acronym	Address Offset	Register Description
SCI0_SCIBR	$0	Baud Rate Register
SCI0_SCICR	$1	Control Register
		Reserved
SCI0_SCISR	$3	Status Register
SCI0_SCIDR	$4	Data Register

Table 4-38 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8147 device

Register Acronym	Address Offset	Register Description
FCMB5_DATA	$6B	Message Buffer 5 Data Register
FCMB5_DATA	$6C	Message Buffer 5 Data Register
FCMB5_DATA	$6D	Message Buffer 5 Data Register
FCMB5_DATA	$6E	Message Buffer 5 Data Register
		Reserved
FCMB6_CONTROL	$70	Message Buffer 6 Control / Status Register
FCMB6_ID_HIGH	$71	Message Buffer 6 ID High Register
FCMB6_ID_LOW	$72	Message Buffer 6 ID Low Register
FCMB6_DATA	$73	Message Buffer 6 Data Register
FCMB6_DATA	$74	Message Buffer 6 Data Register
FCMB6_DATA	$75	Message Buffer 6 Data Register
FCMB6_DATA	$76	Message Buffer 6 Data Register
		Reserved
FCMB7_CONTROL	$78	Message Buffer 7 Control / Status Register
FCMB7_ID_HIGH	$79	Message Buffer 7 ID High Register
FCMB7_ID_LOW	$7A	Message Buffer 7 ID Low Register
FCMB7_DATA	$7B	Message Buffer 7 Data Register
FCMB7_DATA	$7C	Message Buffer 7 Data Register
FCMB7_DATA	$7D	Message Buffer 7 Data Register
FCMB7_DATA	$7E	Message Buffer 7 Data Register
		Reserved
FCMB8_CONTROL	$80	Message Buffer 8 Control / Status Register
FCMB8_ID_HIGH	$81	Message Buffer 8 ID High Register
FCMB8_ID_LOW	$82	Message Buffer 8 ID Low Register
FCMB8_DATA	$83	Message Buffer 8 Data Register
FCMB8_DATA	$84	Message Buffer 8 Data Register
FCMB8_DATA	$85	Message Buffer 8 Data Register
FCMB8_DATA	$86	Message Buffer 8 Data Register
		Reserved
FCMB9_CONTROL	$88	Message Buffer 9 Control / Status Register
FCMB9_ID_HIGH	$89	Message Buffer 9 ID High Register
FCMB9_ID_LOW	$8A	Message Buffer 9 ID Low Register

Table 5-2. Interrupt Priority Encoding

IPIC_LEVEL[1:0][1]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No Interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
01	Priority 1	Priorities 2, 3
11	Priorities 2 or 3	Priority 3

1. See IPIC field definition in Part 5.6.30.2

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIMn register to the appropriate vector number
3. Setting the FIVALn and FIVAHn registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the ITCN handles it as a fast interrupt. The ITCN takes the vector address from the appropriate FIVALn and FIVAHn registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector adddress and if it is not a JSR, the core starts its fast interrupt handling.

5.4 Block Diagram

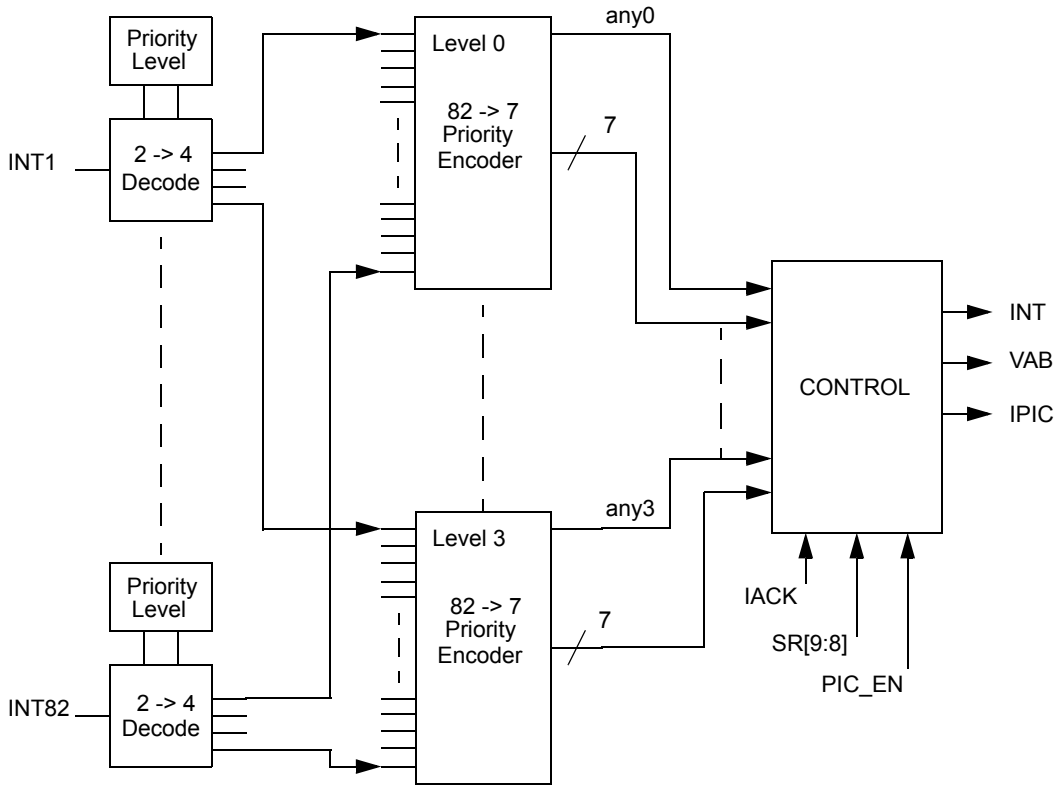


Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode. Also, the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ signals automatically become low-level sensitive in these modes even if the control register bits are set to make them falling-edge sensitive. This is because there is no clock available to detect the falling edge.

  A peripheral which requires a clock to generate interrupts will not be able to generate interrupts during Stop mode. The FlexCAN module can wake the device from Stop mode, and a reset will do just that, or $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ can wake it up.

5.6.17.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.17.2 Fast Interrupt 1 Vector Address High (FIVAH1)—Bits 4–0

The upper five bits of the vector address are used for Fast Interrupt 1. This register is combined with FIVAL1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.18 IRQ Pending 0 Register (IRQP0)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending 0 Register (IRQP0)

5.6.18.1 IRQ Pending (PENDING)—Bits 16–2

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.18.2 Reserved—Bit 0

This bit is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.19 IRQ Pending 1 Register (IRQP1)

$Base + $12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [32:17]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-21 IRQ Pending 1 Register (IRQP1)

5.6.19.1 IRQ Pending (PENDING)—Bits 32–17

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

6.3 Operating Modes

Since the SIM is responsible for distributing clocks and resets across the chip, it must understand the various chip operating modes and take appropriate action. These are:

- **Reset Mode,** which has two submodes:
  - — POR and $\overline{\text{RESET}}$ operation
    The 56800E core and all peripherals are reset. This occurs when the internal POR is asserted or the $\overline{\text{RESET}}$ pin is asserted.
  - — COP reset and software reset operation
    The 56800E core and all peripherals are reset. The MA bit within the OMR is not changed. This allows the software to determine the boot mode (internal or external boot) to be used on the next reset.
- **Run Mode**
  This is the primary mode of operation for this device. In this mode, the 56800E controls chip operation.
- **Debug Mode**
  The 56800E is controlled via JTAG/EOnCE when in debug mode. All peripherals, except the COP and PWMs, continue to run. COP is disabled and PWM outputs are optionally switched off to disable any motor from being driven; see the PWM chapter in the **56F8300 Peripheral User Manual** for details.
- **Wait Mode**
  In Wait mode, the core clock and memory clocks are disabled. Optionally, the COP can be stopped. Similarly, it is an option to switch off PWM outputs to disable any motor from being driven. All other peripherals continue to run.
- **Stop Mode**
  When in Stop mode, the 56800E core, memory, and most peripheral clocks are shut down. Optionally, the COP and CAN can be stopped. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. The CAN (along with any non-gated interrupt) is capable of waking the chip up from Stop mode, but is not fully functional in Stop mode.

6.4 Operating Mode Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NL							CM	XP	SD	R	SA	EX	0	MB	MA
Type	R/W							R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X

Figure 6-1 OMR

The reset state for MB and MA will depend on the Flash secured state. See **Part 4.2** and **Part 7** for detailed information on how the Operating Mode Register (OMR) MA and MB bits operate in this device. For all other bits, see the **DSP56800E Reference Manual**.

Note: The OMR is not a Memory Map register; it is directly accessible in code through the acronym OMR.

6.5.1.2 EMI_MODE (EMI_MODE)—Bit 6

This bit reflects the current (non-clocked) state of the EMI_MODE pin. During reset, this bit, coupled with the EXTBOOT signal, is used to initialize address bits [19:16] either as GPIO or as address. These settings can be explicitly overwritten using the appropriate GPIO peripheral enable register at any time after reset. In addition, this pin can be used as a general purpose input pin after reset.

- 0 = External address bits [19:16] are initially programmed as GPIO
- 1 = When booted with EXTBOOT = 1, A[19:16] are initially programmed as address. If EXTBOOT is 0, they are initialized as GPIO.

6.5.1.3 OnCE Enable (OnCE EBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.5.1.4 Software Reset (SW RST)—Bit 4

This bit is always read as 0. Writing a 1 to this bit will cause the part to reset.

6.5.1.5 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 - Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can be reprogrammed in the future
- 10 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can then only be changed by resetting the device
- 11 - Same operation as 10

6.5.1.6 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 - Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 - The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can be reprogrammed in the future
- 10 - The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can then only be changed by resetting the device
- 11 - Same operation as 10

6.5.2 SIM Reset Status Register (SIM_RSTSTS)

Bits in this register are set upon any system reset and are initialized only by a Power-On Reset (POR). A reset (other than POR) will only set bits in the register; bits are not cleared. Only software should only clear this register.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-4 SIM Reset Status Register (SIM_RSTSTS)

10.9 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 10-17 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	10-5
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16T	—	ns	10-5
$\overline{\text{RESET}}$ Deassertion to First External Address Output[3]	t_{RDA}	63T	64T	ns	10-5
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	10-6
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	18T	—	ns	10-7
	$t_{IDM - FAST}$	14T	—		
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	10-7
	$t_{IG - FAST}$	14T	—		
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Wait) to External Data Memory Access[4]	t_{IRI}	22T	—	ns	10-8
	$t_{IRI -FAST}$	18T	—		
Delay from $\overline{\text{IRQA}}$ Assertion to External Data Memory Access (exiting Stop)	t_{IF}	22T	—	ns	10-9
	$t_{IF - FAST}$	18T	—		
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[5]	t_{IW}	1.5T	—	ns	10-9

1. In the formulas, T = clock cycle. For an operating frequency of 60MHz, T = 16.67ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. During Power-On Reset, it is possible to use the device's internal reset stretching circuitry to extend this period to 2^{21}T.
4. The minimum is specified for the duration of an edge-sensitive $\overline{\text{IRQA}}$ interrupt required to recover from the Stop state. This is not the minimum required so that the $\overline{\text{IRQA}}$ interrupt is accepted.
5. The interrupt instruction fetch is visible on the pins only in Mode 3.

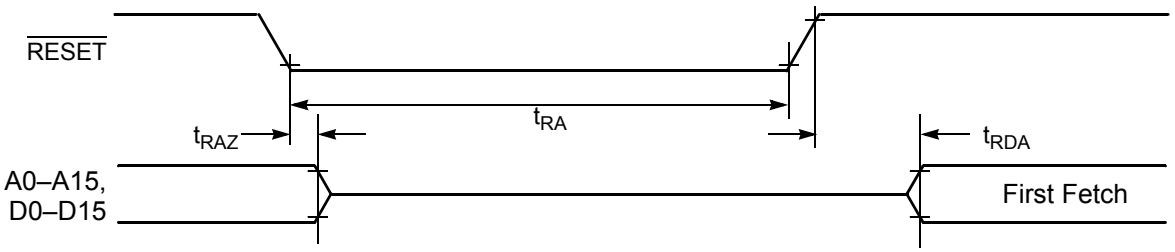


Figure 10-5 Asynchronous Reset Timing

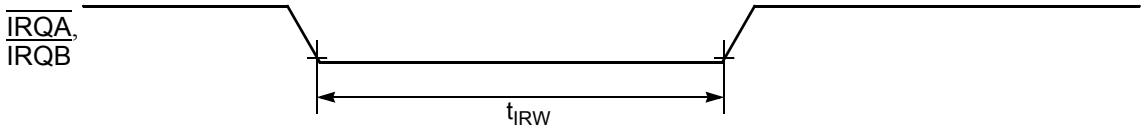


Figure 10-6 External Interrupt Timing (Negative-Edge Sensitive)

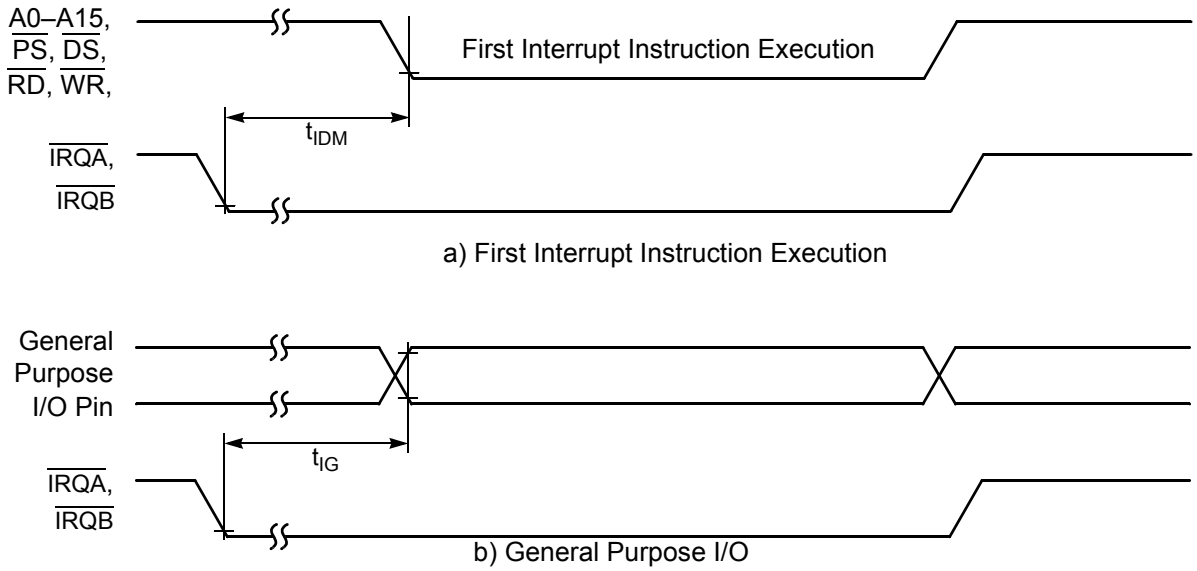


Figure 10-7 External Level-Sensitive Interrupt Timing

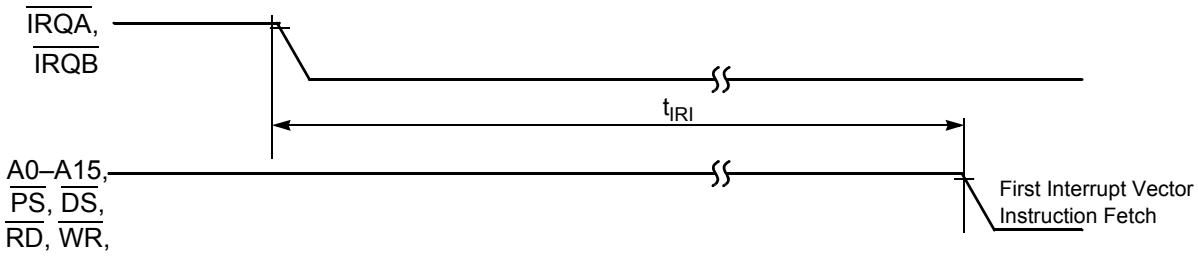


Figure 10-8 Interrupt from Wait State Timing

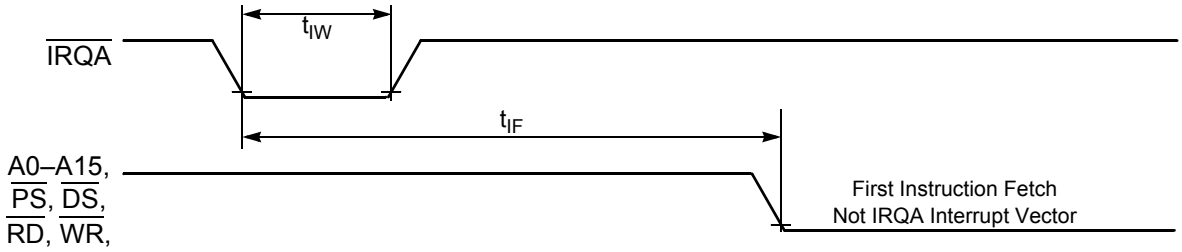


Figure 10-9 Recovery from Stop State Using Asynchronous Interrupt Timing

10.10 Serial Peripheral Interface (SPI) Timing

Table 10-18 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	10-10, 10-11, 10-12, 10-13
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	10-13
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	10-13
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	10-10, 10-11, 10-12, 10-13

Table 11-1 56F8347 160-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{DD_IO}	41	V_{SS}	81	PWMA5	121	ANB5
2	$V_{PP}2$	42	V_{DD_IO}	82	FAULTA0	122	ANB6
3	CLKO	43	PWMB3	83	D2	123	ANB7
4	TXD0	44	PWMB4	84	FAULTA1	124	EXTBOOT
5	RXD0	45	PWMB5	85	FAULTA2	125	V_{SS}
6	PHASEA1	46	GPIOB5	86	D3	126	ISA0
7	PHASEB1	47	GPIOB6	87	FAULTA3	127	ISA1
8	INDEX1	48	GPIOB7	88	D4	128	ISA2
9	HOME1	49	TXD1	89	D5	129	TD0
10	A1	50	RXD1	90	D6	130	TD1
11	A2	51	$\overline{WR}$	91	OCR_DIS	131	TD2
12	A3	52	$\overline{RD}$	92	$V_{DDA\_OSC\_PLL}$	132	TD3
13	A4	53	$\overline{PS}$	93	XTAL	133	TC0
14	A5	54	$\overline{DS}$	94	EXTAL	134	V_{DD_IO}
15	$V_{CAP}4$*	55	GPIOD0	95	$V_{CAP}3$*	135	TC1
16	V_{DD_IO}	56	GPIOD1	96	V_{DD_IO}	136	$\overline{TRST}$
17	A6	57	GPIOD2	97	$\overline{RSTO}$	137	TCK
18	A7	58	GPIOD3	98	$\overline{RESET}$	138	TMS
19	A8	59	GPIOD4	99	CLKMODE	139	TDI
20	A9	60	GPIOD5	100	ANA0	140	TDO
21	A10	61	ISB0	101	ANA1	141	$V_{PP}1$
22	A11	62	$V_{CAP}1$*	102	ANA2	142	CAN_TX
23	A12	63	ISB1	103	ANA3	143	CAN_RX
24	A13	64	ISB2	104	ANA4	144	$V_{CAP}2$*
25	A14	65	$\overline{IRQA}$	105	ANA5	145	$\overline{SS0}$

* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

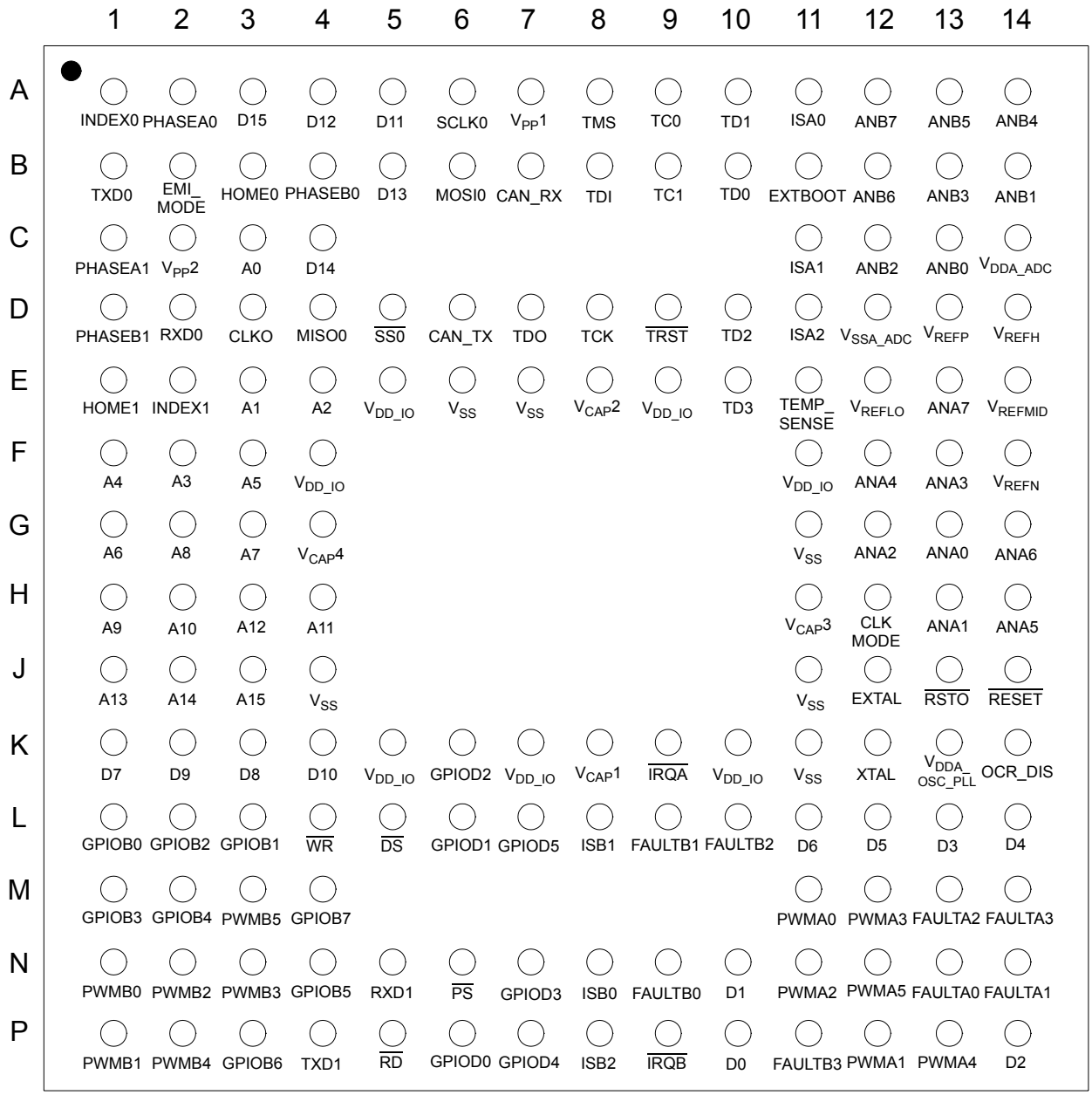


Figure 11-2 Top View, 56F8347 160-Pin MAPBGA Package

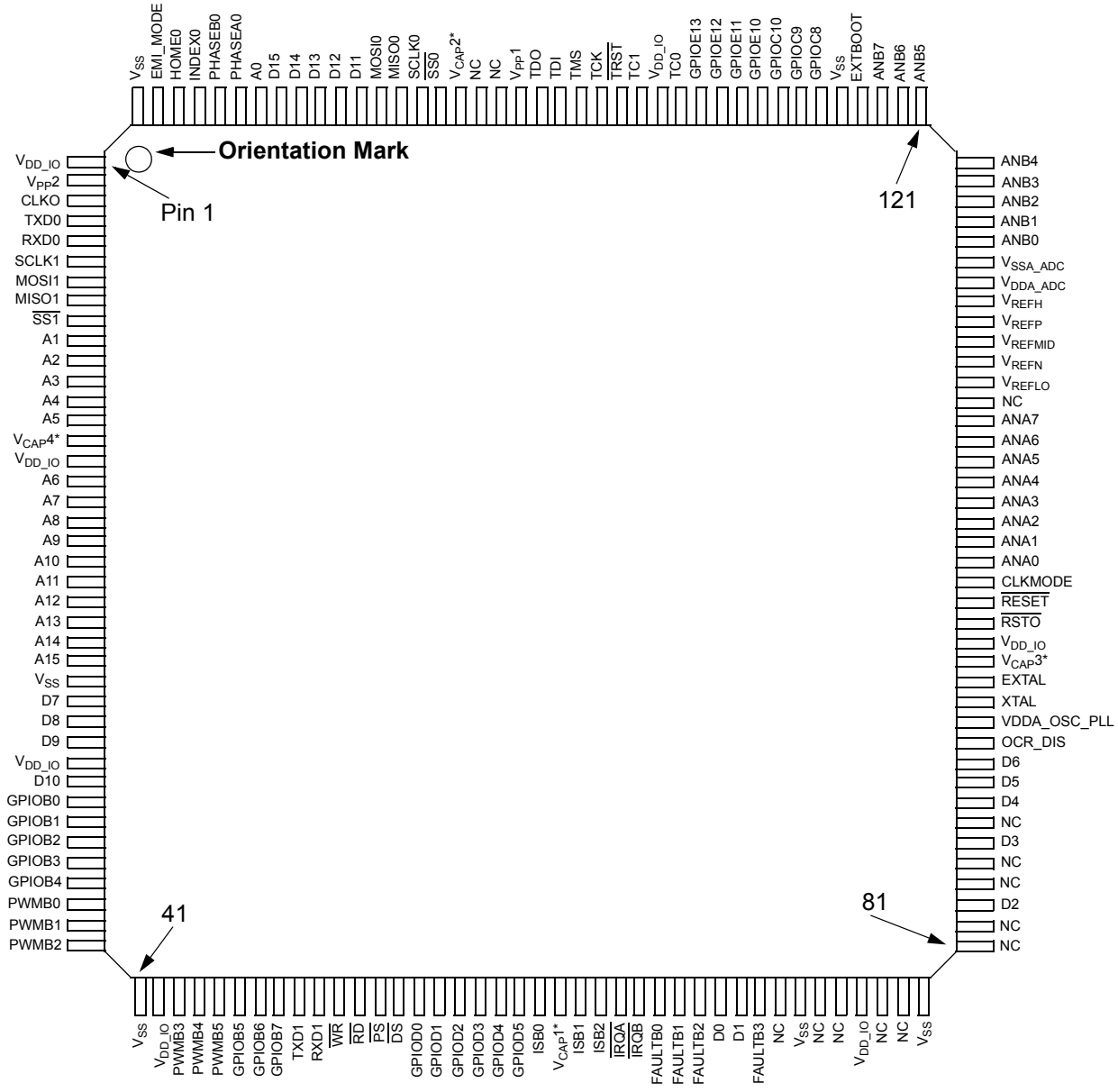
Table 11-2 56F8347 -160 MAPBGA Package Identification by Pin Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
F4	V_{DD_IO}	K11	V_{SS}	N12	PWMA5	A13	ANB5
C2	$V_{PP}2$	K7	V_{DD_IO}	N13	FAULTA0	B12	ANB6
D3	CLKO	N3	PWMB3	P14	D2	A12	ANB7
B1	TXD0	P2	PWMB4	N14	FAULTA1	B11	EXTBOOT
D2	RXD0	M3	PWMB5	M13	FAULTA2	J11	V_{SS}
C1	PHASEA1	N4	GPIOB5	L13	D3	A11	ISA0
D1	PHASEB1	P3	GPIOB6	M14	FAULTA3	C11	ISA1
E2	INDEX1	M4	GPIOB7	L14	D4	D11	ISA2
E1	HOME1	P4	TXD1	L12	D5	B10	TD0
E3	A1	N5	RXD1	L11	D6	A10	TD1
E4	A2	L4	$\overline{WR}$	K14	OCR_DIS	D10	TD2
F2	A3	P5	$\overline{RD}$	K13	$V_{DDA\_OSC\_PLL}$	E10	TD3
F1	A4	N6	$\overline{PS}$	K12	XTAL	A9	TC0
F3	A5	L5	$\overline{DS}$	J12	EXTAL	F11	V_{DD_IO}
G4	$V_{CAP}4$*	P6	GPIOD0	H11	$V_{CAP}3$*	B9	TC1
K5	V_{DD_IO}	L6	GPIOD1	K10	V_{DD_IO}	D9	$\overline{TRST}$
G1	A6	K6	GPIOD2	J13	$\overline{RSTO}$	D8	TCK
G3	A7	N7	GPIOD3	J14	$\overline{RESET}$	A8	TMS
G2	A8	P7	GPIOD4	H12	CLKMODE	B8	TDI
H1	A9	L7	GPIOD5	G13	ANA0	D7	TDO
H2	A10	N8	ISB0	H13	ANA1	A7	$V_{PP}1$
H4	A11	K8	$V_{CAP}1$*	G12	ANA2	D6	CAN_TX
H3	A12	L8	ISB1	F13	ANA3	B7	CAN_RX
J1	A13	P8	ISB2	F12	ANA4	E8	$V_{CAP}2$*
J2	A14	K9	$\overline{IRQA}$	H14	ANA5	D5	$\overline{SS0}$

* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

11.2 56F8147 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8147. This device comes in a 160-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-4** shows the package outline for the 160-pin LQFP, **Figure 11-5** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 160-pin LQFP.



* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

Figure 11-4 Top View, 56F8147 160-Pin LQFP Package