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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8347vvfe

Document Revision History

Version History	Description of Change
Rev 0	Initial release
Rev 1.0	Fixed typos in Section 1.1.3, Replace any reference to Flash Interface Unit with Flash Module, corrected pin number for D14 in **Table 2-2**, added note to Vcap pin in **Table 2-2**, corrected thermal numbers for 160 LQFP in **Table 10-4**,removed unneccessary notes in **Table 10-13**; corrected temperature range in **Table 10-14**; added ADC calibration information to **Table 10-24** and new graphs in **Figure 10-22**.
Rev 2.0	Clarification to **Table 10-23**, corrected Digital Input Current Low (pull-up enabled) numbers in **Table 10-5**. Removed text and Table 10-2; replaced with note to **Table 10-1**.
Rev 3.0	Added 56F8147 information; edited to indicate differences in 56F8347 and 56F8147. Reformatted for Freescale look and feel. Updated Temperature Sensor and ADC tables, then updaated balance of electrical tables for consistency throughout the family. Clarified I/O power description in **Table 2-2**, added note to **Table 10-7** and clarified **Section 12.3**.
Rev 4.0	Correcting **Figure 4-1** Boot Flash Start = $02_0000
Rev 5.0	Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed P_D in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**.
Rev 6.0	Added 160MAPBGA information, TA equation updated in **Table 10-4** and additional minor edits throughout data sheet
Rev 7.0	Updated **Table 10-24** to reflect new value for maximum Uncalibrated Gain Error
Rev 8.0	Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) and corrected Flash Endurance to 10,000 in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover.
Rev 9.0	Corrected **Section 6.4** title (from Operation Mode Register to Operating Mode Register). Updated JTAG ID in **Section 6.5.4**. Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 10.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev. 11	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{\text{TRST}}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.

Please see http://www.freescale.com for the most current data sheet revision.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
$\overline{\text{WR}}$	51	L4	Output	In reset, output is disabled, pull-up is enabled	**Write Enable** — $\overline{\text{WR}}$ is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low, pins D0 - D15 become outputs and the device puts data on the bus. When $\overline{\text{WR}}$ is deasserted high, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0 - A16, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a static RAM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{WR}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.
$\overline{\text{PS}}$ **($\overline{\text{CS0}}$)** **(GPIOD8)**	53	N6	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Program Memory Select** — This signal is actually $\overline{\text{CS0}}$ in the EMI, which is programmed at reset for compatibility with the 56F80x $\overline{\text{PS}}$ signal. $\overline{\text{PS}}$ is asserted low for external program memory access. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{CS0}}$ is tri-stated when the external bus is inactive. $\overline{\text{CS0}}$ resets to provide the $\overline{\text{PS}}$ function as defined on the 56F80x devices. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. To deactivate the internal pull-up resistor, clear bit 8 in the GPIOD_PUR register.
$\overline{\text{DS}}$ **($\overline{\text{CS1}}$)** **(GPIOD9)**	54	L5	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Memory Select** — This signal is actually $\overline{\text{CS1}}$ in the EMI, which is programmed at reset for compatibility with the 56F80x $\overline{\text{DS}}$ signal. $\overline{\text{DS}}$ is asserted low for external data memory access. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A0 - A23 and EMI control signals are tri-stated when the external bus is inactive. $\overline{\text{CS1}}$ resets to provide the $\overline{\text{DS}}$ function as defined on the 56F80x devices. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. To deactivate the internal pull-up resistor, clear bit 9 in the GPIOD_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
GPIOD0 **($\overline{\text{CS2}}$)**	55	P6	Input/ Output Output	Input, pull-up enabled	**Port D GPIO** — These six GPIO pins can be individually programmed as input or output pins. **Chip Select** — $\overline{\text{CS2}}$ - $\overline{\text{CS7}}$ may be programmed within the EMI module to act as chip selects for specific areas of the external memory map. Depending upon the state of the DRV bit in the EMI Bus Control Register (BCR), $\overline{\text{CS2}}$ - $\overline{\text{CS7}}$ are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. At reset, these pins are configured as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOD_PUR register. Example: GPIOD0, clear bit 0 in the GPIOD_PUR register.
GPIOD1 ($\overline{\text{CS3}}$)	56	L6			
GPIOD2 ($\overline{\text{CS4}}$)	57	K6			
GPIOD3 ($\overline{\text{CS5}}$)	58	N7			
GPIOD4 ($\overline{\text{CS6}}$)	59	P7			
GPIOD5 ($\overline{\text{CS7}}$)	60	L7			
TXD0 **(GPIOE0)**	4	B1	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI0 transmit data output **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOE_PUR register.
RXD0 **(GPIOE1)**	5	D2	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI0 receive data input **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
MOSI0 **(GPIOE5)**	148	B6	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0. To deactivate the internal pull-up resistor, clear bit 5 in the GPIOE_PUR register.
MISO0 **(GPIOE6)**	147	D4	Input/ Output Input/ Output	Input, pull-up enabled	**SPI 0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MISO0. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOE_PUR register.
$\overline{\text{SS0}}$ **(GPIOE7)**	145	D5	Input Input/ Output	Input, pull-up enabled	**SPI 0 Slave Select** — $\overline{\text{SS0}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. **Port E GPIO** — This GPIO pin can be individually programmed as input or output pin. After reset, the default state is $\overline{\text{SS0}}$. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
ANB0	116	C13	Input	Analog Input	**ANB0 - 3** — Analog inputs to ADC B, channel 0
ANB1	117	B14			
ANB2	118	C12			
ANB3	119	B13			
ANB4	120	A14	Input	Analog Input	**ANB4 - 7** — Analog inputs to ADC B, channel 1
ANB5	121	A13			
ANB6	122	B12			
ANB7	123	A12			
TEMP_ SENSE	108	E11	Output	Analog Output	**Temperature Sense Diode** — This signal connects to an on-chip diode that can be connected to one of the ADC inputs and used to monitor the temperature of the die. Must be bypassed with a 0.01μF capacitor.
CAN_RX	143	B7	Schmitt Input	Input, pull-up enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pull-up resistor. To deactivate the internal pull-up resistor, set the CAN bit in the SIM_PUDR register.
CAN_TX	142	D6	Open Drain Output	Open Drain Output	**FlexCAN Transmit Data** — CAN output with internal pull-u[enable at reset.* * **Note:** If a pin is configured as open drain output mode, internal pull-up will automatically be disabled when it outputs low. Internal pull-up will be enabled unless it has been manually disabled by clearing the corresponding bit in the PUREN register of the GPIO module, when it outputs high. If a pin is configured as push-pull output mode, internal pull-up will automatically be disabled, whether it outputs low or high.
TC0 **(GPIOE8)**	133	A9	Schmitt Input/ Output Schmitt Input/ Outpu	Input, pull-up enabled	**TC0 - 1**— Timer C, Channel 0 and 1 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pull-up resistor, clear bit 8 of the GPIOE_PUR register.
TC1 (GPIOE9)	135	B9			

4.2 Program Map

The operating mode control bits (MA and MB) in the Operating Mode Register (OMR) control the Program memory map. At reset, these bits are set as indicated in Table 4-2. Table 4-4 shows the memory map configurations that are possible at reset. After reset, the OMR MA bit can be changed and will have an effect on the P-space memory map, as shown in Table 4-3. Changing the OMR MB bit will have no effect.

Table 4-2 OMR MB/MA Value at Reset

OMR MB = Flash Secured State[1, 2]	OMR MA = EXTBOOT Pin	Chip Operating Mode
0	0	Mode 0 – Internal Boot; EMI are configured to use 16 address lines; Flash Memory is secured; external P-space is not allowed; the EOnCE is disabled
0	1	Not valid; cannot boot externally if the Flash is secured and will actually configure to 00 state
1	0	Mode 0 – Internal Boot; EMI is configured to use 16 address lines
1	1	Mode 1 – External Boot; Flash Memory is not secured; EMI configuration is determined by the state of the EMI_MODE pin

1. This bit is only configured at reset. If the Flash secured state changes, this will not be reflected in MB until the next reset.
2. Changing MB in software will not affect Flash memory security.

Table 4-3 Changing OMR MA Value During Normal Operation

OMR MA	Chip Operating Mode
0	Use internal P-space memory map configuration
1	Use external P-space memory map configuration – If MB = 0 at reset, changing this bit has no effect.

The device's external memory interface (EMI) can operate much like the 56F80x family's EMI, or it can be operated in a mode similar to that used on other products in the 56800E family. Initially, $\overline{CS0}$ and $\overline{CS1}$ are configured as $\overline{PS}$ and $\overline{DS}$, in a mode compatible with earlier 56800 devices.

Eighteen address lines are required to shadow the first 192K of internal program space when booting externally for development purposes. Therefore, the entire complement of on-chip memory cannot be accessed using a 16-bit 56800-compatible address bus. To address this situation, the EMI_MODE pin can be used to configure four GPIO pins as Address[19:16] upon reset (Software reconfiguration of the highest address lines [A20-23] is required if the full address range is to be used.)

The EMI_MODE pin also affects the reset vector address, as provided in Table 4-4**.** Additional pins must be configured as address or chip select signals to access addresses at P:$10 0000 and above.

Note: *Program RAM is NOT available on the 56F8147 device.*

Table 4-5 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
GPIOD	32	0-2	P:$40	GPIOD
GPIOC	33	0-2	P:$42	GPIOC
GPIOB	34	0-2	P:$44	GPIOB
GPIOA	35	0-2	P:$46	GPIOA
				Reserved
SPI1	38	0-2	P:$4C	SPI 1 Receiver Full
SPI1	39	0-2	P:$4E	SPI 1 Transmitter Empty
SPI0	40	0-2	P:$50	SPI 0 Receiver Full
SPI0	41	0-2	P:$52	SPI 0 Transmitter Empty
SCI1	42	0-2	P:$54	SCI 1 Transmitter Empty
SCI1	43	0-2	P:$56	SCI 1 Transmitter Idle
				Reserved
SCI1	45	0-2	P:$5A	SCI 1 Receiver Error
SCI1	46	0-2	P:$5C	SCI 1 Receiver Full
DEC1	47	0-2	P:$5E	Quadrature Decoder #1 Home Switch or Watchdog
DEC1	48	0-2	P:$60	Quadrature Decoder #1 INDEX Pulse
DEC0	49	0-2	P:$62	Quadrature Decoder #0 Home Switch or Watchdog
DEC0	50	0-2	P:$64	Quadrature Decoder #0 INDEX Pulse
				Reserved
TMRD	52	0-2	P:$68	Timer D, Channel 0
TMRD	53	0-2	P:$6A	Timer D, Channel 1
TMRD	54	0-2	P:$6C	Timer D, Channel 2
TMRD	55	0-2	P:$6E	Timer D, Channel 3
TMRC	56	0-2	P:$70	Timer C, Channel 0
TMRC	57	0-2	P:$72	Timer C, Channel 1
TMRC	58	0-2	P:$74	Timer C, Channel 2
TMRC	59	0-2	P:$76	Timer C, Channel 3
TMRB	60	0-2	P:$78	Timer B, Channel 0
TMRB	61	0-2	P:$7A	Timer B, Channel 1
TMRB	62	0-2	P:$7C	Timer B, Channel 2
TMRB	63	0-2	P:$7E	Timer B, Channel 3
TMRA	64	0-2	P:$80	Timer A, Channel 0
TMRA	65	0-2	P:$82	Timer A, Channel 1
TMRA	66	0-2	P:$84	Timer A, Channel 2
TMRA	67	0-2	P:$86	Timer A, Channel 3

Table 4-10 External Memory Integration Registers Address Map (Continued) (EMI_BASE = $00 F020)

Register Acronym	Address Offset	Register Description	Reset Value
CSOR 4	$C	Chip Select Option Register 4	
CSOR 5	$D	Chip Select Option Register 5	
CSOR 6	$E	Chip Select Option Register 6	
CSOR 7	$F	Chip Select Option Register 7	
CSTC 0	$10	Chip Select Timing Control Register 0	
CSTC 1	$11	Chip Select Timing Control Register 1	
CSTC 2	$12	Chip Select Timing Control Register 2	
CSTC 3	$13	Chip Select Timing Control Register 3	
CSTC 4	$14	Chip Select Timing Control Register 4	
CSTC 5	$15	Chip Select Timing Control Register 5	
CSTC 6	$16	Chip Select Timing Control Register 6	
CSTC 7	$17	Chip Select Timing Control Register 7	
BCR	$18	Bus Control Register	0x016B sets the default number of wait states to 11 for both read and write accesses

Table 4-11 Quad Timer A Registers Address Map (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMP1	$0	Compare Register 1
TMRA0_CMP2	$1	Compare Register 2
TMRA0_CAP	$2	Capture Register
TMRA0_LOAD	$3	Load Register
TMRA0_HOLD	$4	Hold Register
TMRA0_CNTR	$5	Counter Register
TMRA0_CTRL	$6	Control Register
TMRA0_SCR	$7	Status and Control Register
TMRA0_CMPLD1	$8	Comparator Load Register 1
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_COMSCR	$A	Comparator Status and Control Register
		Reserve
TMRA1_CMP1	$10	Compare Register 1
TMRA1_CMP2	$11	Compare Register 2
TMRA1_CAP	$12	Capture Register
TMRA1_LOAD	$13	Load Register

Table 4-13 Quad Timer C Registers Address Map (Continued) (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register
TMRC1_HOLD	$14	Hold Register
TMRC1_CNTR	$15	Counter Register
TMRC1_CTRL	$16	Control Register
TMRC1_SCR	$17	Status and Control Register
TMRC1_CMPLD1	$18	Comparator Load Register 1
TMRC1_CMPLD2	$19	Comparator Load Register 2
TMRC1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRC2_CMP1	$20	Compare Register 1
TMRC2_CMP2	$21	Compare Register 2
TMRC2_CAP	$22	Capture Register
TMRC2_LOAD	$23	Load Register
TMRC2_HOLD	$24	Hold Register
TMRC2_CNTR	$25	Counter Register
TMRC2_CTRL	$26	Control Register
TMRC2_SCR	$27	Status and Control Register
TMRC2_CMPLD1	$28	Comparator Load Register 1
TMRC2_CMPLD2	$29	Comparator Load Register 2
TMRC2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRC3_CMP1	$30	Compare Register 1
TMRC3_CMP2	$31	Compare Register 2
TMRC3_CAP	$32	Capture Register
TMRC3_LOAD	$33	Load Register
TMRC3_HOLD	$34	Hold Register
TMRC3_CNTR	$35	Counter Register
TMRC3_CTRL	$36	Control Register
TMRC3_SCR	$37	Status and Control Register
TMRC3_CMPLD1	$38	Comparator Load Register 1
TMRC3_CMPLD2	$39	Comparator Load Register 2
TMRC3_COMSCR	$3A	Comparator Status and Control Register

Table 4-20 Analog-to-Digital Converter Registers Address Map (Continued) (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_OFS 5	$26	Offset Register 5
ADCA_OFS 6	$27	Offset Register 6
ADCA_OFS 7	$28	Offset Register 7
ADCA_POWER	$29	Power Control Register
ADCA_CAL	$2A	ADC Calibration Register

Table 4-21 Analog-to-Digital Converter Registers Address Map (ADCB_BASE = $00 F240)

Register Acronym	Address Offset	Register Description
ADCB_CR 1	$0	Control Register 1
ADCB_CR 2	$1	Control Register 2
ADCB_ZCC	$2	Zero Crossing Control Register
ADCB_LST 1	$3	Channel List Register 1
ADCB_LST 2	$4	Channel List Register 2
ADCB_SDIS	$5	Sample Disable Register
ADCB_STAT	$6	Status Register
ADCB_LSTAT	$7	Limit Status Register
ADCB_ZCSTAT	$8	Zero Crossing Status Register
ADCB_RSLT 0	$9	Result Register 0
ADCB_RSLT 1	$A	Result Register 1
ADCB_RSLT 2	$B	Result Register 2
ADCB_RSLT 3	$C	Result Register 3
ADCB_RSLT 4	$D	Result Register 4
ADCB_RSLT 5	$E	Result Register 5
ADCB_RSLT 6	$F	Result Register 6
ADCB_RSLT 7	$10	Result Register 7
ADCB_LLMT 0	$11	Low Limit Register 0
ADCB_LLMT 1	$12	Low Limit Register 1
ADCB_LLMT 2	$13	Low Limit Register 2
ADCB_LLMT 3	$14	Low Limit Register 3
ADCB_LLMT 4	$15	Low Limit Register 4
ADCB_LLMT 5	$16	Low Limit Register 5
ADCB_LLMT 6	$17	Low Limit Register 6
ADCB_LLMT 7	$18	Low Limit Register 7
ADCB_HLMT 0	$19	High Limit Register 0

5.6.5.3 SPI1 Receiver Full Interrupt Priority Level (SPI1_RCV IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.4 Reserved—Bits 9–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.5.5 GPIOA Interrupt Priority Level (GPIOA IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.6 GPIOB Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.7 GPIOC Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources (RESET pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $11F4.

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
Write																
RESET	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Figure 6-6 Most Significant Half of JTAG ID (SIM_MSH_ID)

6.5.5 Least Significant Half of JTAG ID (SIM_LSH_ID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $401D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-7 Least Significant Half of JTAG ID (SIM_LSH_ID)

6.5.6 SIM Pull-up Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pull-up resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pull-ups disabled by setting the appropriate bit in this register. Disabling pull-ups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See **Table 2-2** to identify which pins can deactivate the internal pull-up resistor.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	PWMA1	CAN	EMI_ MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA0	0	CTRL	0	JTAG	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8 SIM Pull-up Disable Register (SIM_PUDR)

6.5.6.1 Reserved—Bit 15

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.2 PWMA1—Bit 14

This bit controls the pull-up resistors on the FAULTA3 pin.

6.5.6.3 CAN—Bit 13

This bit controls the pull-up resistors on the CAN_RX pin.

6.5.6.4 EMI_MODE—Bit 12

This bit controls the pull-up resistors on the EMI_MODE pin.

6.5.6.5 $\overline{\text{RESET}}$—Bit 11

This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.6 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ pins.

6.5.6.7 XBOOT—Bit 9

This bit controls the pull-up resistors on the EXTBOOT pin.

6.5.6.8 PWMB—Bit 8

This bit controls the pull-up resistors on the FAULTB0, FAULTB1, FAULTB2, and FAULTB3 pins.

6.5.6.9 PWMA0—Bit 7

This bit controls the pull-up resistors on the FAULTA0, FAULTA1, and FAULTA2 pins.

6.5.6.10 Reserved—Bit 6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.11 CTRL—Bit 5

This bit controls the pull-up resistors on the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins.

6.5.6.12 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.13 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{\text{TRST}}$, TMS and TDI pins.

6.5.6.14 Reserved—Bits 2 - 0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

6.8 Stop and Wait Mode Disable Function

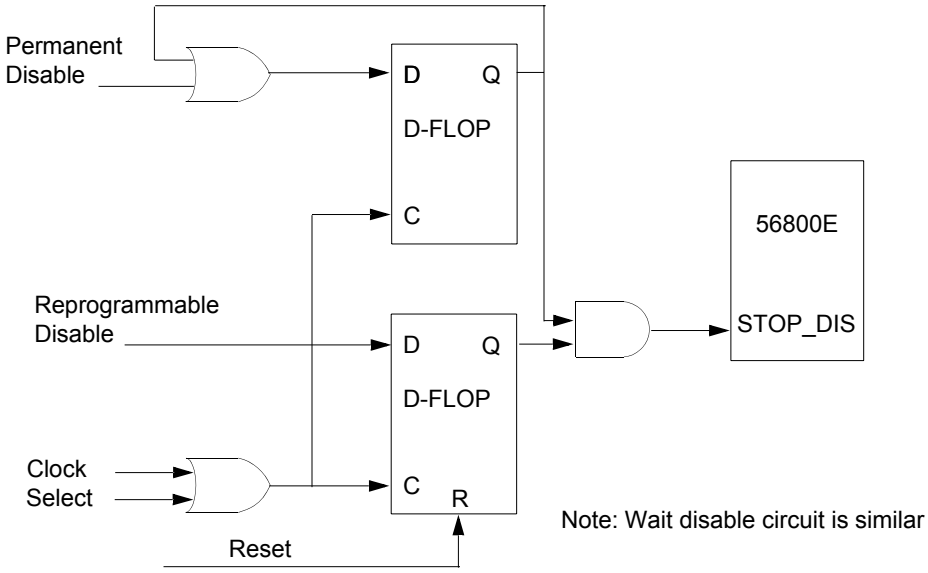


Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the oscillator output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL), described in **Part 6.5.1**. This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing to the SIM_CONTROL register and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is first extended for 2^{21} clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and,

Table 8-3 GPIO External Signals Map (Continued)
Pins in italics are NOT available in the 56F8147 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin
GPIOC	0	Peripheral	*PhaseA1 / TB0* / SCLK1[1]	6
	1	Peripheral	*PhaseB1 / TB1* / MOSI1[1]	7
	2	Peripheral	*Index1 / TB2* / MISO1[1]	8
	3	Peripheral	*Home1 / TB3* / $\overline{\text{SSI1}}$[1]	9
	4	Peripheral	PHASEA0 / TA0	155
	5	Peripheral	PHASEB0 / TA1	156
	6	Peripheral	Index0 / TA2	157
	7	Peripheral	Home0 / TA3	158
	8	Peripheral	*ISA0*	126
	9	Peripheral	*ISA1*	127
	10	Peripheral	*ISA2*	128
GPIOD	0	GPIO	$\overline{\text{CS2}}$	55
	1	GPIO	$\overline{\text{CS3}}$	56
	2	GPIO	$\overline{\text{CS4}}$	57
	3	GPIO	$\overline{\text{CS5}}$	58
	4	GPIO	$\overline{\text{CS6}}$	59
	5	GPIO	$\overline{\text{CS7}}$	60
	6	Peripheral	TXD1	49
	7	Peripheral	RXD1	50
	8	Peripheral	$\overline{\text{PS}}$ / $\overline{\text{CS0}}$	53
	9	Peripheral	$\overline{\text{DS}}$ / $\overline{\text{CS1}}$	54
	10	Peripheral	ISB0	61
	11	Peripheral	ISB1	63
	12	Peripheral	ISB2	64

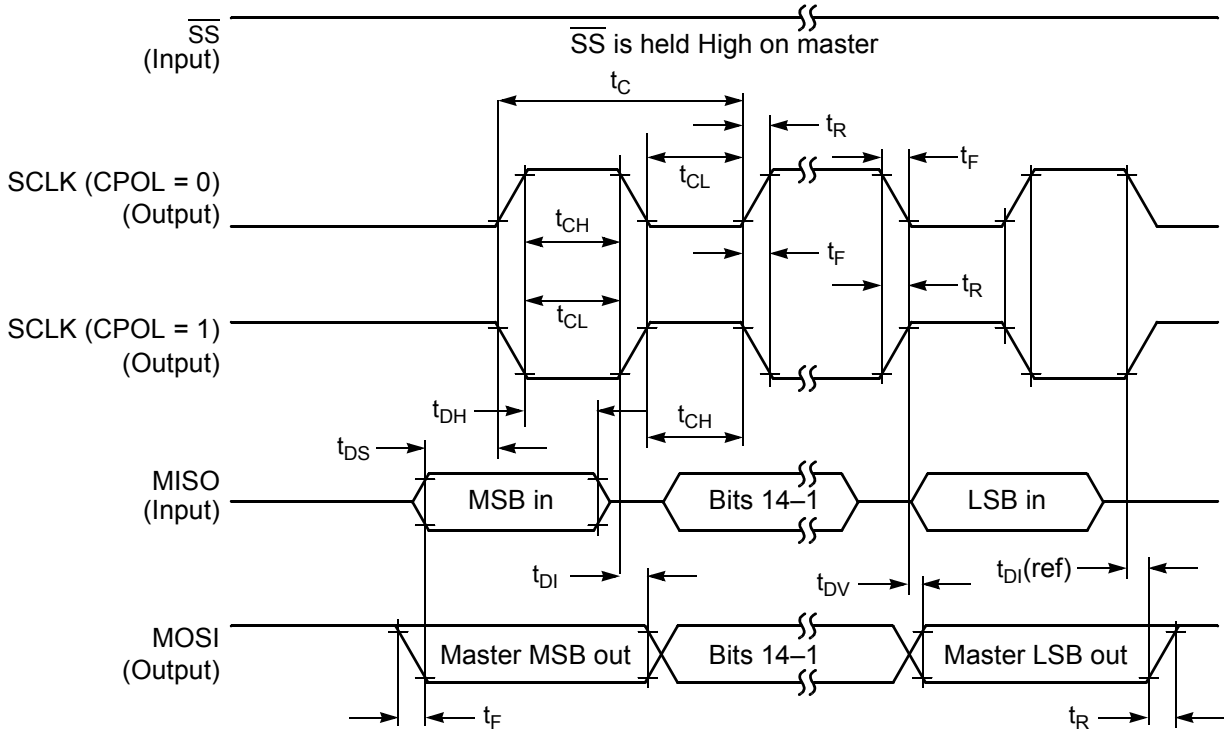


Figure 10-10 SPI Master Timing (CPHA = 0)

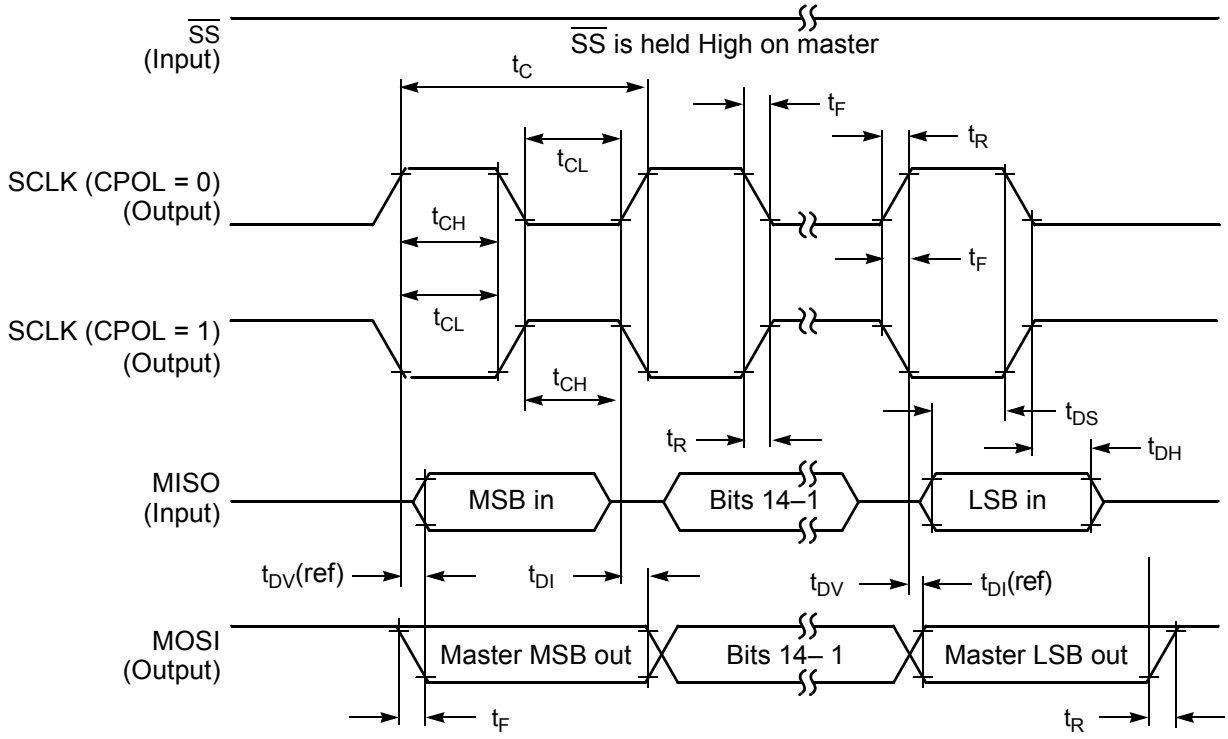


Figure 10-11 SPI Master Timing (CPHA = 1)

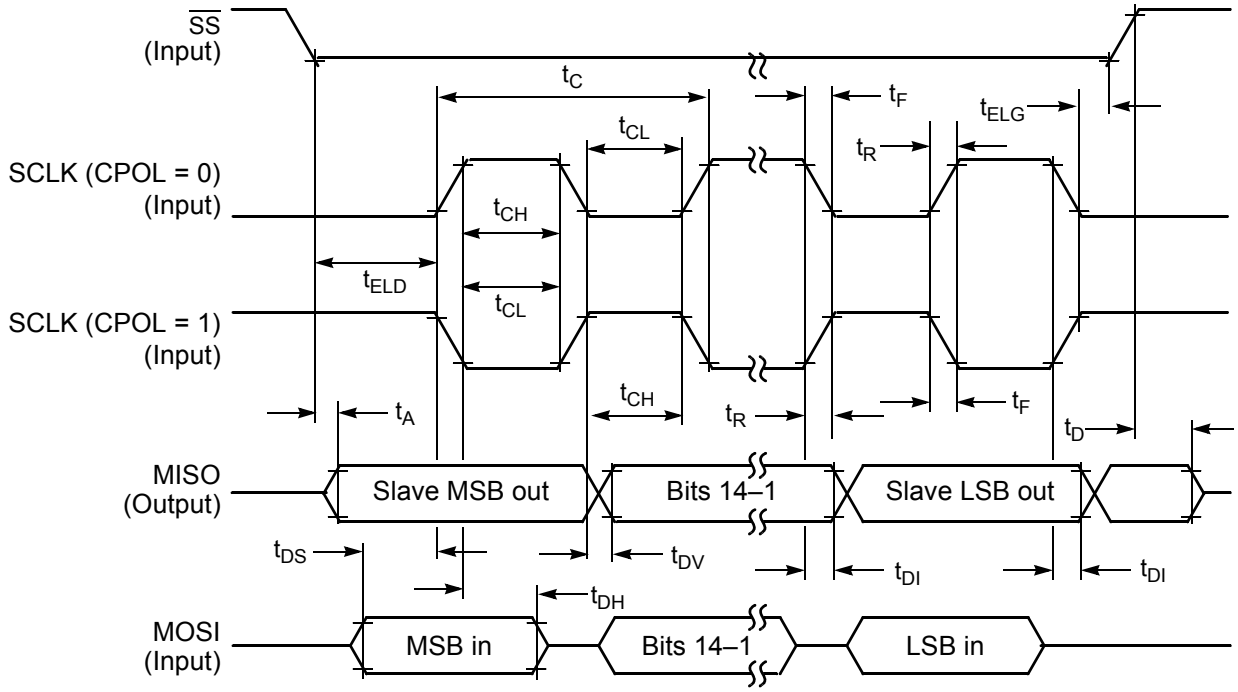


Figure 10-12 SPI Slave Timing (CPHA = 0)

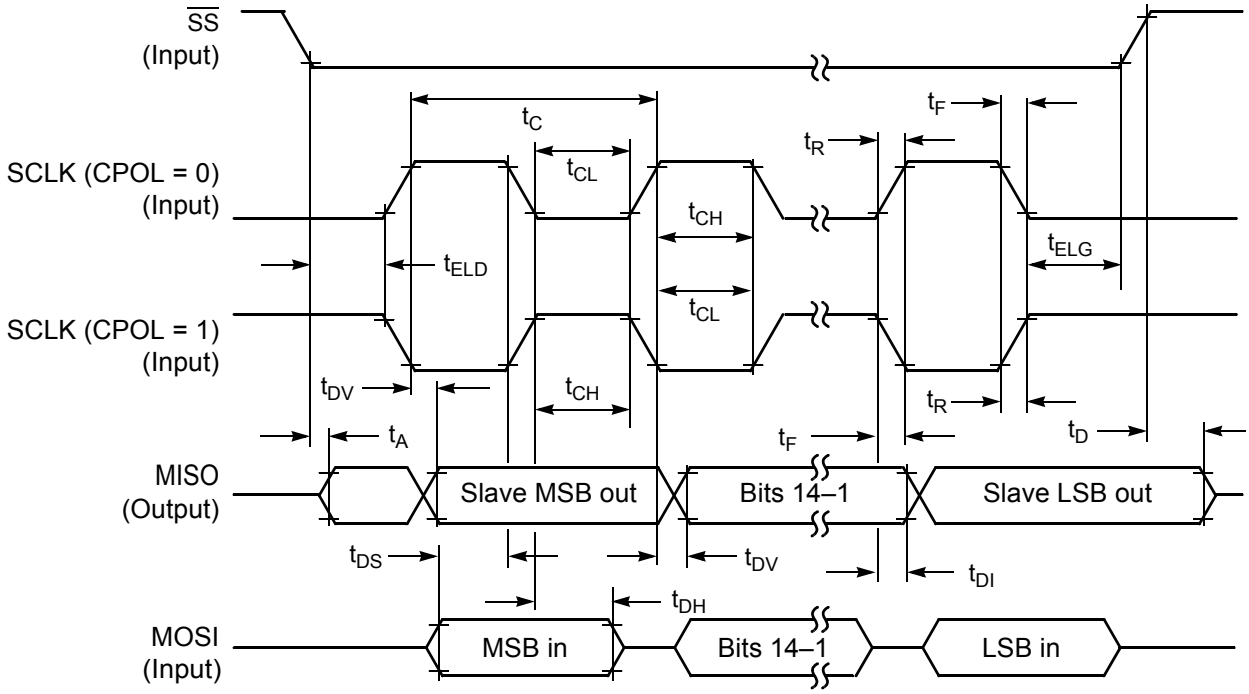


Figure 10-13 SPI Slave Timing (CPHA = 1)

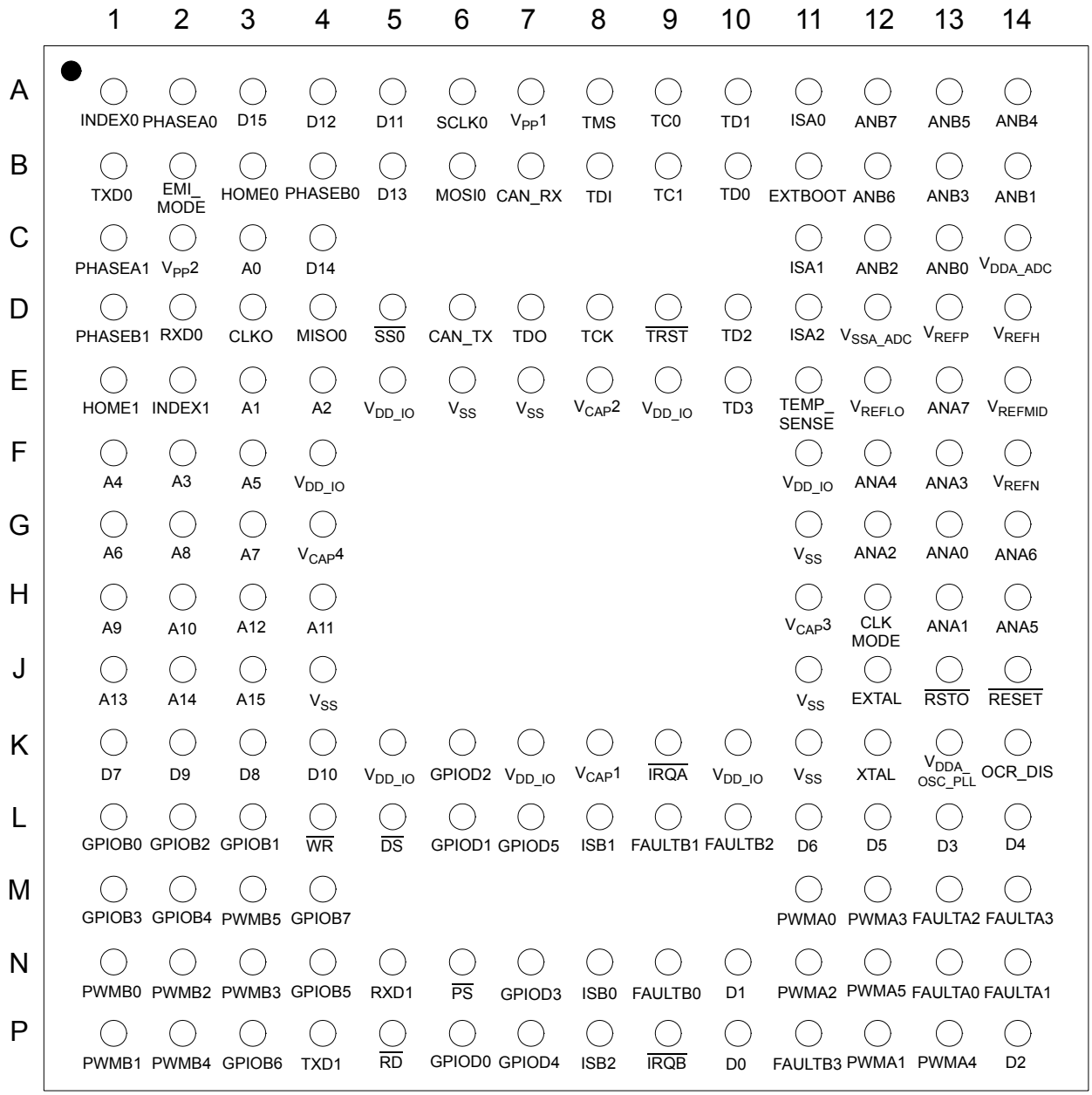
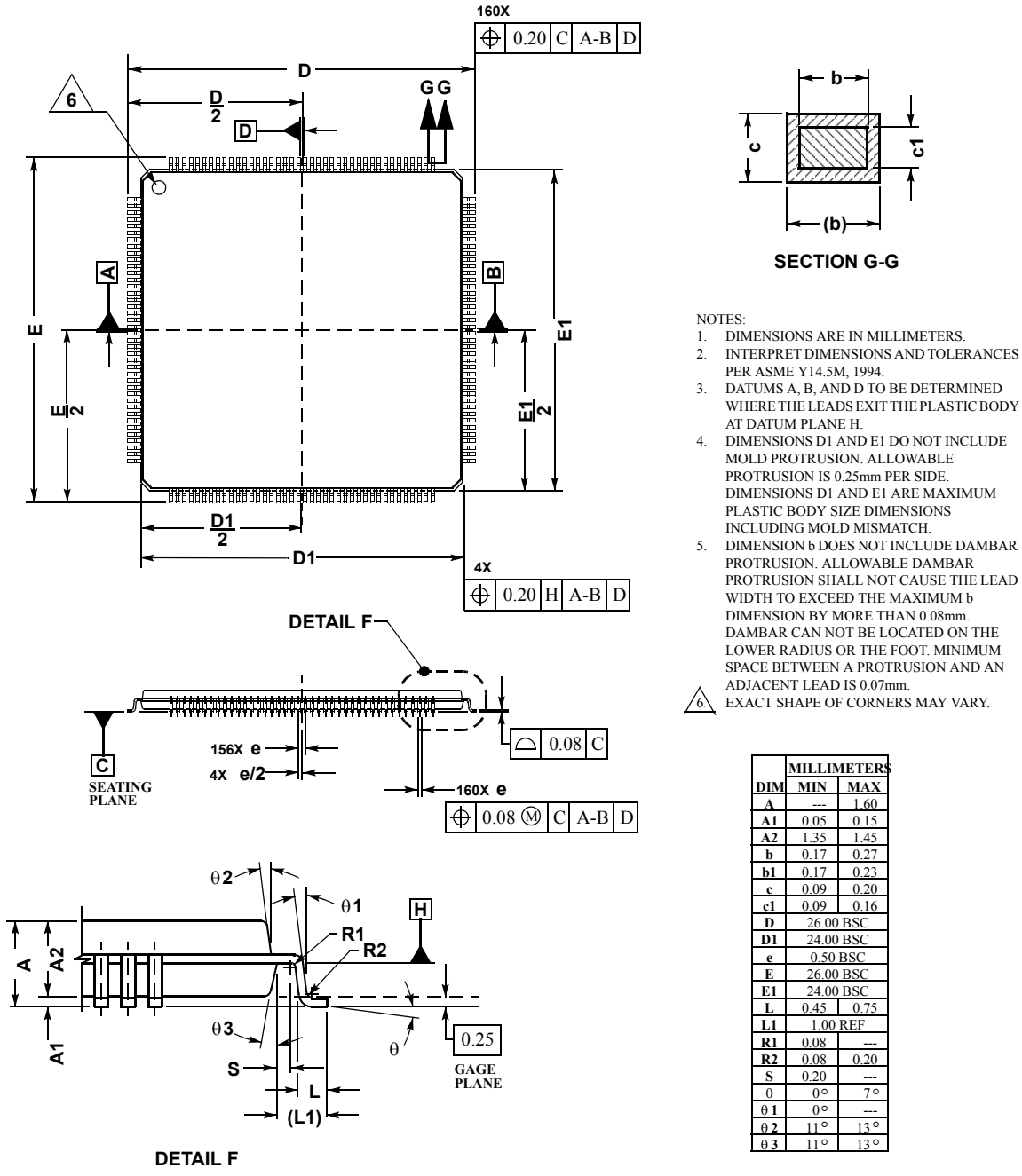


Figure 11-2 Top View, 56F8347 160-Pin MAPBGA Package



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	26.00 BSC	
D1	24.00 BSC	
e	0.50 BSC	
E	26.00 BSC	
E1	24.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	0.20
S	0.20	---
θ	0°	7°
θ1	0°	---
θ2	11°	13°
θ3	11°	13°

Figure 11-5 160-pin LQFP Mechanical Information

Please see http://www.freescale.com for the most current mechanical drawing.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct device operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor