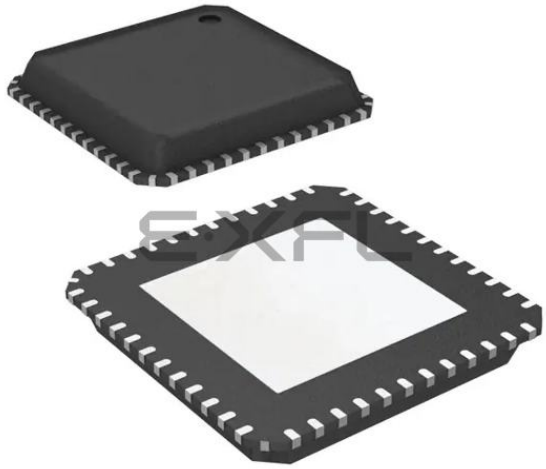

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	XC800
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	3.25K x 8
Interface	LIN, SSI, UART
Number of I/O	11
Voltage - Supply	3V ~ 27V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9835qx

1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9835QX device configuration.

Table 1 Device Configuration

Device Name	Max Clock Frequency	High Side Switches	High Voltage Monitor Inputs	Flash Size	Bidirectional Parallel Port I/O´s	Operational Amplifier
TLE9835QX	40 MHz	2	5	64 kByte	11	yes

Table 2 Acronyms

Acronyms	Name
ROM	Read Only Memory
SCK	SSC Clock
SFR	Special Function Register
SOW	Short Open Window (for WDT1)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
SSU	System Status Unit
TMS	Test Mode Select
UART	Universal Asynchronous Receiver Transmitter
UDIG	Universal Digital Controller for ADC1
VBG	Voltage reference Band Gap
WDT	Watchdog timer
WMU	Wake-up Management Unit
XRAM	On-Chip eXternal Data Memory
XSFR	On-Chip eXternal Special Function Register

3.1.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which serves as pad supply for the parallel port pins and other 5 V analog functions.

Features

- 5 V low-drop voltage regulator
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage overload monitoring with MCU signalling (Interrupt)
- Preregulator for VDDC regulator
- GPIO supply
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor C_{VDDP} is mandatory to ensure a proper regulator functionality.

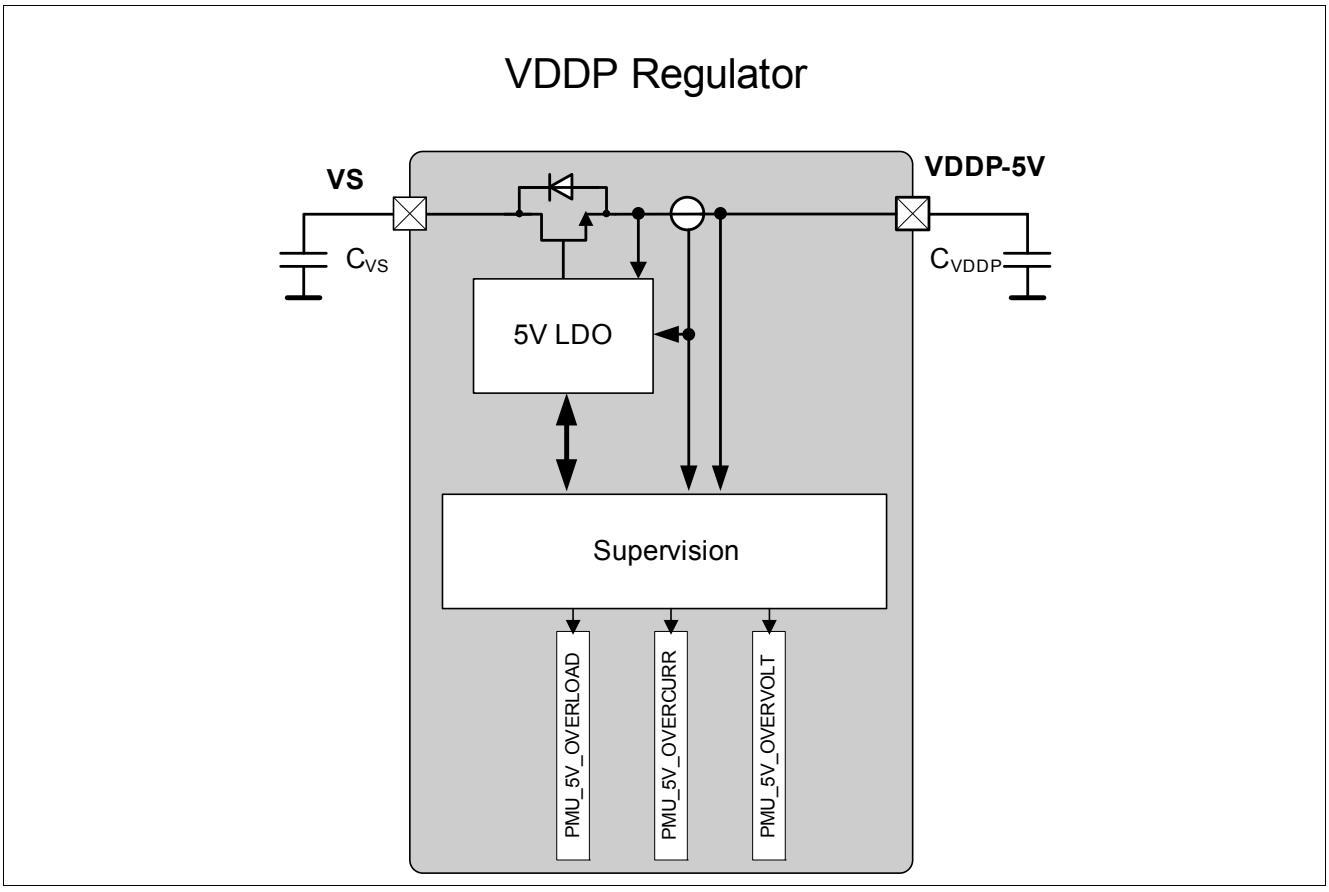

Figure 6 Module Block Diagram of VDDP Voltage Regulator

3.5 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 1.5V supply (VDDC) from the internal voltage regulator and does not require additional programming or erasing voltage.

Features

- In-System Programming via LIN (Flash mode) and DAP
- Error Correction Code (ECC) for dynamic correction of single Bit errors and signalling for double Bit failures
- Support for aborting erase operation
- Program width of 128 Byte (page)
- Minimum erase width of 128 Byte (page)
- 4 Byte read access
- Read access time: 75 ns
- Program time for 1 page: 3 ms
- Page erase time: 4 ms

3.6 Watchdog Timer 1 (WDT1)

Features

- Windowed Watchdog Timer with programmable timing in Active Mode
- Long open window (80ms) after power-up, reset, wake-up
- Short open window (30ms) to facilitate Flash programming
- Disabled during debugging
- Safety shutdown to Sleep Mode after 5 missed WDT1 services

There are two watchdog timers in the system. The Watchdog Timer (WDT) within the microcontroller (see **Chapter 3.7**) and the Watchdog Timer 1 (WDT1), which is described in this section.

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Stop Mode and OCDS mode the WDT1 is disabled.

The behavior of the Watchdog Timer 1 in Active Mode is depicted in **Figure 12**.

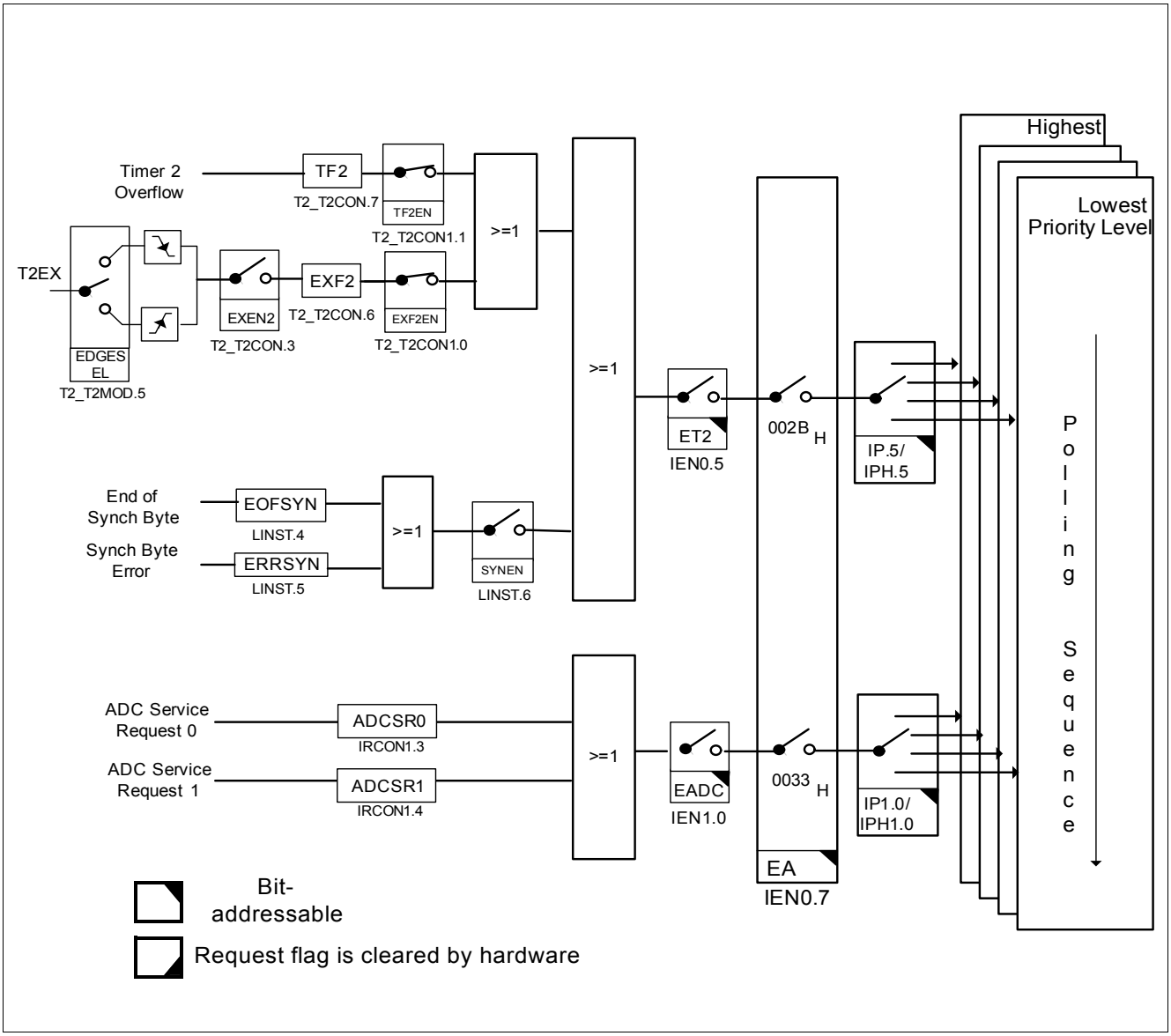

Figure 15 Interrupt Request Sources (Part 2)

3.13 Timer 3

Timer 3 can function as timer or counter. When functioning as a timer, Timer 3 is incremented in periods based on the system clock. When functioning as a counter, Timer 3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer 3 can be configured in four different operating modes to use in a variety of applications, see **Table 8**.

Table 8 Timer 3 Modes

Mode	Sub-Mode	Operation
0	**-**	**13-Bit Timer** The timer is essentially an 8-Bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**a**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter.
1	**b**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable a single shot measurement on a preset channel with the measurement unit.
1	**c**	**16-Bit Timer** The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable the LIN Baudrate Measurement.
2	**-**	**8-Bit Timer with Auto-reload** The timer register TLx is reloaded with a user-defined 8-Bit value in THx upon overflow.
3	**a**	**Timer 3 operates as Two 8-Bit Timers** The timer registers, TL3 and TH3, operate as two separate 8-Bit counters.
3	**b**	**Timer 3 operates as Two 8-Bit Timers** The timer registers, TL3 and TH3, operate as two separate 8-Bit counters. In this mode the 100 kHz Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as an counter which counts the time between the edges.

3.18 Measurement Unit

The measurement unit is a functional unit that comprises the following associated sub-modules:

- 1 x 8 Bit ADC (ADC2) with 10 inputs. 5 are for single ended input signals and 5 are for differential input signals.
- Monitoring inputs voltage attenuators with two selectable attenuation settings: divide by 4 and divide by 6
- Supply voltage attenuators with attenuation of VBAT_SENSE, VS, VDDP and VDDC.
- VBG monitoring of 8-Bit ADC (ADC2) to guarantee functional safety requirements.
- Low Side Switch current sensing of LS1 and LS2. Allows a scalable overcurrent pre warning.
- Temperature sensor for monitoring the chip temperature and Low Side Switches temperature.
- Supplement block with reference voltage generation, bias current generation, voltage buffer for Flash reference voltage, voltage buffer for analog module reference voltage and test interface.

Table 10 Measurement functions and associated modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-Bit ADC. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the Flash module
8-Bit ADC (ADC2)	8-Bit ADC module with 10 multiplexed inputs	1. 5 single-ended inputs 0 ... 1.23V 2. 5 differential inputs 0 ... 1.23V (allocation see following overview figure)
10-Bit ADC (ADC1)	10-Bit ADC module including analog test bus interface - part of µC subsystem	1. VBAT_SENSE measurement on channel 0 of ADC1. 2. VS measurement on channel 2 of ADC1. 3. MONx measurement on channel 6 of ADC1. 4. 5 additional (5V) analog inputs from Port 2.
Supply Voltage Attenuator	Resistive supply voltage attenuator	Scales down the supply voltages of the system to the input voltage range of ADC1 and ADC2.
Monitoring Input Attenuator	Resistive attenuator for (HV)	Scales down 5 monitoring input voltages to the input voltage range of the ADC1.
Central Temperature - Low Side Switch Temperature Sensor	Temperature sensor readout with two multiplexed ΔV_{be} sensing elements	Generates outputs voltage which is a linear function of the local chip (junction) temperature.
Measurement Core Module	Digital signal processing and ADC control unit	1. Generates the control signal for the 8-Bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

The structure of the measurement functions module is shown in **Figure 25**.

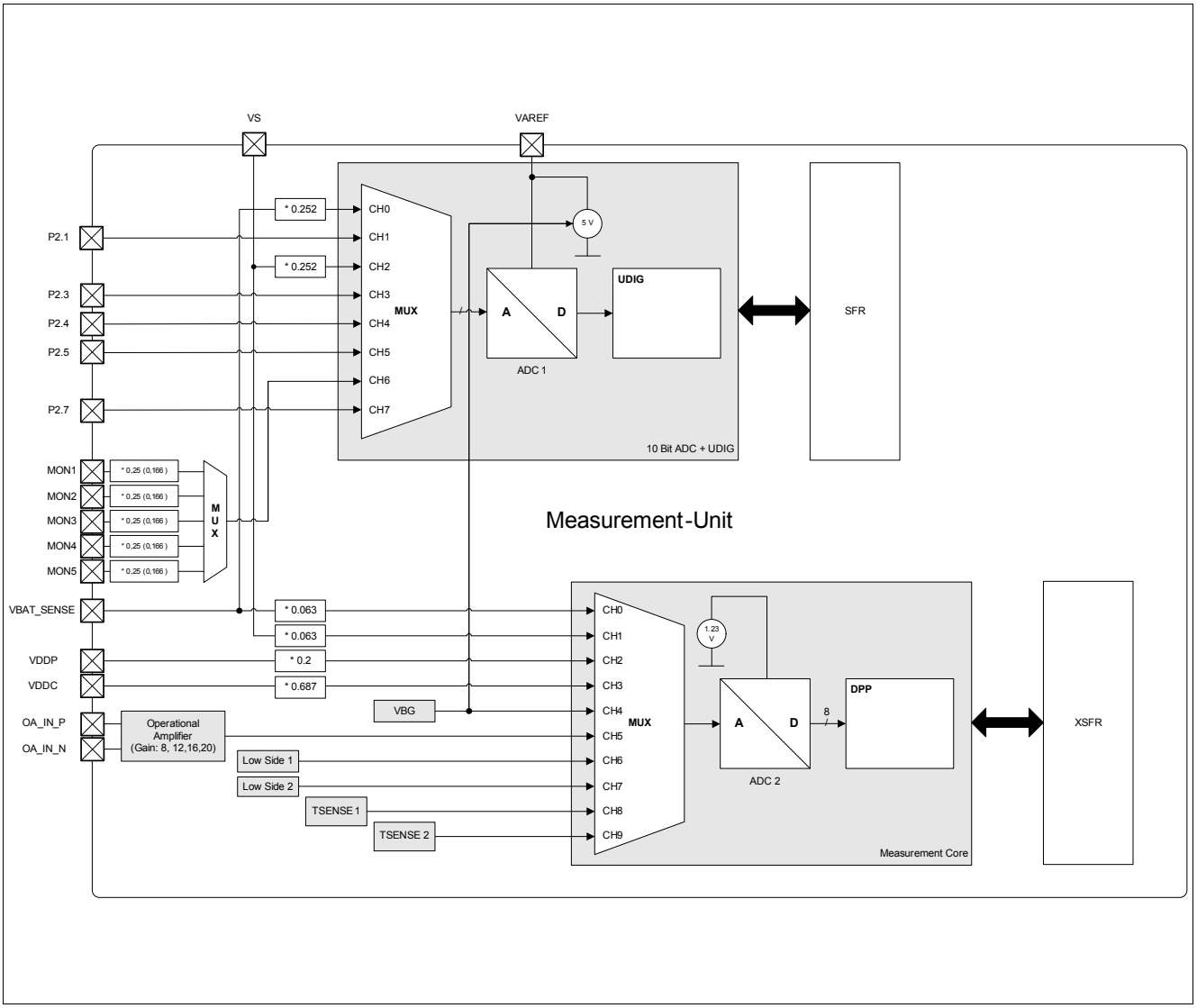

Figure 25 TLE9835QX Measurement Unit-Overview

3.21 High Voltage Monitor Input

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at each high-voltage MON_IN pin in low-power mode. Each input is sensitive to an input level monitoring. It is available when the module is switched to Active Mode via the MON_int (internal signal name) output with a small filter delay of typical 2 µs.

Features

- High-voltage input with V_S/2 threshold voltage
- Edge sensitive wake capability for power saving modes
- Level sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC1 in Active Mode, using adjustable threshold values (see also **Chapter 3.20**).

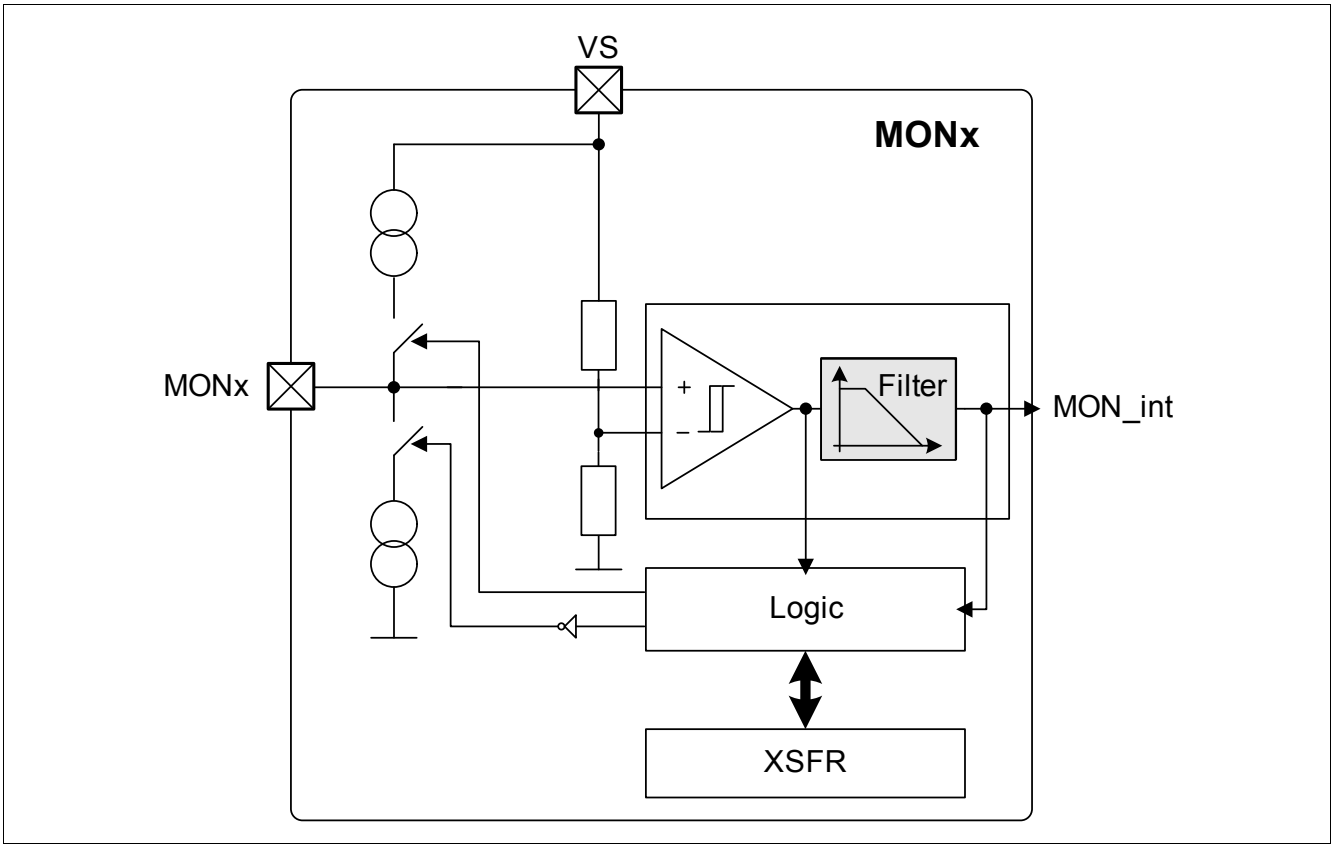

Figure 27 Monitoring Input Block Diagram

4 Application Information

4.1 Motor Drive with p/n-channel MOSFET Power Half Bridge

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

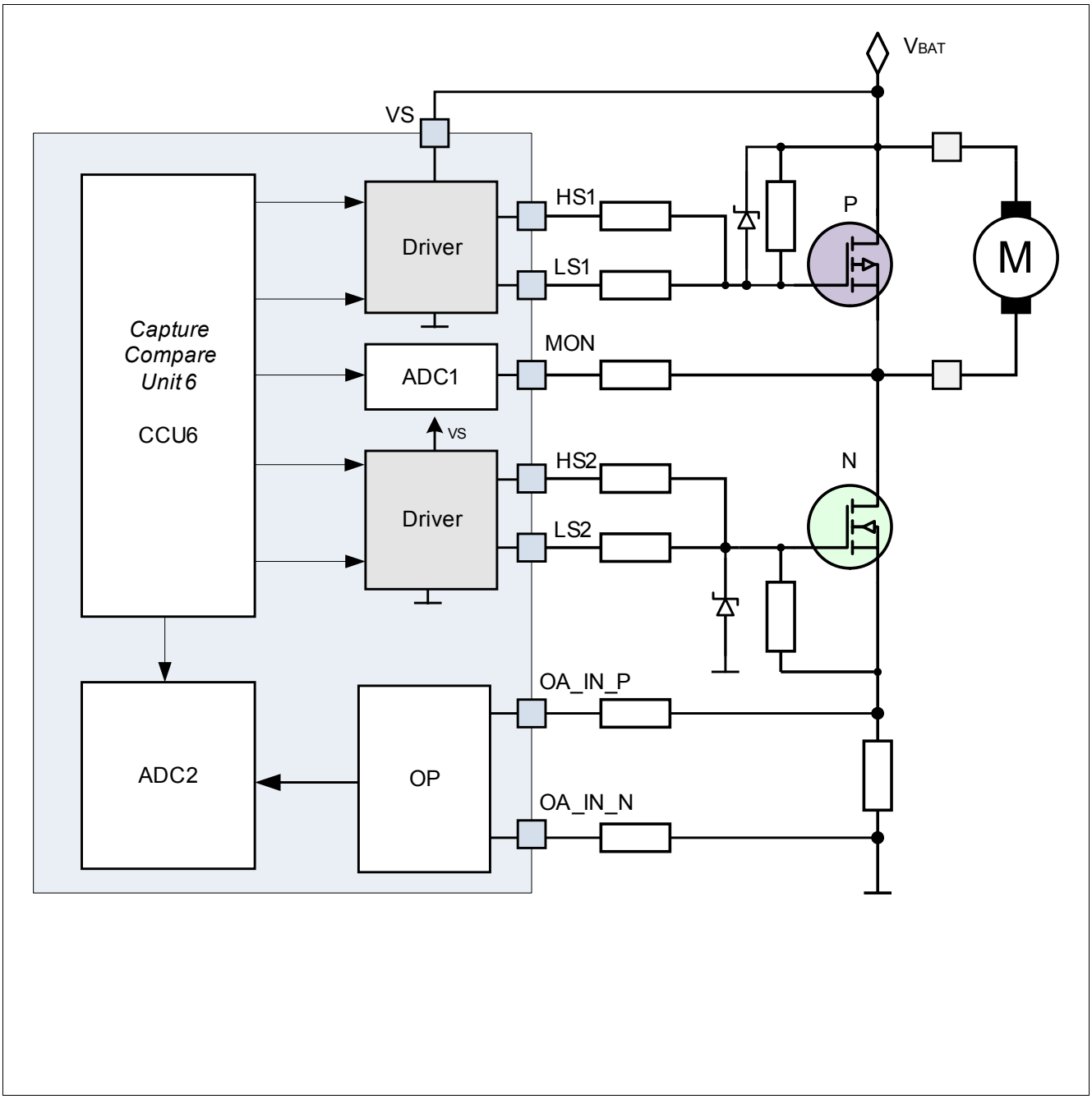

Figure 32 Scheme of relevant blocks used for single phase brush DC-motor control

4.1.1.3 MOSFET protection

For overload protection of the power MOSFET's two different options are provided by TLE9835QX:

- Current measurement by using the Operational Amplifier module[1].
- Output voltage measurement by using the Monitor Inputs

Assuming one terminal of the motor is connected to battery the protection against short circuit to battery of the power half bridge is possible by synchronous measurment of the active current over the shunt resistor. If the current exceeds the internally selected overcurrent threshold an interrupt will be generated which can be used to disable the respective gate driver stage of the n-channel MOSFET. Furthermore it is recommended to implement a software algorithm for detection of a motor stall condition based on the measured motor current. In case of a stall condition the power half bridge has to be disabled to avoid overheating of the MOSFET's. If a Hall sensor is available the signals of the sensor can be used in the software to detect a stall condition. .

4.1.2 Application hints

In **Figure 34** a simplified application diagram for brush-DC motor with terminal connected to battery is shown. Beside the above described functions it further includes an option to perform an output voltage monitoring using MON1 and LS2 in combination with R_{m2_v} and R_{m2_h} for pre-drive[2] output monitoring. The following diagnosis functions can be executed:

- Motor connection interrupted: LS2 activated => V_{M-}~0V instead of V_{Bat}
- Motor shorted to ground: LS2 off => V_{M-}~0V instead of V_{Bat}

To ensure stable supply voltage condition during PWM operation a buffer capacity C_1 in combination with C_0 is mandatory. Both capacitors need to be placed as close as possible to the power half bridge. C_1 should be dimensioned with respect to the PWM frequency as well as the allowed current and supply voltage ripple. To reduce the emission over the battery line a filter build up with an inductance L_1 and C_2 is required. The value of C_2 should be selected roughly in the region of 10% of the C_1 capacity. It is recommended to define the filter frequency of L_1 and C_2 to 50% of the PWM frequency. For reverse polarity protection a p-channel MOSFET provides a feasible solution.

1) This works only for shunt resistors to ground.

2) This means outputs HSx/LSx are switched off and will be enabled in a specific way for pre-drive check before starting normal operation.

5.2.3 VDDEXT Voltage Regulator 5.0V

Table 21 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Current	I_{VDDEXT}	0	–	20	mA	1)	P_5.2.20
Output Capacitance	C_{VDDEXT}	10	–	1000	nF	1) ESR < 1 Ω	P_5.2.21
Output Voltage including line regulation	V_{DDEXT}	4.9	5.0	5.1	V	I_{load} < 20mA;Vs > 5.5V	P_5.2.22
Output Drop	V_s-V_{DDEXT}		–	+400	mV	1) I_{load} < 20mA; 3V < V_s < 5.5V	P_5.2.23
Dynamic Load Regulation	$V_{DDEXTLOR}$	-50	–	50	mV	1) 2 ... 20mA; C=10nF; dI/dt=10mA/µs	P_5.2.24
Dynamic Line Regulation	$V_{VDDEXTLIR}$	-25	–	25	mV	V_s= 5.5 ... 20V; dV/dt=5V/µs	P_5.2.25
Power Supply Ripple Rejection1)	$P_{SSRVDDEXT}$	50	–	–	dB	V_s= 13.5V; f=0 ... 1KHz; V_r=2Vpp	P_5.2.26
Over Voltage Detection	$V_{VDDEXTOV}$	5.05	–	5.4	V	V_s > 5.5V	P_5.2.27
Under Voltage Detection	$V_{VDDEXTUV}$	2.6	–	2.9	V	2)V_s > 3.0V	P_5.2.28
Over Current Diagnostic	$I_{VDDEXTOC}$	25	–	70	mA	–	P_5.2.29

1) Not subject to production test, specified by design

2) When the condition is met, the Bit VDDEXT_CTRL.VDDEXT_SHORT will be set

5.3 System Clocks

5.3.1 Oscillators and PLL

Table 22 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK1}	14	18	22	MHz	this clock is used at startup and can be used in case the PLL fails	P_5.3.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	this clock is used for cyclic wake and cyclic sense	P_5.3.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Oscillator frequency	f_{INTOSC}		5		MHz		P_5.3.42
Short term frequency deviation	f_{TRIMST}	-0.5%		+0.5%		[1] for duration < 5ms	P_5.3.43
Short term frequency deviation	f_{TRIMST}	-1.5%		+1.5%		[1] for duration >=5ms and <100ms	P_5.3.3
Long term frequency deviation	f_{TRIMLT}	-3.0%		+3.0%		[2]over lifetime and temperature	P_5.3.4
CGU-OSC Start-up time	T_{OSC}	–	–	10	µs	startup time OSC from Sleep Mode and Stop Mode, power supply stable	P_5.3.5
PLL (Clock Generation Unit Microcontroller)							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_5.3.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_5.3.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_5.3.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_5.3.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_5.3.10
Free-running frequency Mode 0	$f_{VCOfree\_0}$	–	–	38	MHz	VCOSEL =”0”	P_5.3.11
Free-running frequency Mode 1	$f_{VCOfree\_1}$	–	–	76	MHz	VCOSEL =”1”	P_5.3.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_5.3.13
Peak period jitter	t_{jp}	-500	–	500	ps	for K=1	P_5.3.14

Table 22 Electrical Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Accumulated jitter	jacc	–	–	5	ns	for K=1	P_5.3.15
lock-in time	T_L	–	–	200	µs	–	P_5.3.16

1) V_{DDC} = 1.5 V, T_j = 25°C

2) including short term frequency deviation

5.3.2 External Clock Parameters XTAL1, XTAL2

Table 23 Functional Range

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range limits for signal on XTAL1	V_{IX1_SR}	-1.7 + V_{DDC}	–	1.7	V	1)	P_5.3.17
Input voltage (amplitude) on XTAL1	V_{AX1_SR}	0.3 x V_{DDP}	–	–	V	2) Peak-to-peak voltage	P_5.3.18
XTAL1 input current	I_{IL}	–	–	±20	µA	0 V < V_{IN} < V_{DDC}	P_5.3.19
Oscillator frequency	f_{OSC}	4	–	24	MHz	Clock signal	P_5.3.20
Oscillator frequency	f_{OSC}	4	–	16	MHz	Crystal or Resonator	P_5.3.21
High time	t_1	6	–	–	ns	–	P_5.3.22
Low time	t_2	6	–	–	ns	–	P_5.3.23
Rise time	t_3	–	8	8	ns	–	P_5.3.24
Fall time	t_4	–	8	8	ns	–	P_5.3.25

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

5.4 Flash Parameters

This chapter includes the parameters for the 64 kByte embedded flash module.

Table 24 Flash Characteristics [1)]

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 Byte page	t_{PR}	–	[2)]3	3.5	ms	–	P_5.4.1
Erase time per sector/page	t_{ER}	–	[2)]4	4.5	ms	–	P_5.4.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_5.4.3
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_5.4.4

1) Not subject for production test, specified by design

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.

5.5 Parallel Ports (GPIO)

5.5.1 Functional Range

Table 25 Functional Range

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output current on any pin	I_{OH} , I_{OL}	–	–	20	mA	1) 2)	P_5.5.1
Max output current for all GPIOs	I_{max}	–	–	60	mA	1) 2)	P_5.5.2

1) One of these limits must be kept.

2) Not subject to production test, specified by design

5.5.2 DC Parameters

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 26 DC Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage (all except XTAL1)	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	–	P_5.5.3
Input high voltage (all except XTAL1)	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	–	P_5.5.4
Input Hysteresis[1)]	HYS	0.11 x V_{DDP}	–	–	V	Series resistance = 0 Ω	P_5.5.5
Output low voltage	V_{OL}	–	–	1.0	V	2) $I_{OL} \le I_{OLmax}$	P_5.5.6
Output low voltage	V_{OL}	–	–	0.4	V	2) $I_{OL} \le$ 3) I_{OLnom}	P_5.5.7
Output high voltage[4)]	V_{OH}	V_{DDP} - 1.0	–	–	V	2) $I_{OH} \ge I_{OHmax}$	P_5.5.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	2)3) $I_{OH} \ge I_{OHnom}$	P_5.5.9
Input leakage current (Port 2)	I_{OZ1}	-400	–	+400	nA	$T_J \le 85°C$, 0 V < V_{IN} < V_{DDP}	P_5.5.10
Input leakage current (all other)[5)]	I_{OZ2}	-5	–	+5	µA	$T_J \le 85°C$, 0.45 V < V_{IN} < V_{DDP}	P_5.5.11

Table 28 Electrical Characteristics (cont'd) **LIN Transceiver**

V_s = 5.5V - 18V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	0.5	6	µs	–	P_5.6.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.0	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_5.6.33
Duty cycle D7 (for worst case at 115 kBit/s) for +1 µs Receiver delay symmetry	t_{duty1}	0.399	–	–		8) duty cycle D7 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus\_rec(min)}$/2 t_{bit};	P_5.6.34
Duty cycle D8 (for worst case at 115 kBit/s) for +1 µs Receiver delay symmetry	t_{duty2}	–	–	0.578		6) duty cycle 8 TH_{Rec}(max) = 0.422 × V_S; TH_{Dom}(max) = 0.284 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus\_rec(max)}$/2 t_{bit};	P_5.6.35
TxD dominant time out	$t_{timeout}$	6	12	20	ms	8) V_{TxD} = 0 V	P_5.6.36

1) Maximum limit specified by design.
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) This parameter is not subject to production test
5) Bus load concerning LIN Spec 2.1:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Bus loads:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
7) Bus load concerning LIN Spec 2.1:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
8) Timeout can be disabled optional

5.9.2 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 36 A/D Converter Characteristics

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREFSR}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_5.9.7
Analog reference ground	V_{AGNDSR}	GND - 0.05	–	1.5	V	2)	P_5.9.8
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	3)	P_5.9.9
Analog clock frequency	f_{ADCI}	0.5	–	20	MHz	4)	P_5.9.10
Conversion time for 10-bit result[5)]	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	6)	P_5.9.11
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	6)	P_5.9.12
Wake-up time from analog Stop Mode, fast mode	t_{WAF}	–	–	4	µs	7)	P_5.9.13
Wake-up time from analog Stop Mode, slow mode	t_{WAS}	–	–	15	µs	7)	P_5.9.14
Total unadjusted error[8)]	TUE	-15	–	+ 15	LSB	1) V_{AREF} = 5.0 V±1%	P_5.9.15
DNL error	EA_{DNL}EA	-2	–	+ 2	LSB	–	P_5.9.16
INL error	EA_{INL}EA	-5	–	+ 5	LSB	–	P_5.9.17
Gain error	EA_{GAIN}EA	-10	–	+ 10	LSB	–	P_5.9.18
Offset error	EA_{OFF}EA	-2	–	+ 2	LSB	–	P_5.9.19
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	7)9)	P_5.9.20
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	7)9)	P_5.9.21
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	7)9)	P_5.9.22
Total capacitance of the reference input	C_{AREFT}	–	–	15	pF	7)9)	P_5.9.23
Switched capacitance of the reference input	C_{AREFS}	–	–	7	pF	7)9)	P_5.9.24
Resistance of the reference input path	R_{AREF}	–	–	2	kΩ	7)9)	P_5.9.25

Table 41 Electrical Characteristics (cont'd)

V_S = 5.5 V to 27 V, T_j = -40° C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn OFF Delay time, PWM mode	$t_{dOff,f\text{-}LS}$	–	–	2	µs	LS_ON=0 to 0.1*Vs V_S=13.5V, R_L =270Ω	P_5.12.12
Turn OFF Rise time, PWM mode	$t_{OFFR,PWM}$	–	1	1.25	µs	V_{LS} 0.1*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_5.12.13
Turn OFF Rise time, slow mode	$t_{OFFR,Slow}$	–	100	150	µs	1) V_{LS} 0.9*Vs to 0.9*Vs; V_S=13.5V, R_L =270Ω	P_5.12.14
Minimum Duty Cycle Pulse Width variation	ton_{MIN}	1.5	2	3.5	µs	ton(dig) = 2µs2)	P_5.12.15
Typical (systematic) Pulse Width increase LS_ON to VLS	$d\ ton_{TYP}$	–	1.25	–	µs	ton(dig) = 2µs2)	P_5.12.16
Zener Clamp Voltage	V_{AZ}	–	50	–	V	values are valid at T_j = 25°C	P_5.12.17
Clamping Energy (repetitive)	E_{clamp}	–	–	2	mJ	2) 1.000.000 cycles	P_5.12.18
Clamping Energy	E_{clamp}	–	–	14	mJ	2) Tstart = 25°C	P_5.12.19
Clamping Energy (single), hot	E_{clamp}	–	–	7	mJ	2) 10 cycles, Tstart = 85°C	P_5.12.20

1) Static ON mode (no PWM)

2) Not subject to production test, specified by design

7 Revision History

Revision	Date	Changes
1.0	2012-06-27	Initial revision