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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e217afg

6.3 Auxiliary SRAM

W79E217 has a 2 KB of data space SRAM which is read/write accessible and is memory mapped. This on-chip SRAM is accessed by the MOVX instruction. There is no conflict or overlap among the 256 bytes scratch-pad memory and the 2 KB auxiliary sram as they use different addressing modes and instructions. Access to the on-chip Data Memory is optional under software control. Set DMEO bit of PMR SFR to 1 will enable the on-chip 2 KB MOVX SRAM and at the same time EnNVM bit must be cleared as NVM memory uses the same instruction of MOVX. Refer to Table 6-3: W79E217 NVM page (n) area definition table.

6.4 2-KB NVM Data Flash Memory

W79E217 2-KB NVM memory block shown in the diagram on Figure 6-1, shares the same address as AUX-RAM address.

Due to overlapping of AUX-RAM, NVM data memory and external data memory physical address, the following table is defined. EnNVM bit (NVMCON.5) will enable read access to NVM data memory area. DME0 (PMR.0) will enable read access to AUX-RAM.

ENNVM	DME0	DATA MEMORY AREA
0	0	Enable External RAM read/write access by MOVX
0	1	Enable AUX-RAM read/write access by MOVX
1	X	Enable NVM data Memory read access by MOVX only. If EER or EWR is set and NVM flash erase or write control is busy, to set this bit read NVM data is invalid.

Table 6-1: Bits setting for MOVX access to Data Memory Area

INSTRUCTIONS		ENNVM = 1	
		NVM SIZE = SRAM (2K)	
		ADDR ≤ 2K	ADDR > 2K
Read access	MOVX A, @DPTR (Read)	NVM	Ext memory
	MOVX A, @R0 (Read)	NVM	NOP
	MOVX A, @R1 (Read)	NVM	NOP
Write access	MOVX @DPTR, A (Write)	NOP	Ext memory
	MOVX @R0, A (Write)	NOP	NOP
	MOVX @R1, A (Write)	NOP	NOP

Table 6-2: MOVX read/write access destination

7. SPECIAL FUNCTION REGISTERS

The W79E217 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E217 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses.

F8	EIP	EIE1	EIP1	CCL0 /PCNTL	CCH0 /PCNTH	CCL1 /PLSCNTL	CCH1 /PLSCNTH	INTCTRL
F0	B			SPCR	SPSR	SPDR	I2CSADEN	EIPH
E8	EIE	I2CON	I2ADDR	NVMADD RH	I2DAT	I2STATUS	I2CLK	I2TIMER
E0	ACC	ADCCON	ADCH	ADCL	LCDCN	PDTC1	PDTC0	PWMCON4
D8	WDCON	PWMPL	PWM0L	NVMADDR L	PWMCON1	PWM2L	PWM6L	PWMCON3
D0	PSW	PWMPH	PWM0H	NVMDAT	QEICON	PWM2H	PWM6H	WDCON2
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4L
C0	SCON1	SBUF1	T3MOD	T3CON	PMR	FSPLT	ADCPS	TA
B8	IP	SADEN	SADEN1	POVM	POVD	PIO	PWMEN	PWM4H
B0	P3	P5	P6	P7	RCAP3L	RCAP3H	EIP1H	IPH
A8	IE	SADDR	SADDR1	LCDPT	SFRAL	SFRAH	SFRFD	SFRCN
A0	P2	XRAMAH	P4CSIN	CAPCON0	CAPCON1	P4	CCL2 /MAXCNTL	CCH2 /MAXCNTH
98	SCON	SBUF	P42AL	P42AH	P43AL	P43AH	NVMCON	CHPCON
90	P1	EXIF	P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CKCON1
80	P0	SP	DPL	DPH	TL3	TH3	LCDDATA	PCON

Table 7-1: Special Function Register Location Table

SYMBOL	DEFINITION	ADDRESS	MSB LSB				BIT_ADDRESS,			SYMBOL	RESET
INTCTRL	INTERRUPT CONTROL REGISTER	FFH	-	-	INT5CT1	INT5CT0	INT4CT1	INT4CT0	INT3CT1	INT3CT0	xx00 0000B
CCH1 /PLSCNTH	CAPTURE COUNTER HIGH 1 REGISTER	FEH	CCH1.7 /PLSCNTH.7	CCH1.6 /PLSCNTH.6	CCH1.5 /PLSCNTH.5	CCH1.4 /PLSCNTH.4	CCH1.3 /PLSCNTH.3	CCH1.2 /PLSCNTH.2	CCH1.1 /PLSCNTH.1	CCH1.0 /PLSCNTH.0	0000 0000B
CCL1 /PLSCNTL	CAPTURE COUNTER LOW 1 REGISTER	FDH	CCL1.7 /PLSCNTL.7	CCL1.6 /PLSCNTL.6	CCL1.5 /PLSCNTL.5	CCL1.4 /PLSCNTL.4	CCL1.3 /PLSCNTL.3	CCL1.2 /PLSCNTL.2	CCL1.1 /PLSCNTL.1	CCL1.0 /PLSCNTL.0	0000 0000B
CCH0 /PCNTH	CAPTURE COUNTER HIGH 0 REGISTER	FCH	CCH0.7 /PCNTH.7	CCH0.6 /PCNTH.6	CCH0.5 /PCNTH.5	CCH0.4 /PCNTH.4	CCH0.3 /PCNTH.3	CCH0.2 /PCNTH.2	CCH0.1 /PCNTH.1	CCH0.0 /PCNTH.0	0000 0000B
CCL0 /PCNTL	CAPTURE COUNTER LOW 0 REGISTER	FBH	CCL0.7 /PCNTL.7	CCL0.6 /PCNTL.6	CCL0.5 /PCNTL.5	CCL0.4 /PCNTL.4	CCL0.3 /PCNTL.3	CCL0.2 /PCNTL.2	CCL0.1 /PCNTL.1	CCL0.0 /PCNTL.0	0000 0000B
EIP1	EXTENDED INTERRUPT PRIORITY 1	FAH	-	-	PNVMI	PCPTF	PT3	PBKF	PPWMF	PSPI	xx00 0000B
EIE1	INTERRUPT ENABLE 1	F9H	-	-	ENVM	ECPTF	ET3	EBK	EPWM	ESPI	xx00 0000B
EIP	EXTENDED INTERRUPT PRIORITY	F8H	(FF) PS1	(FE) PX5	(FD) PX4	(FC) PWDI	(FB) PX3	(FA) PX2	(F9) -	(F8) PI2C	0000 00x0B
EIPH	EXTENDED INTERRUPT HIGH PRIORITY	F7H	PS1H	PX5H	PX4H	PWDIH	PX3H	PX2H	-	PI2CH	0000 00x0B
I2CSADEN	I2C SLAVE ADDRESS MASK	F6H	I2CSADEN.7	I2CSADEN.6	I2CSADEN.5	I2CSADEN.4	I2CSADEN.3	I2CSADEN.2	I2CSADEN.1	I2CSADEN.0	1111 1110B
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0	xxxx xxxxB
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-	0000 0xxxB
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100B
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
I2TIMER	I2C TIMER COUNTER REGISTER	EFH	-	-	-	-	-	ENTI	DIV4	TIF	xxxx x000B
I2CLK	I2C CLOCK RATE	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C STATUS REGISTER	EDH									1111 1000B
I2DAT	I2C DATA	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	0000 0000B
NVMADDRH	NVM HIGH BYTE ADDRESS	EBH	-	-	-	-	-	NVMADDRH.10	NVMADDRH.9	NVMADDRH.8	xxxx x000B
I2ADDR	I2C SLAVE ADDRESS	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	0000 0000B
I2CON	I2C CONTROL REGISTER	E9H	-	ENS	STA	STO	SI	AA	I2CIN	-	X000 000xB
EIE	EXTENDED INTERRUPT ENABLE	E8H	(EF) ES1	(EE) EX5	(ED) EX4	(EC) EWDI	(EB) EX3	(EA) EX2	(E9)	(E8) EI2C	0000 00x0B
PWMCON4	PWM CONTROL REGISTER 4	E7H	PWMEOM	PWMOOM	PWM6OM	PWM7OM	-	-	-	BKF	0000 xxx0B
PDTC0	DEAD TIME CONTROL REGISTER 0	E6H	PDTC0.7	PDTC0.6	PDTC0.5	PDTC0.4	PDTC0.3	PDTC0.2	PDTC0.1	PDTC0.0	0000 0000B
PDTC1	DEAD TIME CONTROL REGISTER 1	E5H	PDTC1.7	PDTC1.6	PDTC1.5	PDTC1.4	PDTC1.3	PDTC1.2	PDTC1.1	PDTC1.0	0000 0000B
LCDCN	LCD CONTROL REGISTER	E4H	LCDEN	Clear	Duty	Pump	-	FS2	FS1	FS0	0000 x000B
ADCL	ADC CONVERTER RESULT LOW BYTE	E3H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxB

		serial port 1 to which the slave processor is designated.

LCD POINTER REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	LCDPT.3	LCDPT.2	LCDPT.1	LCDPT.0

Mnemonic: LCDPT Address: ABh

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-0	LCDPT	Address pointer between 0h~Fh.

ISP ADDRESS LOW BYTE

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: SFRAL Address: ACh

Low byte destination address for In System Programming operations.

ISP ADDRESS HIGH BYTE

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: SFRAH Address: ADh

Low byte destination address for In System Programming operations. (SFRAH, SFRAL) represents the address of the ROM byte that will be erased, programmed or read.

ISP DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Mnemonic: SFRFD Address: AEh

In ISP mode, read/write a specific byte ROM content must go through SFRFD register.

ISP OPERATION MODES

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: AFh

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7-0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial port data. When SADEN.n is 0, then the bit becomes don't care in the comparison. This register enables the Automatic Address Recognition feature of the Serial port. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

SLAVE ADDRESS MASK ENABLE 1

Bit:	7	6	5	4	3	2	1	0
	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0

Mnemonic: SADEN1 Address: BAh

BIT	NAME	FUNCTION
7-0	SADEN1	This register enables the Automatic Address Recognition feature of the Serial port 1. When a bit in the SADEN1 is set to 1, the same bit location in SADDR1 will be compared with the incoming serial port data. When SADEN1.n is 0, then the bit becomes don't care in the comparison. This register enables the Automatic Address Recognition feature of the Serial port. When all the bits of SADEN1 are 0, interrupt will occur for any incoming address.

PWM OUTPUT OVERRIDE CONTROL REGISTERS

Bit:	7	6	5	4	3	2	1	0
	POVM.7	POVM.6	POVM.5	POVM.4	POVM.3	POVM.2	POVM.1	POVM.0

Mnemonic: POVM Address: BBh

BIT	NAME	FUNCTION
7-0	POVM	PWM Override Mode enable bits; 0: The PWM output follows the corresponding PWM generator. 1: The PWM output is equal to corresponding bit in POVD.

PWM OUTPUT STATE REGISTERS

Bit:	7	6	5	4	3	2	1	0
	POVD.7	POVD.6	POVD.5	POVD.4	POVD.3	POVD.2	POVD.1	POVD.0

Mnemonic: POVD Address: BCh

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7-6</td><td>PDTC1</td><td>Dead-time clock frequency (FDT) prescaler select bits.
<table><tr><td>PDTC1.7</td><td>PDTC1.6</td><td>FDT</td></tr><tr><td>0</td><td>0</td><td>FOSC/2</td></tr><tr><td>0</td><td>1</td><td>FOSC/4</td></tr><tr><td>1</td><td>0</td><td>FOSC/8</td></tr><tr><td>1</td><td>1</td><td>FOSC/16</td></tr></table></td></tr>
<tr><td>5-0</td><td>PDTC1</td><td>Dead time counter. Unsigned 6 bit dead time value bits for Dead Time Unit.
Dead-time = FDT * (PDTC1 [5:0]+1)</td></tr>
</table>

PWM DEAD-TIME CONTROL REGISTER 0

Bit:	7	6	5	4	3	2	1	0
	PDTC0.7	PDTC0.6	PDTC0.5	PDTC0.4	PDTC0.3	PDTC0.2	PDTC0.1	PDTC0.0

Mnemonic: PDTC0 Address: E6h

BIT	NAME	FUNCTION
7-4	PDTC0	Control complementary PWM to delay a dead-time at every rising edge or falling edge. Reset value = 0. 1 = Dead-time is inserted at falling edge. 0 = Dead-time is inserted at rising edge. PDTC0.4 - controls the pair of (PWM0, PWM1). PDTC0.5 - controls the pair of (PWM2, PWM3). PDTC0.6 - controls the pair of (PWM4, PWM5). PDTC0.7 - controls the pair of (PWM6, PWM7).
3-0	PDTC0	Enable dead-time insertion; Dead-time insertion is only active when the pair of complementary PWM is enabled. Reset value=0. If dead-time insertion is inactive, the outputs of pin pair are complementary without any delay. 1 = Programmable dead-time is inserted into the pair signals of comparator output to delay the pair signals change from low to high. 0 = Disable dead-time insertion. PDTC0.0 - enables the dead-time insertion on the pin pair (PWM0, PWM1). PDTC0.1 - enables the dead-time insertion on the pin pair (PWM2, PWM3). PDTC0.2 - enables the dead-time insertion on the pin pair (PWM4, PWM5). PDTC0.3 - enables the dead-time insertion on the pin pair (PWM6, PWM7).

PWM CONTROL REGISTER 4

Bit:	7	6	5	4	3	2	1	0
	PWMEOM	PWMOOM	PWM6OM	PWM7OM	-	-	-	BKF

Mnemonic: PWMCON4 Address: E7h

Continued

OP-CODE	HEX CODE	BYTES	W79E217 MACHINE CYCLE	W79E217 CLOCK CYCLES	8032 CLOCK CYCLES	W79E217 VS. 8032 SPEED RATIO
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3	PORT4	PORT5	PORT6	PORT7
Idle	Internal	1	1	Data	Data	Data	Data	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data	Data	Data	Data	Data
Power Down	Internal	0 [1] 1 [2]	0 [1] 1 [2]	Data	Data	Data	Data	Data	Data	Data	Data
Power Down	External	0 [1] 1 [2]	0 [1] 1 [2]	Float	Data	Data	Data	Data	Data	Data	Data

Table 9-1: Status of external pins during Idle and Power Down

Note:

1. When PWDNH=0.
2. When PWDNH=1.

14. PULSE-WIDTH-MODULATED (PWM) OUTPUTS

14.1 PWM Features

The PWM block supports the following features;

- Four 12-bit PWM channels or complementary pairs:
  - 4 independent PWM outputs: PWM0, PWM2, PWM4 & PWM6.
  - 4 complementary PWM pairs with insertion of programmable dead-time: (PWM0,PWM1), (PWM2,PWM3), (PWM4,PWM5), (PWM6,PWM7)
- Three operation mode:
  Edge aligned mode, Center aligned mode and Single shot mode.
- Programmable dead-time insertion between paired PWMs.
- Output override control for Electrically Commutated Motor operation.
- Hardware/software brake protection.
- Support 2 independent interrupts:
  - Interrupt request when up/down counter comparison matched or underflow.
  - Interrupt request when external brake asserted.
- Flexible operation in debug mode.
- High Source/Sink current.

The outputs for PWM0 to PWM7 are on P2[5:0] (PWM[5:0]) and P5[1:0] (PWM [7:6]) respectively. After CPU reset, the internal output of each PWM channel depends on the output controls and polarity settings. The interval between successive outputs is controlled by a 12–bit up/down counter which uses the oscillator frequency with configurable internal clock prescaler as its input. The PWM counter clock, has the frequency as the clock source F_{PWM} = F_{OSC}/Prescaler. The following is the block diagram for PWM.

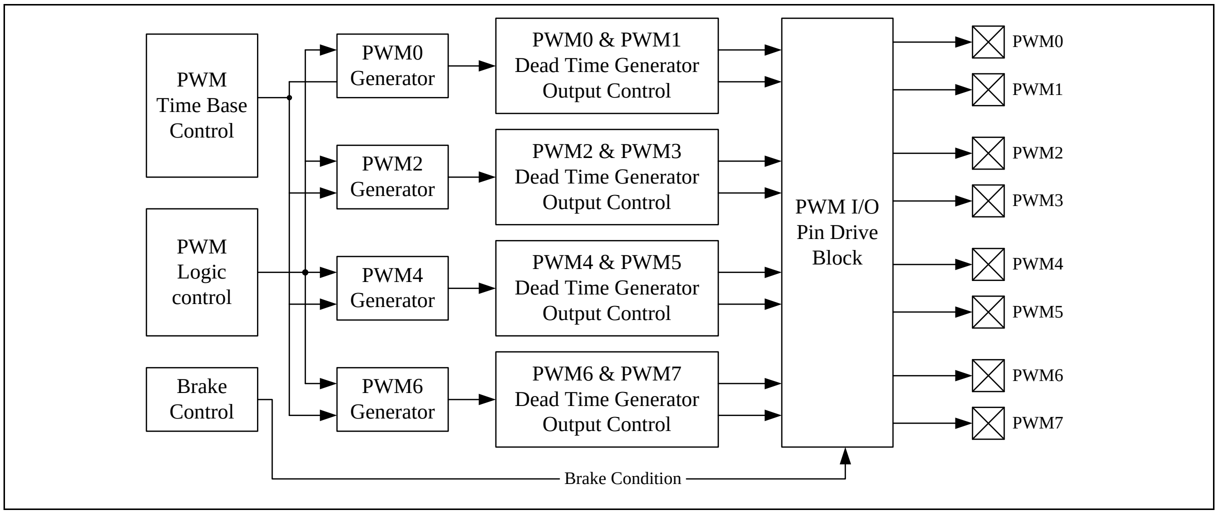

Figure 14-1: PWM Block Diagram

14.4 Complementary PWM with Dead-time and Override functions

In this module there are four duty-cycle generators, from 0 through 3. The total of eight PWM output pins in this module, from 0 through 7. The eight PWM outputs are grouped into output pairs of even and odd numbered outputs. In complimentary modes, the odd PWM pins must always be the complement of the corresponding even PWM pin. For example, PWM1 will be the complement of PWM0. PWM3 will be the complement of PWM2, PWM5 will be the complement of PWM4 and PWM7 will be the complement of PWM6. Complementary mode is enabled only when both PWMeEN and the corresponding PWMoEN are set to high. The time base for the PWM module is provided by its own 12-bit timer, which also incorporates selectable prescaler options.

Note: PWM pairs of (PWM2, 3), (PWM4, 5) and (PWM6, 7) are in the same structure as pair of (PWM0, 1). (Refer to Figure 14-9).

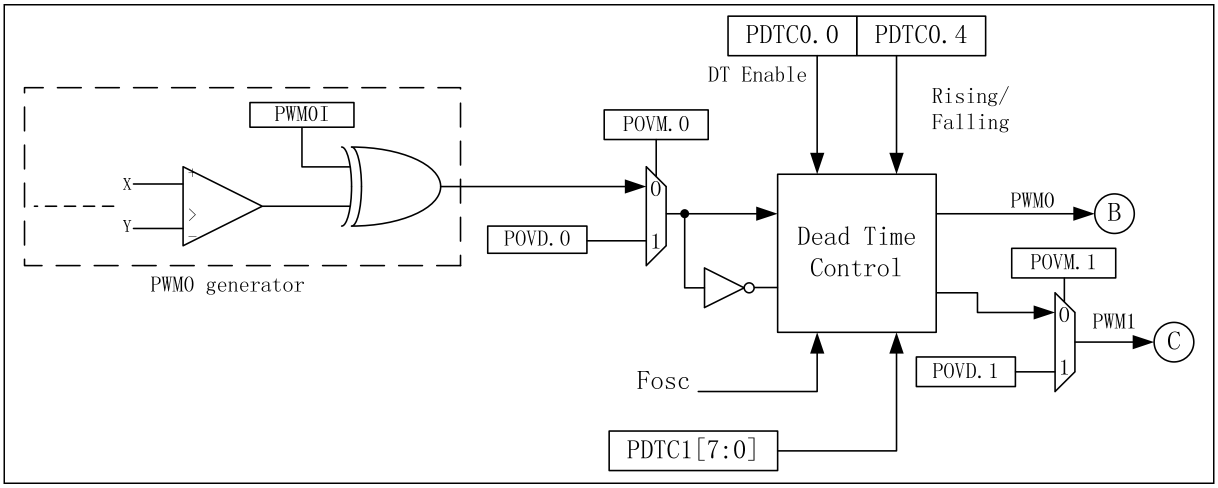

Figure 14-9: Complementary PWM with Dead-time and Override functions

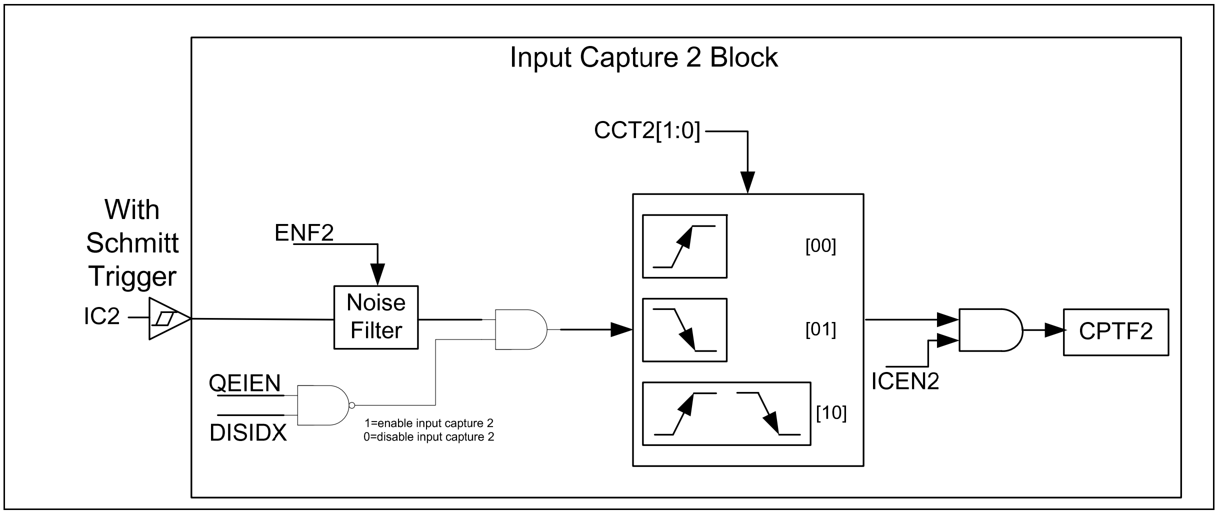

Figure 15-3: Input Capture 2 block diagram

Note: When QEI enabled (QEIEN=1), input capture 2 (IC2) still can detect edge changes.

.

The following table shows the bits setting for enabling input capture 2 edge detection.

QEIEN	DISIDX	ICEN2	INPUT CAPTURE 2 EDGE DETECTION
0	X(don't care)	0	Disabled.
		1	Enabled.
1	0	0	Disabled.
		1	Enabled.
1	1	X	Disabled,

upon matching with RCAP3 value, TF3 will be set (which will generate an interrupt request if enable Timer 3 interrupt ET3 is enabled) and the timer reload from 0 and starts counting again.

15.1.2 Reload Mode

Timer 3 can be also be configured for reload mode. The reload mode is enabled by clearing the CMP/$\overline{\text{RL3}}$ bit to 0 in the T3CON register. In this mode, RCAP serves as a reload register. When timer 3 overflows, a reload is generated that causes the contents of the RCAP3L and RCAP3H registers to be reloaded into the TL3 and TH3 registers, if ENLD is set. TF3 flag is set, and interrupt request is generated if enable Timer 3 interrupt ET3 is enabled. However, if ENLD = 0, timer 3 will be reload with 0, and count up again.

Alternatively, other reload source is also possible by the input capture pins by configuring the CCLD [1:0] bit. If the ICENx bit is set, then a trigger of external IC0, IC1 or IC2 pin (respectively) will also cause a reload. This action also sets the CPTF0, CPTF1 or CPTF2 flag bit in SFR CAPCON1, respectively.

15.2 Quadrature Encoder Interface (QEI)

The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses quadrature encoder for feedback. The QEI block supports the features as below:

- Two QEI phase inputs: QEA and QEB.
- 16-bit Up/Down Pulse Counter (PLSCNT) with 16-bit read access latched buffer (PCNT).
- Four pulse counter update modes:
  - Mode0: x4 free-counting mode.
  - Mode1: x2 free-counting mode.
  - Mode2: x4 compare-counting mode.
  - Mode3: x2 compare-counting mode.
- Three interrupt sources:
  - Pulse counter interrupt (CPTF0/QEIF).
  - Direction index of motion detection with direction interrupt (CPTF1/DIRF).
  - Input Capture 2 interrupt (CPTF2).
- The three 16-bit SFRs in QEI share the same addresses with the capture counter registers.

INPUT CAPTURE MODE	QEI MODE
Capture0 Counter Register (CCH0, CCL0)	Pulse Read Counter Register (PCNTH, PCNTL)
Capture1 Counter Register (CCH1, CCL1)	Pulse Counter Register (PLSCNTH, PLSCNTL)
Capture2 Counter Register (CCH2, CCL2)	Maximum Counter Register (MAXCNTH, MAXCNTL)

In QEI mode, IC1 and IC0 work as QEB and QEA inputs respectively. QEA and QEB accept the outputs from a quadrature encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.

16.6 Multiprocessor Communications

Multiprocessor communication is available in modes 1, 2 and 3 and makes use of the 9th data bit and the automatic address recognition feature. This approach eliminates the software overhead required to check every received address and greatly simplifies the program.

In modes 2 and 3, address bytes are distinguished from data bytes by 9th bit set, which is set high in address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends the address of the target slave(s). The slave processors have already set their SM2 bits high so that they are only interrupted by an address byte. The automatic address recognition feature then ensures that only the addressed slave is actually interrupted. This feature compares the received byte to the slave's Given or Broadcast address and only sets the RI flag if the bytes match. This slave then clears the SM2 bit, clearing the way to receive the data bytes. The unaddressed slaves are not affected, as they are still waiting for their address.

In mode 1, the 9th bit is the stop bit, which is 1 in valid frames. Therefore, if SM2 is 1, RI is only set if a valid frame is received and if the received byte matches the Given or Broadcast address.

The master processor can selectively communicate with groups of slaves using the Given Address or all the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN registers. The slave address is the 8-bit value specified in SADDR. SADEN is a mask for the value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is a don't-care condition in the address comparison. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This provides flexibility to address multiple slaves without changing addresses in SADDR.

The following example shows how to setup the Given Addresses to address different slaves.

Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given Address for slaves 1 and 2 differ in the LSB. In slave 1, it is a don't-care, while, in slave 2, it is 1. Thus, to communicate with only slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly, bit 1 is 0 for slave 1 and don't-care for slave 2. Hence, to communicate only with slave 2, the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. Since bit 3 is don't-care for both slaves, two different addresses can address both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously using the Broadcast Address. The Broadcast Address is formed from the logical OR of the SADDR and SADEN registers. The zeros in the result are don't–care values. In most cases, the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN registers are located at addresses A9h and B9h, respectively. These two registers default to 00h, so the Given Address and Broadcast Address default to XXXX XXXX (i.e., all bits don't-care), which effectively removes the multiprocessor communications feature

17.4.1 Master/Transmitter Mode

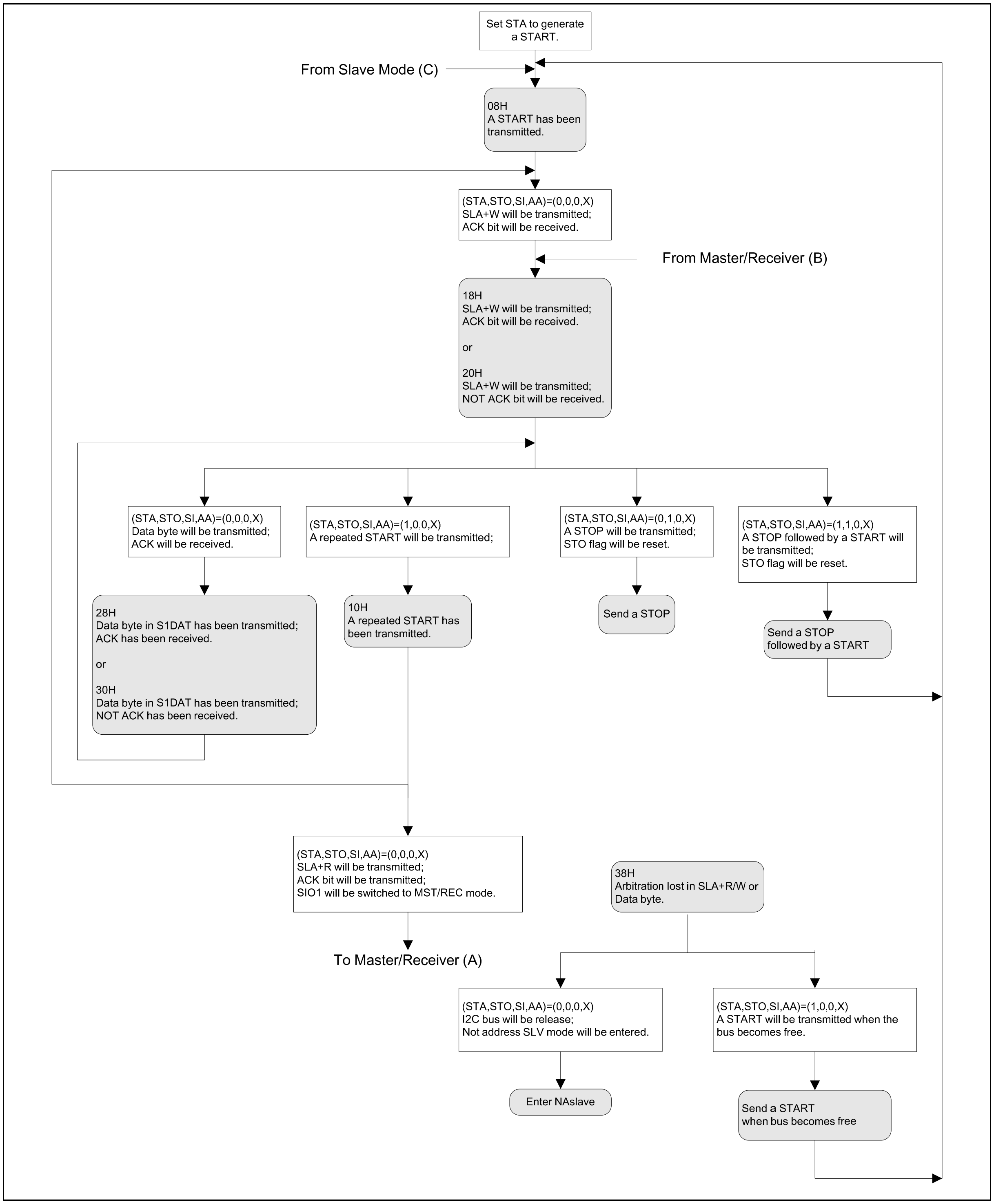

Figure 17-5: Master Transmitter Mode

17.4.5 GC Mode

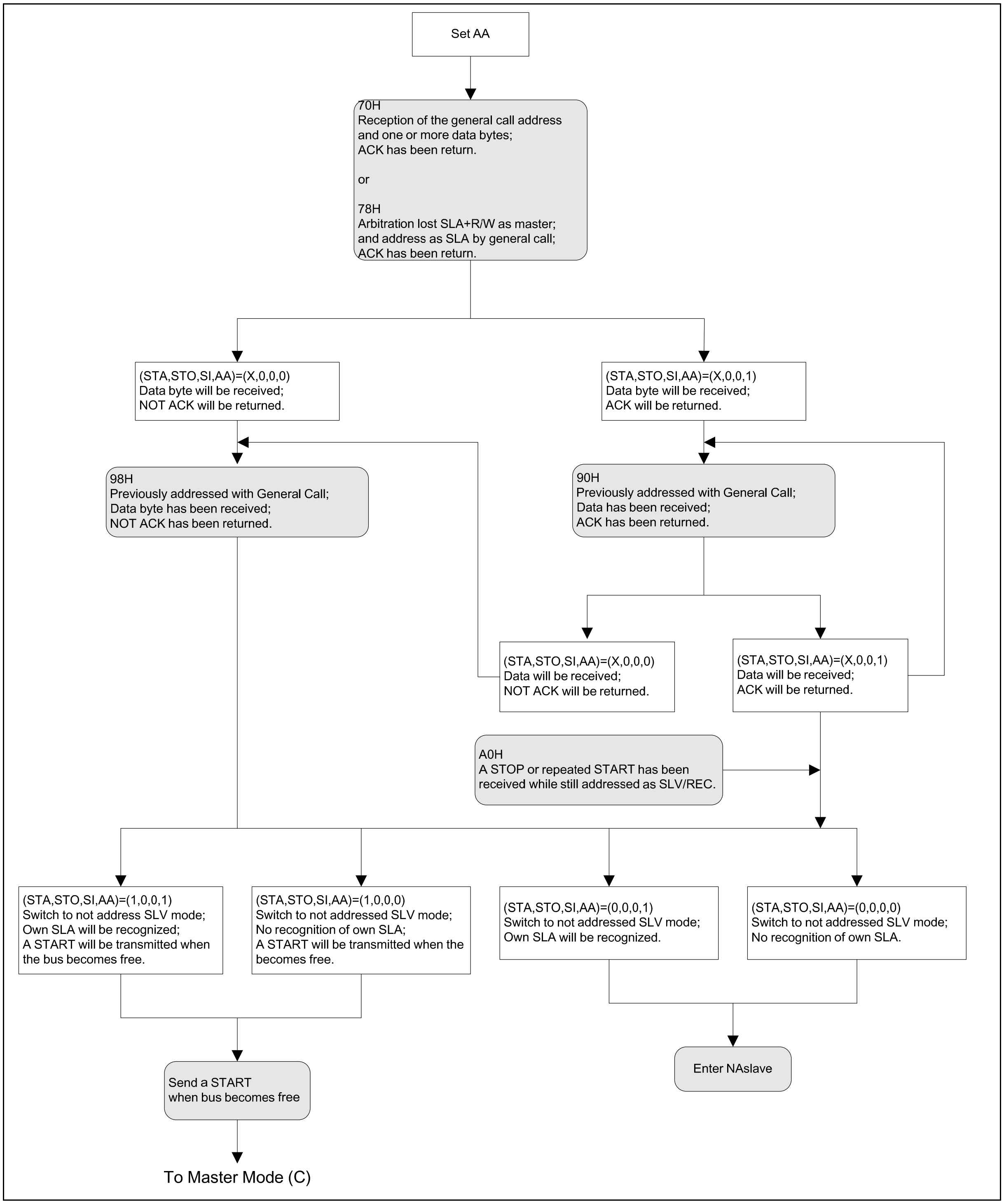

Figure 17-9: General Call Address

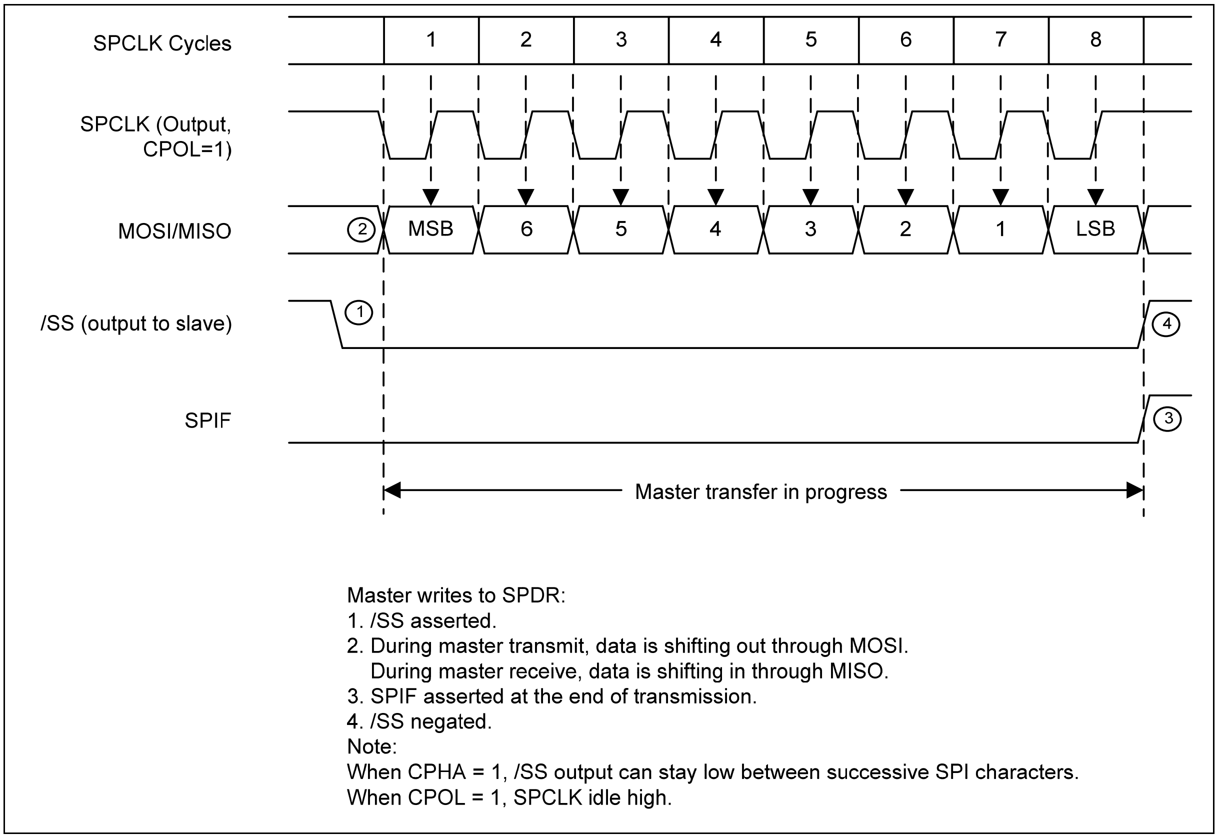

Figure 18-5: Master Mode Transmission (CPOL = 1, CPHA = 1)

18.3.2 Slave Mode

When in slave mode, the SPCLK pin becomes input and it will be clock by another master SPI device. The $\overline{SS}$ pin also becomes input. Similarly, before data transmissions occurs, and remain low until the transmission completed. If $\overline{SS}$ goes high, the SPI is forced into idle state. If the $\overline{SS}$ is forced to high at the middle of transmission, the transmission will be aborted and the receiving shifter buffer will be high and goes into idle states.

Data flows from master to slave on MOSI pin and flows from slave to master on MISO pin. The SPDR is used when transmitting or receiving data on the serial bus. Only a write to this register initiates transmission or reception of a byte, and this only occurs in the master device. At the completion of transferring a byte of data, the SPIF status bit is set in both the master and slave devices.

A read of the SPDR is actually a read of a buffer. To prevent an overrun and the loss of the byte that caused the overrun, the first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated.

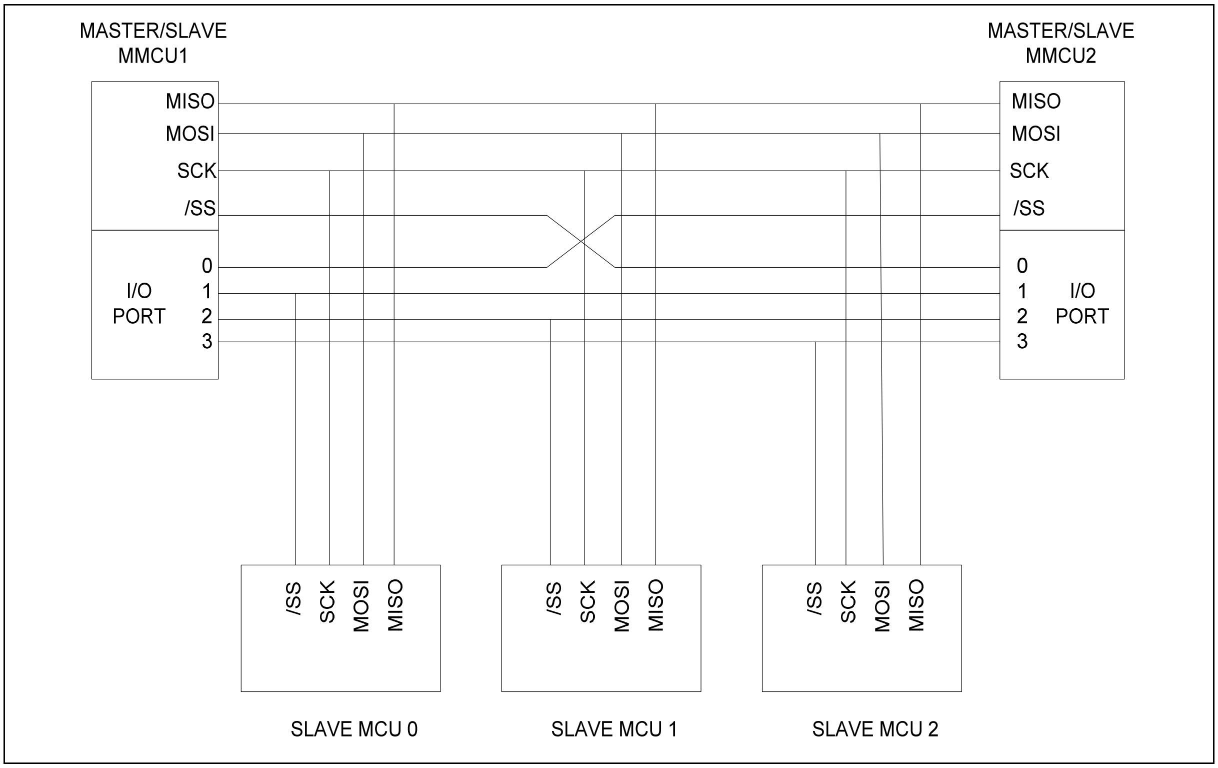

Figure 18-12: SPI multi-master slave environment

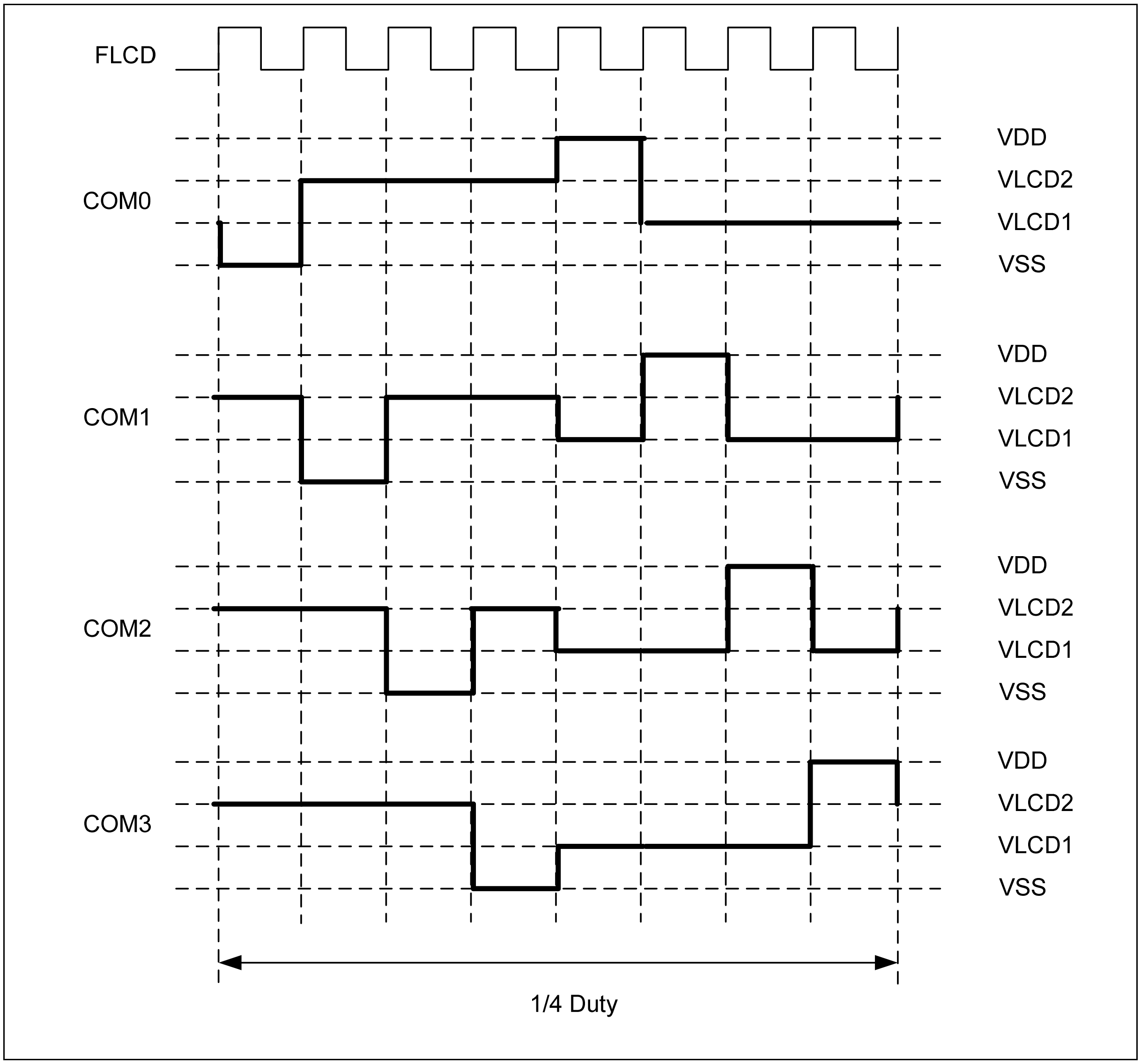

Figure 20-7: LCD com output pins configured using Voltage Pump B type with ¼ duty.

```
MOV  R6,#D0H                        ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT
15 ms DEPENDING ON USER'S SYSTEM CLOCK RATE.
MOV R7, #8AH
MOV TL0, R6
MOV TH0, R7

ERASE_P_4K:
MOV SFRCN, #22H                     ; SFRCN = 22H, ERASE APFlash APFlash0
                                    ; SFRCN = A2H, ERASE APFlash1
MOV TCON, #10H                      ; TCON = 10H, TR0 = 1, GO
MOV PCON, #01H                      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
MOV SFRCN, #0H                      ; SFRCN = 00H, READ APFlashB APFlash0
                                    ; SFRCN = 80H, READ APFlashB APFlash1
MOV SFRAH, #0H                      ; START ADDRESS = 0H
MOV SFRAL, #0H
MOV R6, #FDH                        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
MOV R7, #FFH
MOV TL0, R6
MOV TH0, R7

blank_check_loop:
SETB TR0                            ; Enable TIMER 0
MOV PCON, #01H                      ; Enter idle mode
MOV A, SFRFD                        ; Read one byte
CJNE A, #FFH, blank_check_error
INC SFRAL                           ; Next address
MOV A, SFRAL
JNZ   blank_check_loop
INC  SFRAH
MOV A, SFRAH
CJNE A, #0H, blank_check_loop       ; End address = FFFFH
JMP PROGRAM_APFlashROM

blank_check_error:
JMP $

;******************************************************************************
;* RE-PROGRAMMING APFlashB APFlash BANK
;******************************************************************************
PROGRAM_APFlashROM:
```