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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	8MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	29
Program Memory Size	8KB (8K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-SOP (0.330", 8.40mm Width)
Supplier Device Package	36-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m37547g2fp-u0

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Table 1 Performance overview

Parameter			Function
Number of basic instructions			71
Instruction execution time			0.25 μs (Minimum instruction, oscillation frequency 8 MHz: double-speed mode)
Oscillation frequency			8 MHz (max.)
Memory sizes	ROM		8 K to 16 K bytes
	RAM		384 to 512 bytes
I/O port	P0, P1, P2, P3		•8-bit × 3, 5-bit × 1
Interrupts			18 sources, 16 vectors
Timer			•8-bit × 2, 16-bit × 2
Output compare			4 channel
Input capture			2 channel
Serial interface			8-bit × 2 (UART or clock synchronous)
A/D converter			10-bit × 8 channel
Watchdog timer			16-bit × 1
Clock generating circuit			Built-in (external ceramic resonator or quartz-crystal oscillator, RC oscillation available) (Low consumption current by on-chip oscillator available)
Power source voltage (at ceramic resonance)	Double-speed mode	At 8MHz oscillation	4.5 to 5.5 V
		At 6.5MHz oscillation	4.0 to 5.5 V
		At 2MHz oscillation	2.4 to 5.5 V
		At 1MHz oscillation	2.2 to 5.5 V
	High-speed mode Middle-speed mode	At 8MHz oscillation	4.0 to 5.5 V
		At 4MHz oscillation	2.4 to 5.5 V
		At 2MHz oscillation	2.2 to 5.5 V
Power source voltage (at RC oscillation)	High-speed mode Middle-speed mode	At 4MHz oscillation	4.0 to 5.5 V
		At 2MHz oscillation	2.4 to 5.5 V
		At 1MHz oscillation	2.2 to 5.5 V
Power source voltage (at on-chip oscillation)			1.8 to 5.5 V
Power dissipation			29.5 mW (Typ.)
Operating temperature range			-20 to 85 °C
Device structure			CMOS silicon gate
Package			36-pin plastic molded SSOP

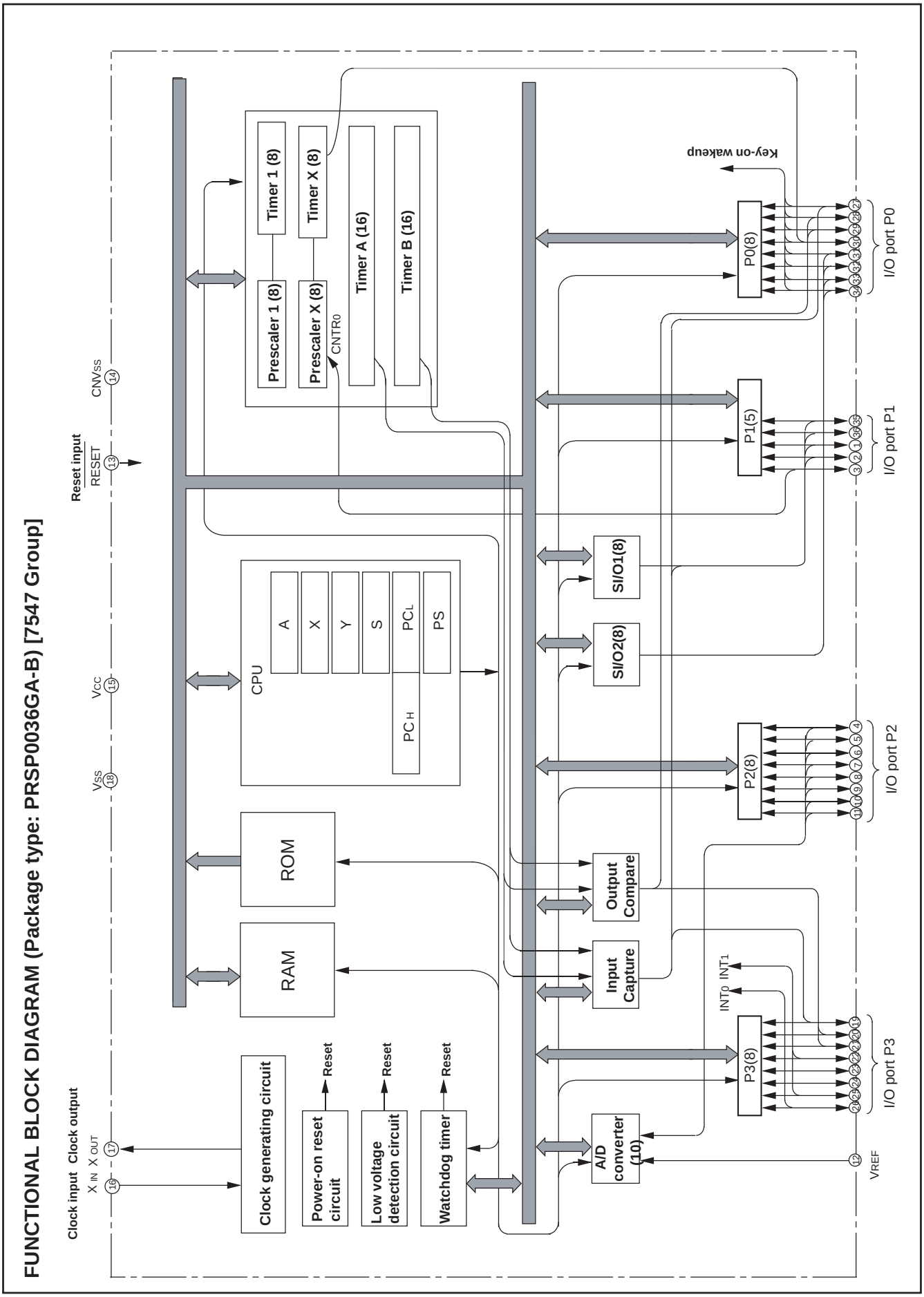


Fig. 2 Functional block diagram (Package type: PRSP0036GA-B)

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.
After reset, the Interrupt disable (I) flag is set to “1”, but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

(3) Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is “1”.
When an interrupt occurs, this flag is automatically set to “1” to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”. The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)
When the T flag is “0”, arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Code Protect Address (address $FFDB_{16}$)

Address $FFDB_{16}$, which is the reserved ROM area of QzROM, is the ROM code protect address. "00_{16}" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00_{16}" or "FF_{16}" can be selected as the ROM option setup (referred to as "Mask option setup" in MM) when ordering.

■ **Notes**

Because the contents of RAM are indefinite at reset, set initial values before using.

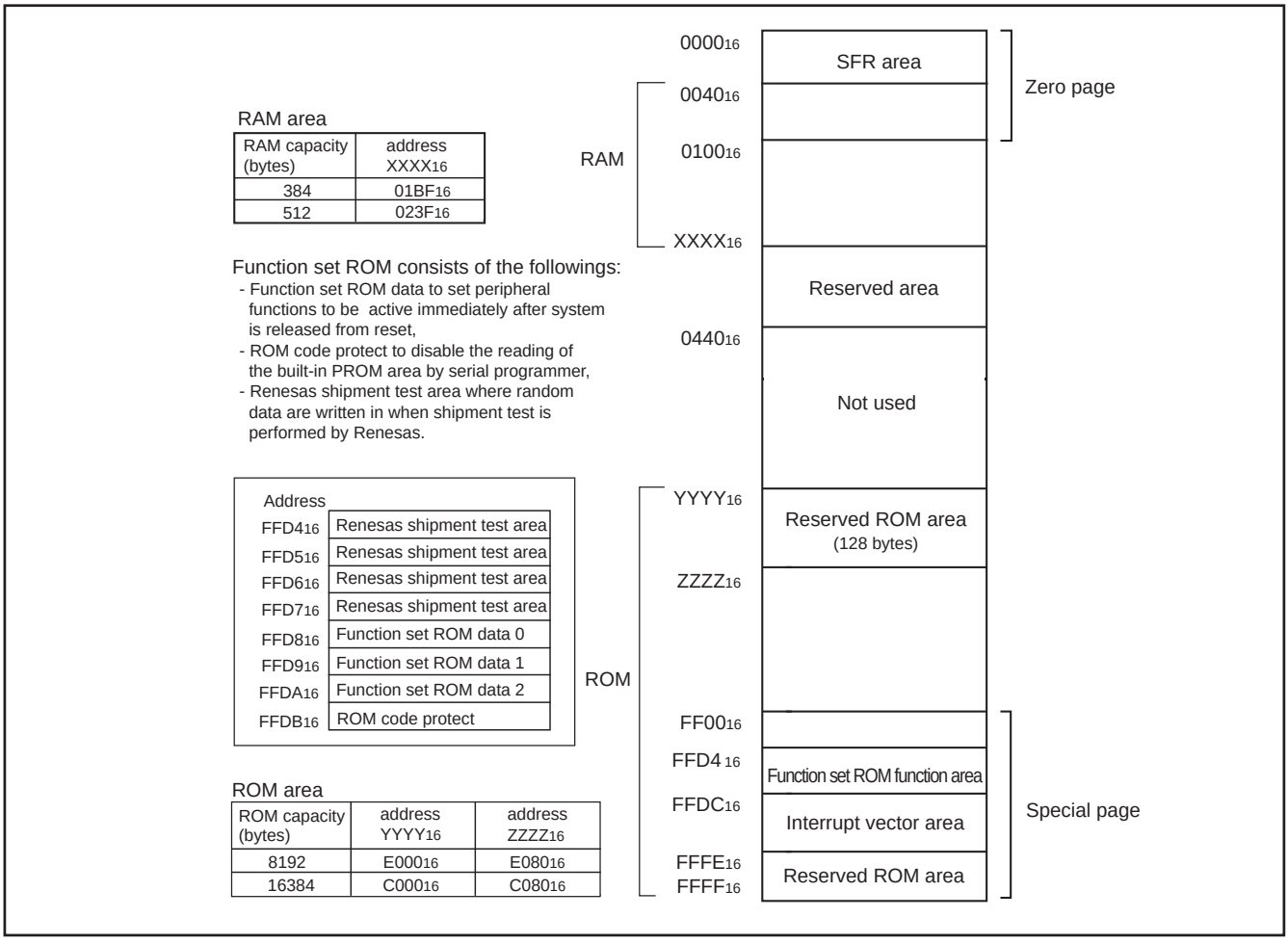


Fig. 6 Memory map diagram

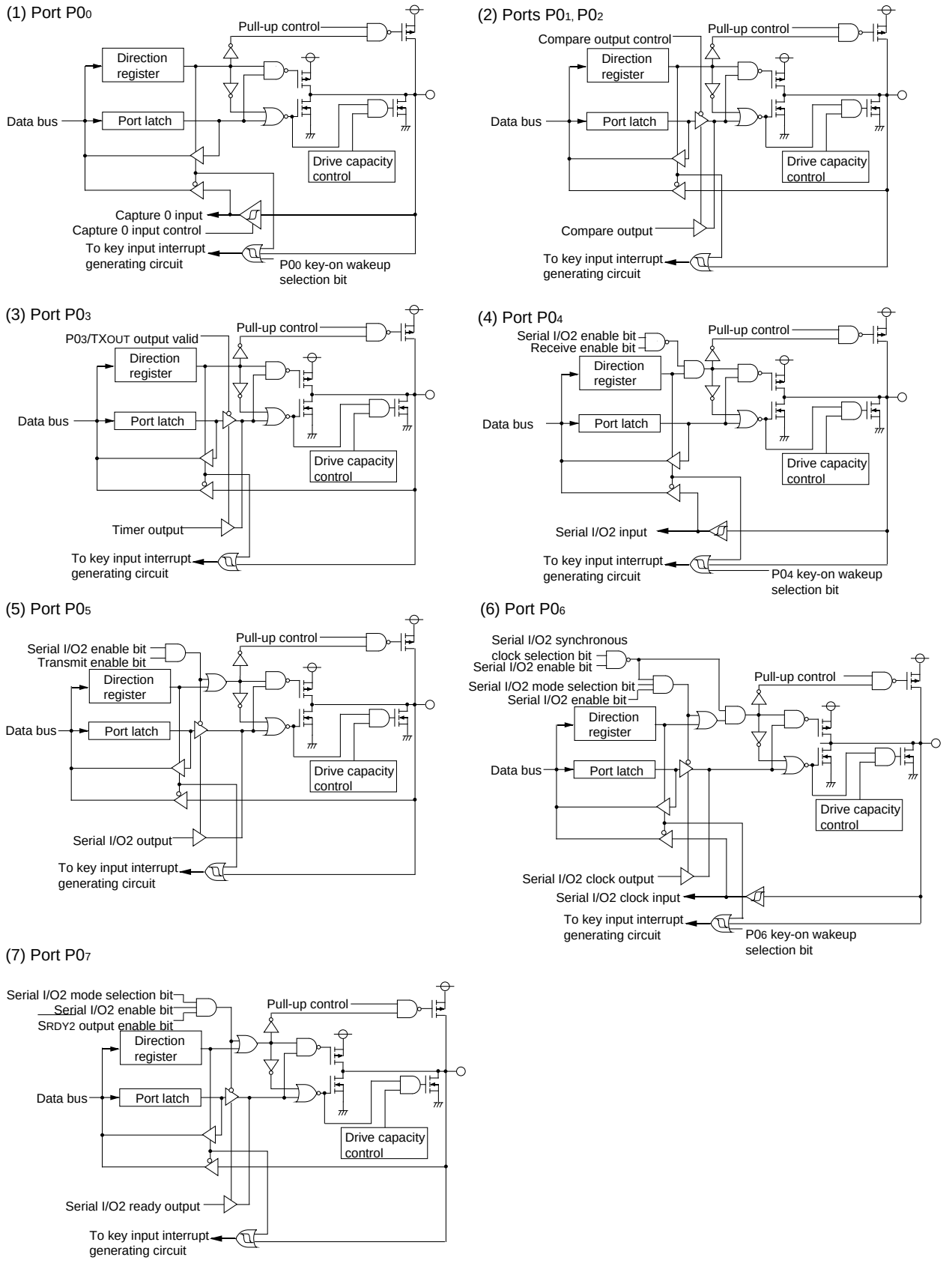


Fig. 13 Block diagram of ports (1)

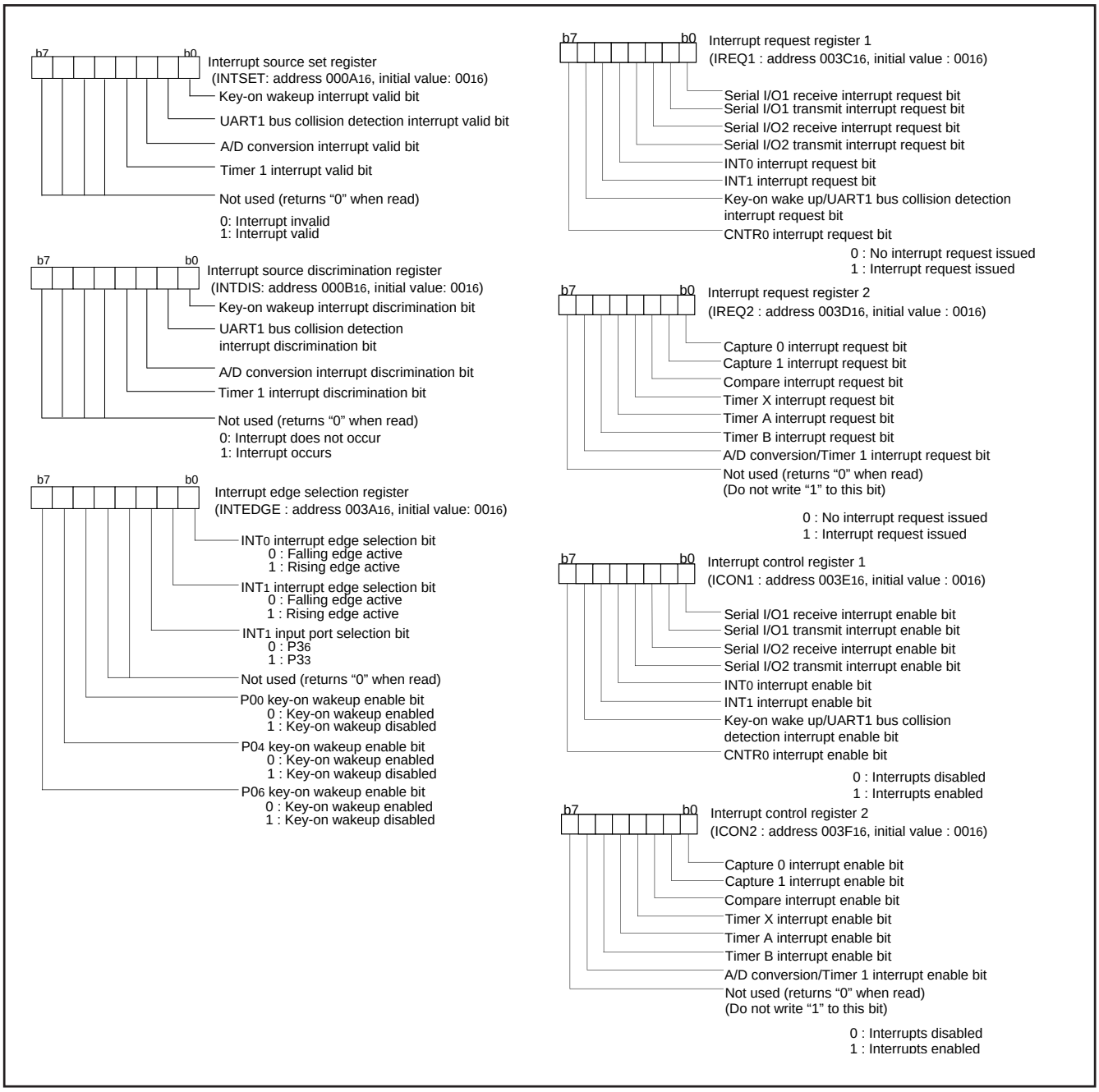


Fig. 17 Structure of Interrupt-related registers

Output compare

7547 group has 4-output compare channels. Each channel (0 to 3) has the same function and can be used to output waveform by using count value of either Timer A or Timer B.
The source timer for each channel is selected by setting value of the compare x (x = 0, 1, 2, 3) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each compare channel, set “1” to the compare x output port bit and set the port direction register corresponding to compare channel to output mode.

The compare value for each channel is set to the compare register (low-order) and compare register (high-order).
Writing to the register for each channel is controlled by setting value of compare register write pointer. Writing to each register is in the following order;

1. Set the value of corresponded output compare channel to the compare register write pointer.
2. Write a value to the compare register (low-order) and compare register (high-order).
3. Set “1” to the compare latch y (y = 00, 01, 10, 11, 20, 21, 30, 31) re-load bit.
   When “1” is set to the compare latch y re-load bit, the value set to the compare register is loaded to compare latch when the next timer underflow.

When count value of timer and setting value of compare latch is matched, compare output trigger occurs.
When “1: Enabled” is set to the compare trigger x enable bit, the output waveform from port is inverted by compare trigger.
When “0: Disabled” is set to the compare trigger x enable bit, the output waveform is not inverted, so port output can be fixed to “H” or “L”.

When “0: Positive” is set to the compare x output level latch, the compare output waveform is turned to “H level” at compare latch x0’s match and turned to “L level” at compare latch x1’s match.
When “1 :Negative” is set to the compare x output level latch, the compare output waveform is turned to “L level” at compare latch x0’s match and turned to “H level” at compare latch x1’s match.
The compare output level of each channel can be confirmed by reading the compare x output status bit.

Compare output interrupt is available when match of each compare channel and timer count value. The interrupt request from each channel can be disabled or enabled by setting value of compare latch y interrupt source bit.

Compare 0,1 (2,3) modulation mode

In compare modulation mode, modulation waveform can be generated by using compare channel 0 and 1, or compare channel 2 and 3.
To use this mode,

- Set “1: Enabled” to the compare 0,1 (2, 3) modulation mode bit.
- Set Timer A underflow for Timer B count source.
- Set Timer A for the timer source of compare channel 0 (2).
- Set Timer B for the timer source of compare channel 1 (3).

In this mode, AND waveform of compare 0 (1) and compare 2 (3) is generated from Port $P0_1$ and $P3_1$, respectively. Accordingly, in order to use this mode, set “1” to the compare 0 output port bit or compare 2 output port bit.

■ Notes on Output Compare

- When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
- Do not write the same data to both of compare latch x0 and x1.
- When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to “L” or “H” level.
  However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare match interrupt occurs.
- When the compare x trigger enable bit is cleared to “0” (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to “L” or “H” level.
  However, in this case, the compare match signal is generated. Accordingly, compare match interrupt occurs.

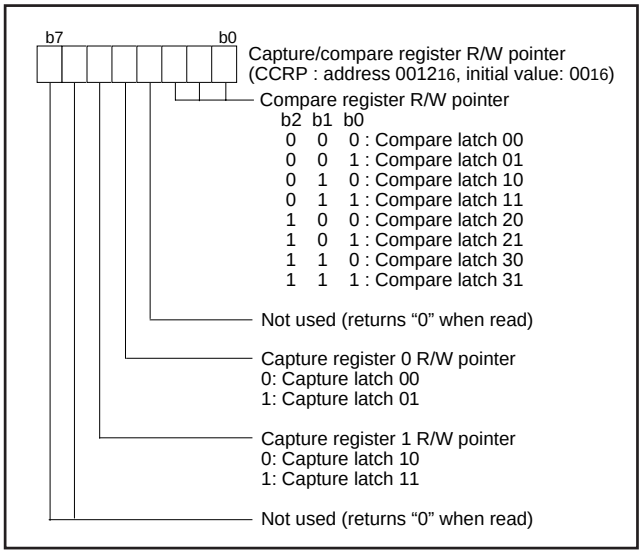


Fig. 28 Structure of capture/compare register R/W pointer

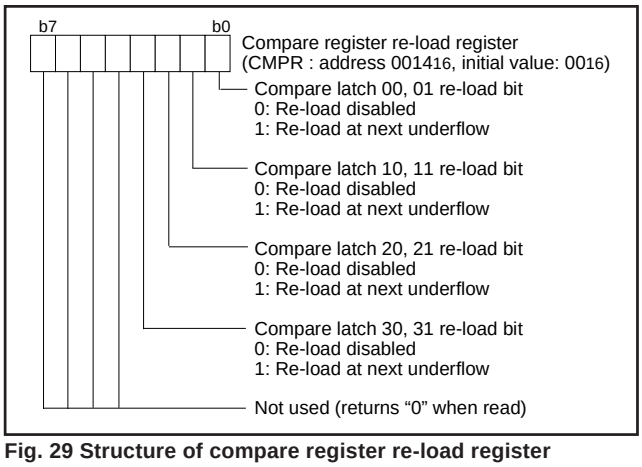


Fig. 29 Structure of compare register re-load register

[Transmit buffer register 1/receive buffer register 1 (TB1/RB1)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 status register (SIO1STS)] 0019$_{16}$

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 control register (SIO1CON)] 001A$_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 control register (UART1CON)] 001B$_{16}$

The UART1 control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P11/TxD1 pin.

[Baud rate generator 1 (BRG1)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes on Serial I/O1

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
② Set the transmit enable bit to "1".
③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O1 is enabled.

The functions of P12 and P13 are switched with the setting values of a serial I/O1 mode selection bit and a serial I/O1 synchronous clock selection bit as follows.

(1) Serial I/O1 mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O1 synchronous clock selection bit
"0" : P12 pin turns into an output pin of a synchronous clock.
"1" : P12 pin turns into an input pin of a synchronous clock.
Setup of a $\overline{\text{SRDY1}}$ output enable bit (SRDY)
"0" : P13 pin can be used as a normal I/O pin.
"1" : P13 pin turns into a $\overline{\text{SRDY1}}$ output pin.

(2) Serial I/O1 mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O1 synchronous clock selection bit
"0": P12 pin can be used as a normal I/O pin.
"1": P12 pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is P13 pin. It can be used as a normal I/O pin.

Bus collision detection (SIO1)

SIO1 can detect a bus collision by setting UART1 bus collision detection interrupt enable bit.

When transmission is started in the clock synchronous or asynchronous (UART) serial I/O mode, the transmit pin TxD_1 is compared with the receive pin RxD_1 in synchronization with rising edge of transmit shift clock. If they do not coincide with each other, a bus collision detection interrupt request occurs.

When a transmit data collision is detected between LSB and MSB of transmit data in the clock synchronous serial I/O mode or between the start bit and stop bit of transmit data in UART mode, a bus collision detection can be performed by both the internal clock and the external clock.

A block diagram is shown in Fig. 54.
A timing diagram is shown in Fig. 55.

Note: Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

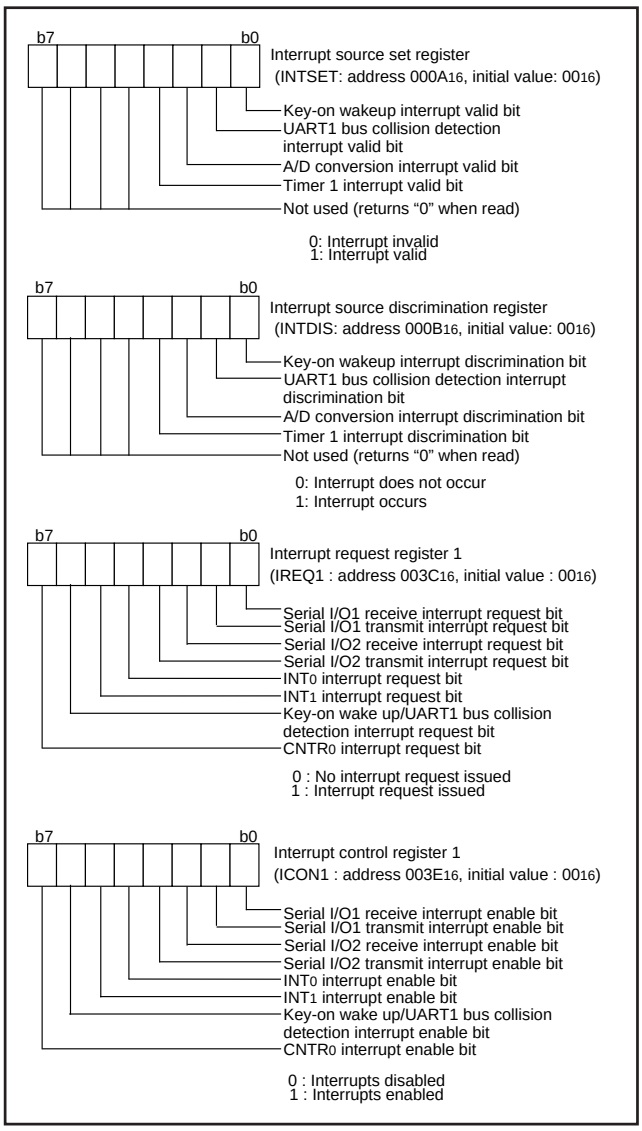


Fig. 53 Bus collision detection circuit related registers

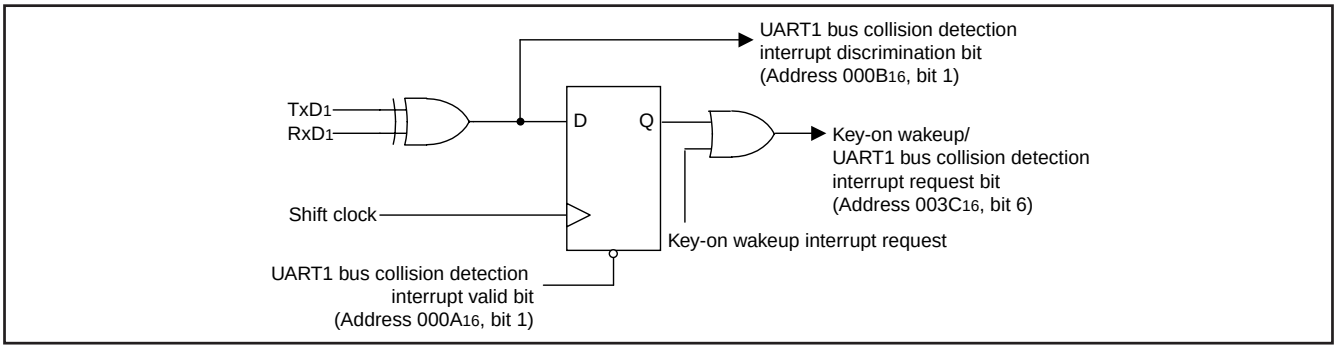


Fig. 54 Block diagram of bus collision detection interrupt circuit

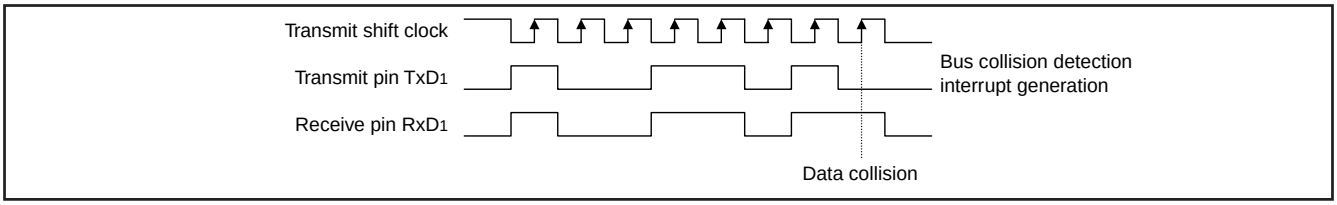


Fig. 55 Timing diagram of bus collision detection interrupt

●Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O2 Mode

Clock synchronous serial I/O2 mode can be selected by setting the serial I/O2 mode selection bit of the serial I/O2 control register (bit 6) to "1".

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

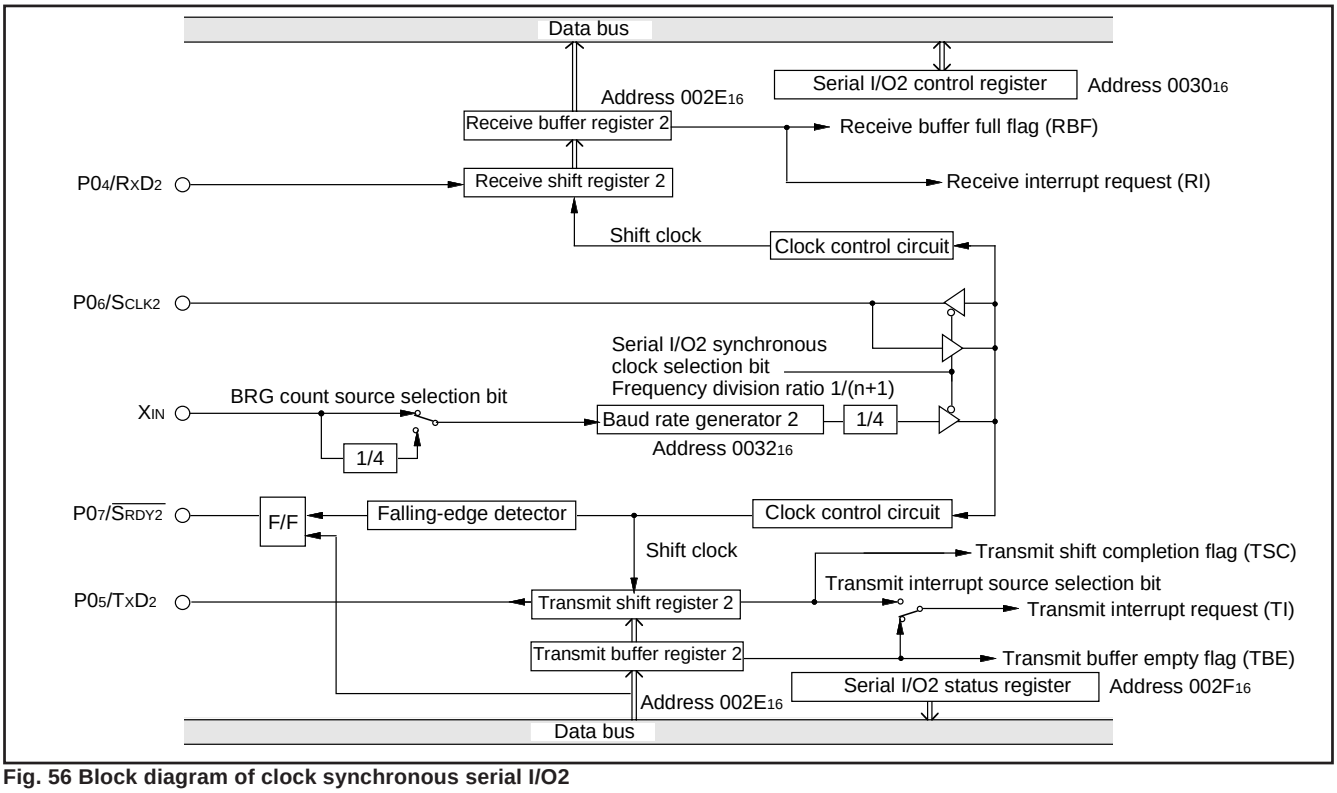
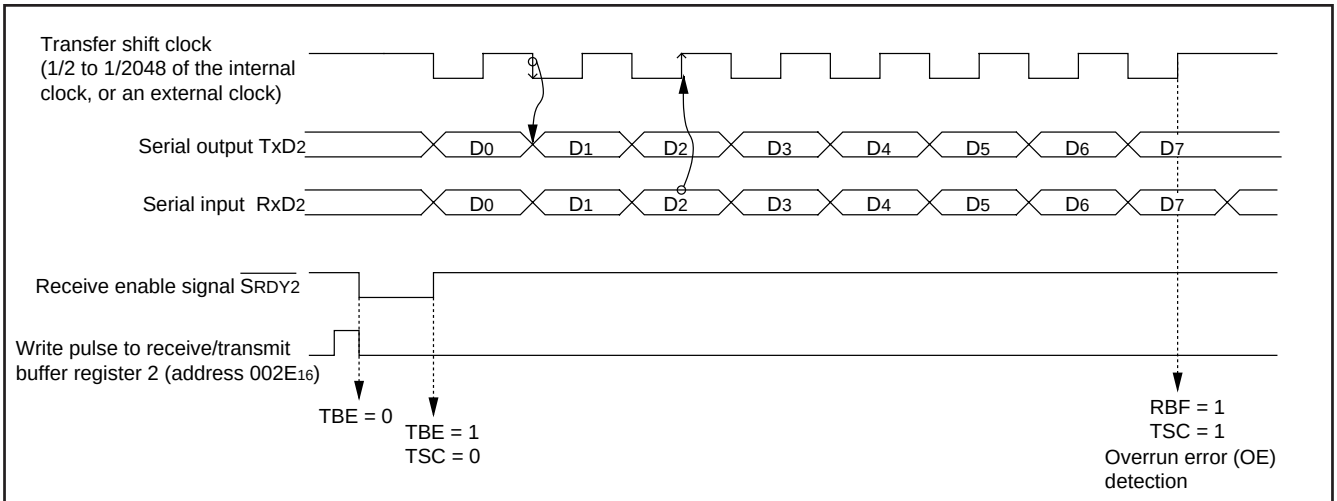


Fig. 56 Block diagram of clock synchronous serial I/O2



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O2 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD_2 pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 57 Operation of clock synchronous serial I/O2 function

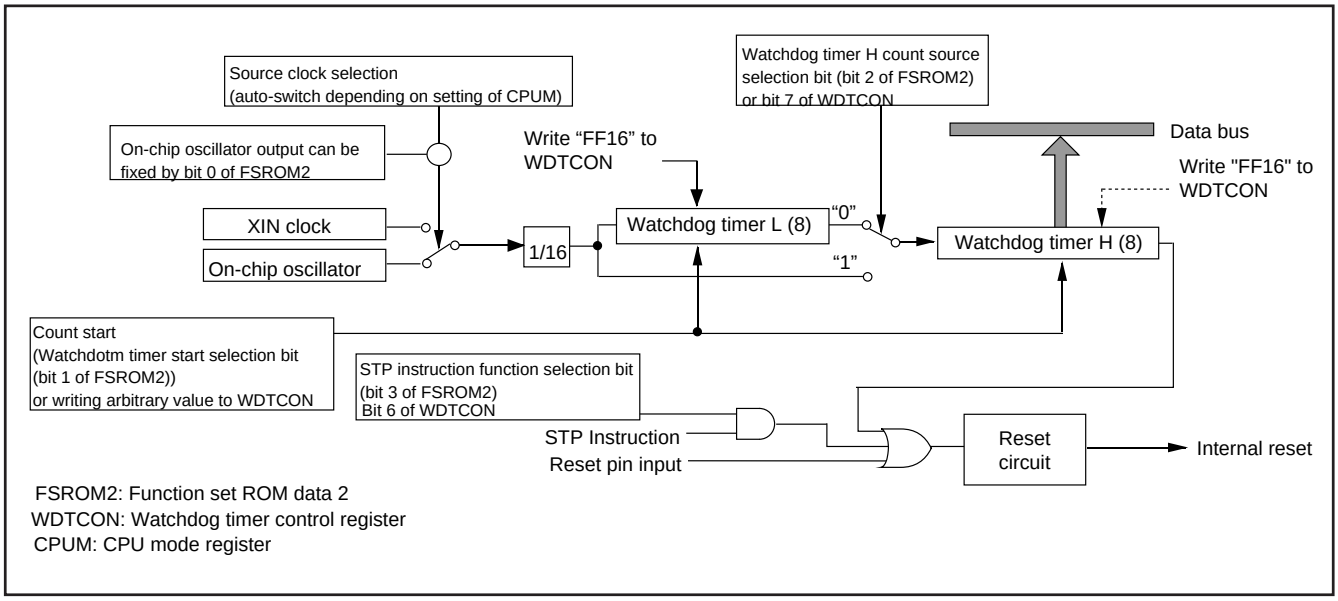
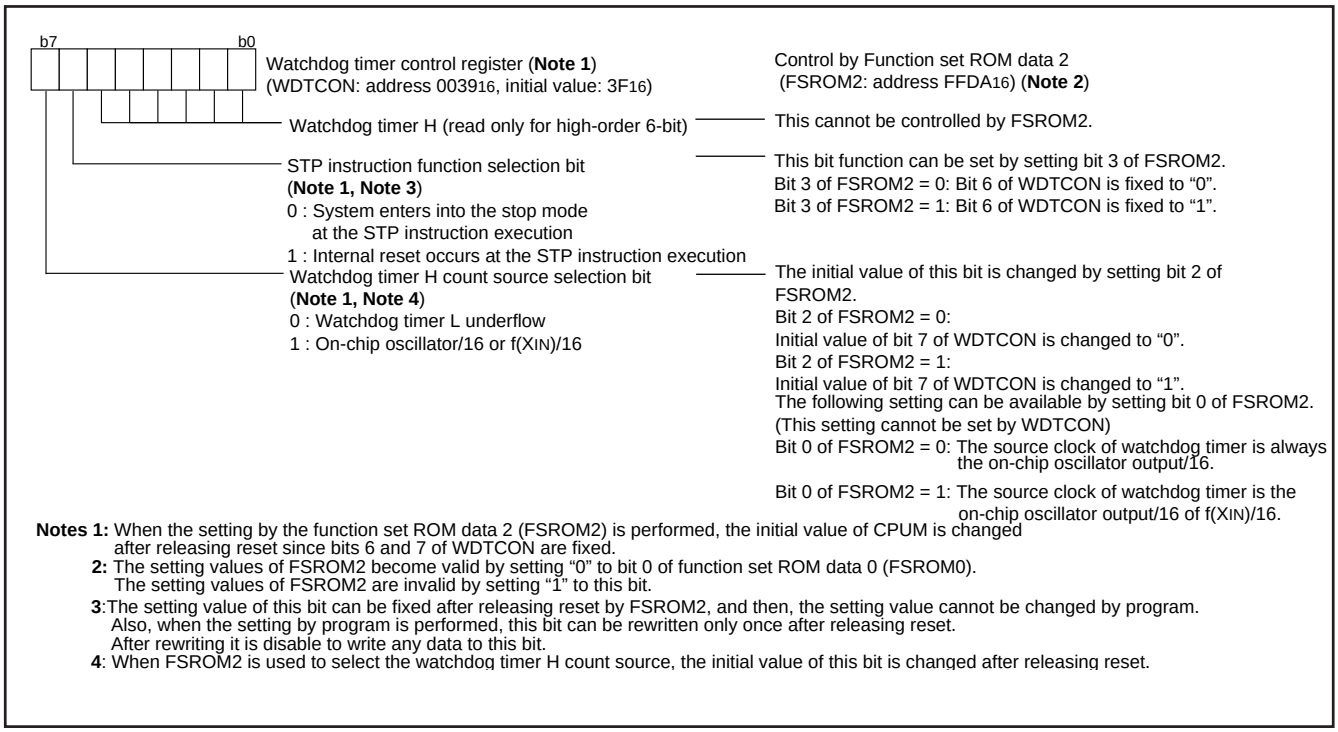


Fig. 64 Block diagram of watchdog timer



Notes 1: When the setting by the function set ROM data 2 (FSROM2) is performed, the initial value of CPUM is changed after releasing reset since bits 6 and 7 of WDTCON are fixed.

2: The setting values of FSROM2 become valid by setting “0” to bit 0 of function set ROM data 0 (FSROM0). The setting values of FSROM2 are invalid by setting “1” to this bit.

3:The setting value of this bit can be fixed after releasing reset by FSROM2, and then, the setting value cannot be changed by program. Also, when the setting by program is performed, this bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit.

4: When FSROM2 is used to select the watchdog timer H count source, the initial value of this bit is changed after releasing reset.

Fig. 65 Structure of watchdog timer control register

	Address	Register contents
(1) Port P0 direction register (P0D)	0001_{16}	00_{16}
(2) Port P1 direction register (P1D)	0003_{16}	X X X 0 0 0 0 0
(3) Port P2 direction register (P2D)	0005_{16}	00_{16}
(4) Port P3 direction register (P3D)	0007_{16}	00_{16}
(5) Interrupt source set register (INTSET)	$000A_{16}$	00_{16}
(6) Interrupt source discrimination register (INTDIS)	$000B_{16}$	00_{16}
(7) Compare register (low-order) (CMPL)	0010_{16}	00_{16}
(8) Compare register (high-order) (CMPH)	0011_{16}	00_{16}
(9) Capture/Compare register R/W pointer (CCRP)	0012_{16}	00_{16}
(10) Capture software trigger register (CSTR)	0013_{16}	00_{16}
(11) Compare register re-load register (CMPR)	0014_{16}	00_{16}
(12) Port P0P3 drive capacity control register (DCCR)	0015_{16}	00_{16}
(13) Pull-up control register (PULL)	0016_{16}	00_{16}
(14) Port P1P3 control register (P1P3C)	0017_{16}	00_{16}
(15) Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(16) Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(17) UART1 control register (UART1CON)	$001B_{16}$	1 1 1 0 0 0 0 0
(18) Timer A, B mode register (TABM)	$001D_{16}$	00_{16}
(19) Capture/Compare port register (CCPR)	$001E_{16}$	00_{16}
(20) Timer source selection register (TMSR)	$001F_{16}$	00_{16}
(21) Capture mode register (CAPM)	0020_{16}	00_{16}
(22) Compare output mode register (CMOM)	0021_{16}	00_{16}
(23) Capture/Compare status register (CCSR)	0022_{16}	00_{16}
(24) Compare interrupt source register (CISR)	0023_{16}	00_{16}
(25) Timer A (low-order) (TAL)	0024_{16}	FF_{16}
(26) Timer A (high-order) (TAH)	0025_{16}	FF_{16}
(27) Timer B (low-order) (TBL)	0026_{16}	FF_{16}
(28) Timer B (high-order) (TBH)	0027_{16}	FF_{16}
(29) Prescaler 1 (PRE1)	0028_{16}	FF_{16}
(30) Timer 1 (T1)	0029_{16}	01_{16}
(31) Timer count source set register (TCSS)	$002A_{16}$	00_{16}
(32) Timer X mode register (TXM)	$002B_{16}$	00_{16}
(33) Prescaler X (PREX)	$002C_{16}$	FF_{16}
(34) Timer X (TX)	$002D_{16}$	FF_{16}
(35) Serial I/O2 control register (SIO2STS)	$002F_{16}$	1 0 0 0 0 0 0 0
(36) Serial I/O2 register (SIO2CON)	0030_{16}	00_{16}
(37) UART2 control register (UART2CON)	0031_{16}	1 1 1 0 0 0 0 0
(38) A/D control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(39) On-chip oscillation division ratio selection register (RODR)	0037_{16}	0 0 0 0 0 0 1 0
(40) MISRG	0038_{16}	00_{16}
(41) Watchdog timer control register (WDTCON) (Note 3)	0039_{16}	0 0 1 1 1 1 1 1
(42) Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(43) CPU mode register (CPUM) (Note 3)	$003B_{16}$	1 0 0 0 0 0 0 0
(44) Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(45) Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(46) Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(47) Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(48) Processor status register	(PS)	X X X X X 1 X X
(49) Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$
(50) Watchdog timer H		FF_{16}
(51) Watchdog timer L		FF_{16}

Notes 1: X : Undefined
2: The content of other registers is undefined when the microcomputer is reset. The initial values must be surely set before you use it.
3: When the setting by the function set ROM data 2 (FSROM2) is performed, the initial values of these registers at reset are changed.

Fig. 69 Internal status of microcomputer at reset

● Oscillation stop detection circuit

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or RC oscillation circuit stops by disconnection. To use this circuit, set an on-chip oscillator to be in active.

The oscillation stop detection circuit is in active to set “1” to the ceramic or RC oscillation stop detection function active bit. When the oscillation stop detection circuit is in active, ceramic or RC oscillation is watched by the on-chip oscillator. When stop of ceramic or RC oscillation is detected, the oscillation stop detection status bit is set to “1”. While “1” is set to the oscillation stop reset bit, internal reset occurs when oscillation stop is detected.

The external reset and the oscillation stop reset can be discriminated by reading the oscillation stop detection status bit.
The oscillation stop detection status bit retains “1”, not initialized, when the oscillation stop reset occurs. The oscillation stop detection status bit is initialized to “0” when the external reset occurs. Accordingly, reset by oscillation stop can be confirmed by using this flag.

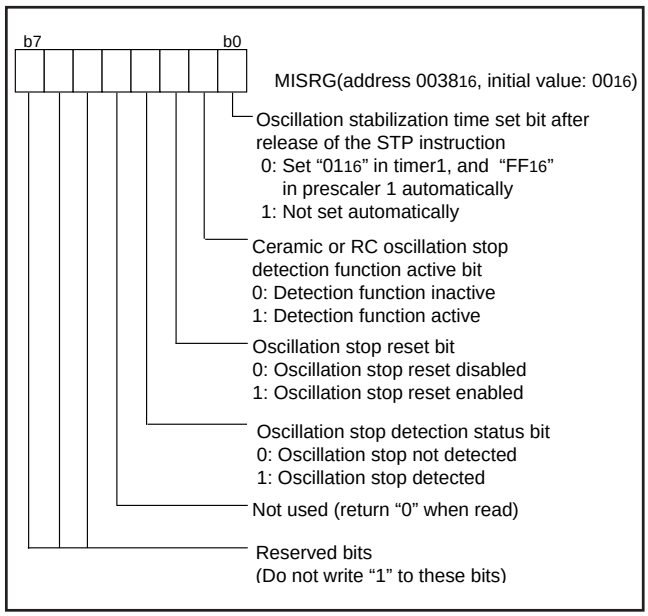


Fig. 79 Structure of MISRG

■ Notes on Oscillation Stop Detection Circuit

- Do not execute the transition to “state 2’a” shown in Fig. 80 because in this “state 2’a”, MCU is stopped without reset even when XIN oscillation is stopped.
- Ceramic or RC oscillation stop detection function active bit is not cleared by the oscillation stop internal reset. Accordingly, the oscillation stop detection circuit is in active when system is released from internal reset cause of oscillation stop detection.
- Oscillation stop detection status bit is initialized by the following operation.
  (1) External reset
  (2) Write “0” data to the ceramic or RC oscillation stop detection function active bit.
- The oscillation stop detection circuit is not included in the emulator MCU “M37542RSS”.

4. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

<Reason>

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

<Reason>

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

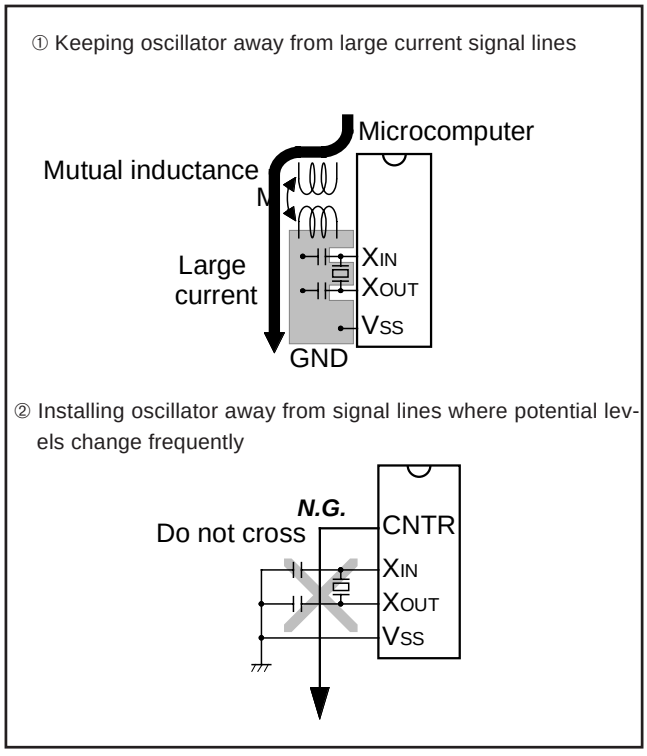


Fig. 94 Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.

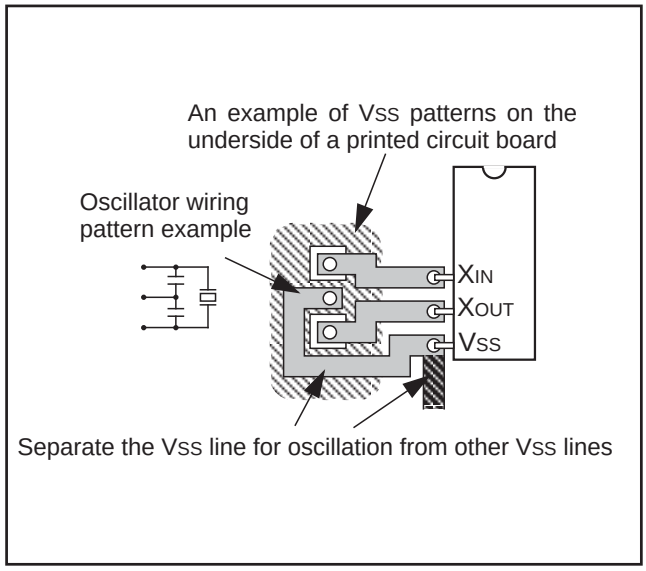


Fig. 95 Vss pattern on the underside of an oscillator

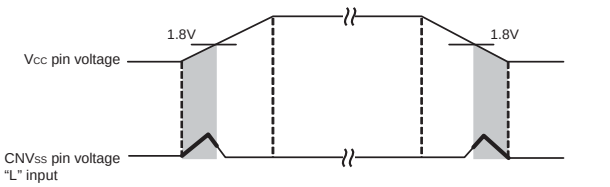
NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage

Make sure that voltage exceeding the V_{CC} pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for CNV_{SS} pin (V_{PP} power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.



(1) Input voltage to other MCU pins rises before V_{CC} pin voltage.
(2) Input voltage to other MCU pins falls after V_{CC} pin voltage.
Note: The internal circuitry is unstable when V_{CC} is below the minimum voltage specification of 1.8V (shaded portion), so particular care should be exercised regarding overvoltage.

Fig. 98 Timing Diagram (bold-lined periods are applicable)

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

A/D Converter Characteristics

A/D Converter characteristics

(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy	Ta = 25 °C VCC = VREF = 2.7 to 5.5 V			± 3	LSB
tCONV	Conversion time	AD conversion clock = f(XIN)/2			122	tc(XIN)
		AD conversion clock = f(XIN)			61	
RLADDER	Ladder resistor			55		kΩ
IVREF	Reference power source input current	VREF = 5.0 V	50	150	200	μA
		VREF = 3.0 V	30	90	120	
II(AD)	A/D port input current				5.0	μA

Note: AD conversion accuracy may be low under the following conditions;

(1) When the VREF voltage is set to be lower than the VCC voltage, an analog circuit in this microcomputer is affected by noise. The accuracy is lower than the case the VREF voltage is the same as VCC voltage.

(2) When the VREF voltage is 3.0 V or less at the low temperature, the AD conversion accuracy may be very lower than at room temperature. When system is used at low temperature, that VREF is 3.0 V or more is recommended.

Timing Requirements

Timing requirements (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR0)}$	CNTR0 input cycle time	200			ns
$t_{WH(CNTR0)}$	CNTR0, INT0, INT1, CAP0, CAP1 input “H” pulse width (Note 1)	80			ns
$t_{WL(CNTR0)}$	CNTR0, INT0, INT1, CAP0, CAP1 input “L” pulse width (Note 1)	80			ns
$t_{C(SCLK1)}$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	800			ns
$t_{WH(SCLK1)}$	Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2)	370			ns
$t_{WL(SCLK1)}$	Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2)	370			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1, serial I/O2 input set up time	220			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1, serial I/O2 input hold time	100			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Timing requirements (2)

(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR0)}$	CNTR0 input cycle time	500			ns
$t_{WH(CNTR0)}$	CNTR0, INT0, INT1, CAP0, CAP1 input “H” pulse width (Note 1)	230			ns
$t_{WL(CNTR0)}$	CNTR0, INT0, INT1, CAP0, CAP1 input “L” pulse width (Note 1)	230			ns
$t_{C(SCLK1)}$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2)	950			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1, serial I/O2 input set up time	400			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1, serial I/O2 input hold time	200			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

NOTES ON PERIPHERAL FUNCTIONS
Notes on I/O Ports

1. Port P0P3 drive capacity control register
The number of LED drive port (drive capacity is HIGH) is 8.

2. Pull-up control register
When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.
<Reason>
Pull-up control is effective only when each direction register is set to the input mode.

3. Notes in stand-by state
In stand-by state*1 for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".
Pull-up (connect the port to Vcc) or pull-down (connect the port to Vss) these ports through a resistor.
When determining a resistance value, note the following points:
- External circuit
- Variation of output levels during the ordinary operation
  When using a built-in pull-up resistor, note on varied current values:
- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external.

<Reason>
The output transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input port and an I/O port are "undefined". This may cause power source current.

*1 stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

4. Modifying output data with bit handling instruction
When the port latch of an I/O port is modified with the bit handling instruction*1, the value of an unspecified bit may change.
<Reason>
I/O ports can be set to input mode or output mode in byte units. When the port register is read or written, the following will be operated:
- Port as input mode
  Read: Read the pin level
  Write: Write to the port latch
- Port as output mode
  Read: Read the port latch or peripheral function output
  (specifications vary depending on the port)
  Write: Write to the port latch
  (output the content of the port latch from the pin)

Meanwhile, the bit handling instructions are the read-modifywrite instructions*2. Executing the bit handling instruction to the port register allows reading and writing a bit unspecified with the instruction at the same time.
If an unspecified bit is set to input mode, the pin level is read and the value is written to the port latch. At this time, if the original content of the port latch and the pin level do not match, the content of the port latch changes.
If an unspecified bit is set to output mode, the port latch is normally read, but the peripheral function output is read in some ports and the value is written to the port latch. At this time, if the original content of the port latch and the peripheral function output do not match, the content of the port latch changes.

*1 Bit handling instructions: CLB, SEB
*2 Read-modify-write instruction: Reads 1-byte of data from memory, modifies the data, and writes 1-byte of the data to the original memory.

5. Direction register
The values of the port direction registers cannot be read.
That is, it is impossible to use the **LDA** instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as **BBC** and **BBS**.
It is also impossible to use bit operation instructions such as **CLB** and **SEB** and read-modify-write instructions of direction registers for calculations such as **ROR**.
For setting direction registers, use the **LDM** instruction, **STA** instruction, etc.

Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

(1) I/O ports

Set the I/O ports for the input mode and connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.

When using the I/O ports as the output mode, open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) I/O ports setting as input mode

[1] Do not open in the input mode.

<Reason>

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) shown on the above "1. Terminate unused pins".

[2] Do not connect to V_{CC} or V_{SS} directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Change of relevant register settings

When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Figure 4.

- When switching external interrupt active edge
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

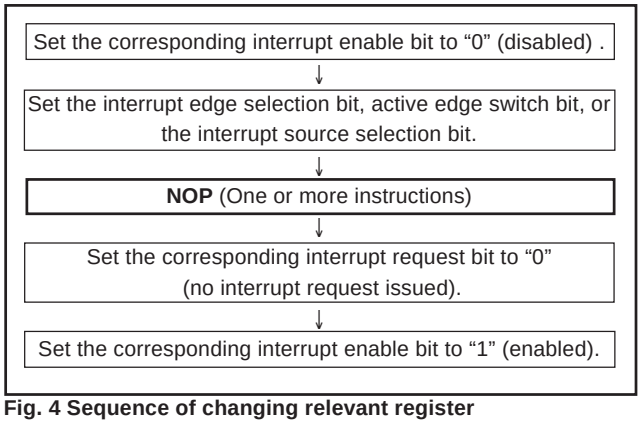


Fig. 4 Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".

- When switching external interrupt active edge
  - INT_0 interrupt edge selection bit
    (bit 0 of Interrupt edge selection register (address $003A_{16}$))
  - INT_1 interrupt edge selection bit
    (bit 1 of Interrupt edge selection register)
  - $CNTR_0$ active edge switch bit
    (bit 2 of timer X mode register (address $002B_{16}$))
  - Capture 0 interrupt edge selection bit
    (bits 1 and 0 of capture mode register (address 0020_{16}))
  - Capture 1 interrupt edge selection bit
    (bits 3 and 2 of capture mode register)

2. Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to determine an interrupt request bit immediately after this bit is set to "0", take the following sequence.

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

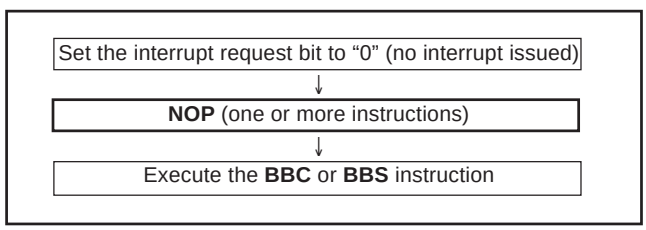


Fig. 5 Sequence of check of interrupt request bit