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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	8MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	29
Program Memory Size	8KB (8K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-SOP (0.330", 8.40mm Width)
Supplier Device Package	36-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m37547g2fp-w4

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 5.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

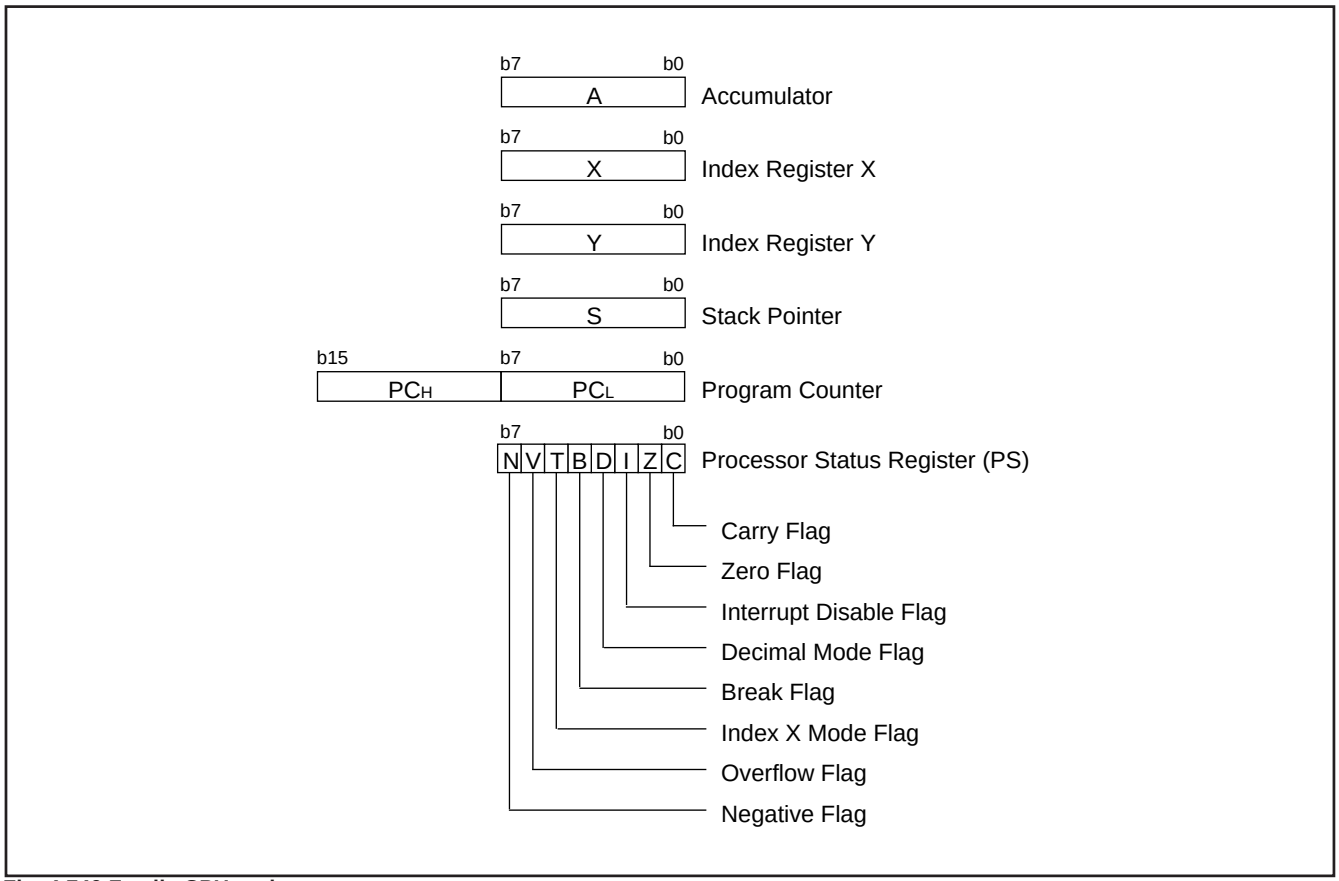


Fig. 4 740 Family CPU register structure

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Code Protect Address (address $FFDB_{16}$)

Address $FFDB_{16}$, which is the reserved ROM area of QzROM, is the ROM code protect address. "00_{16}" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00_{16}" or "FF_{16}" can be selected as the ROM option setup (referred to as "Mask option setup" in MM) when ordering.

■ **Notes**

Because the contents of RAM are indefinite at reset, set initial values before using.

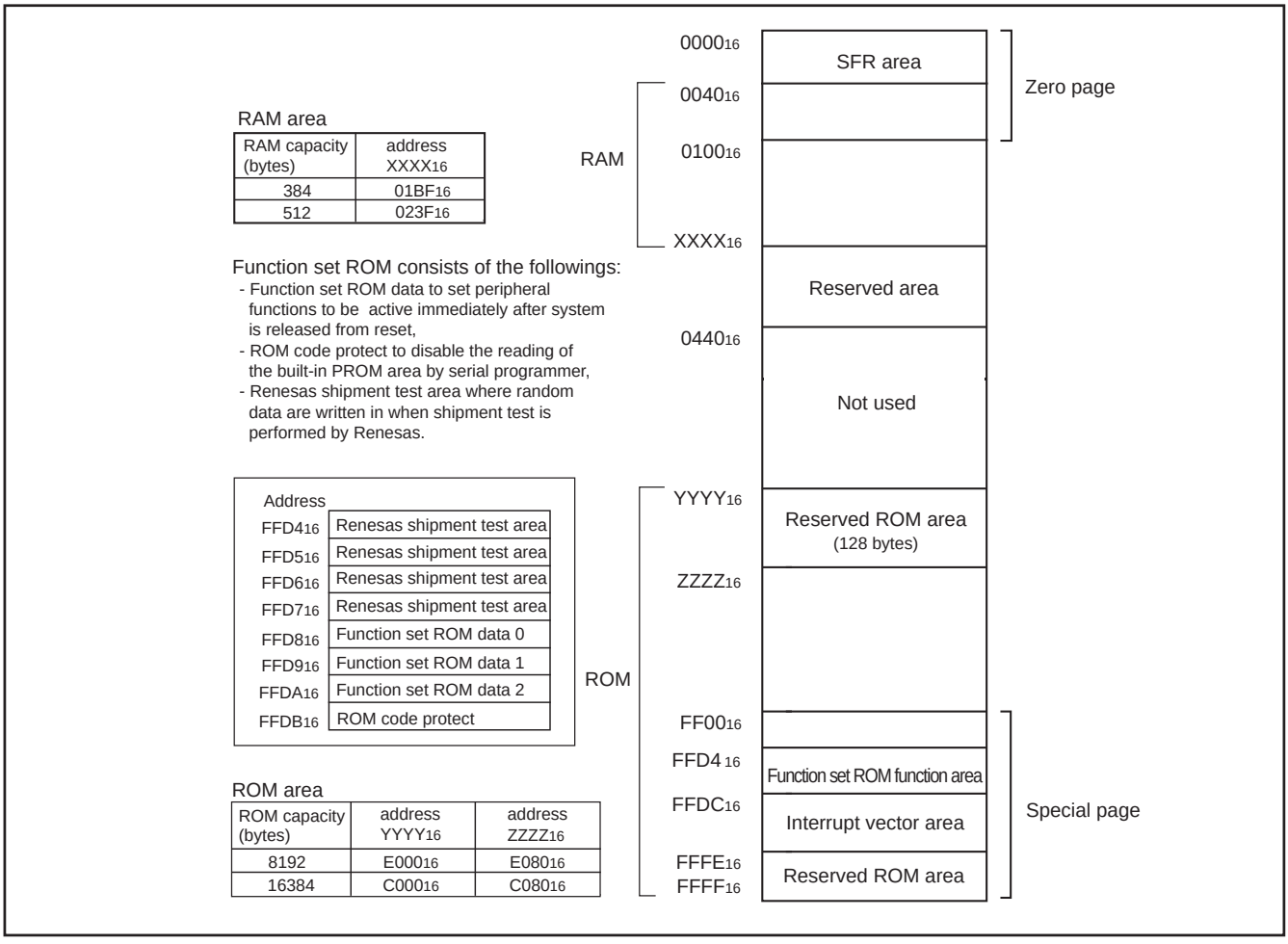


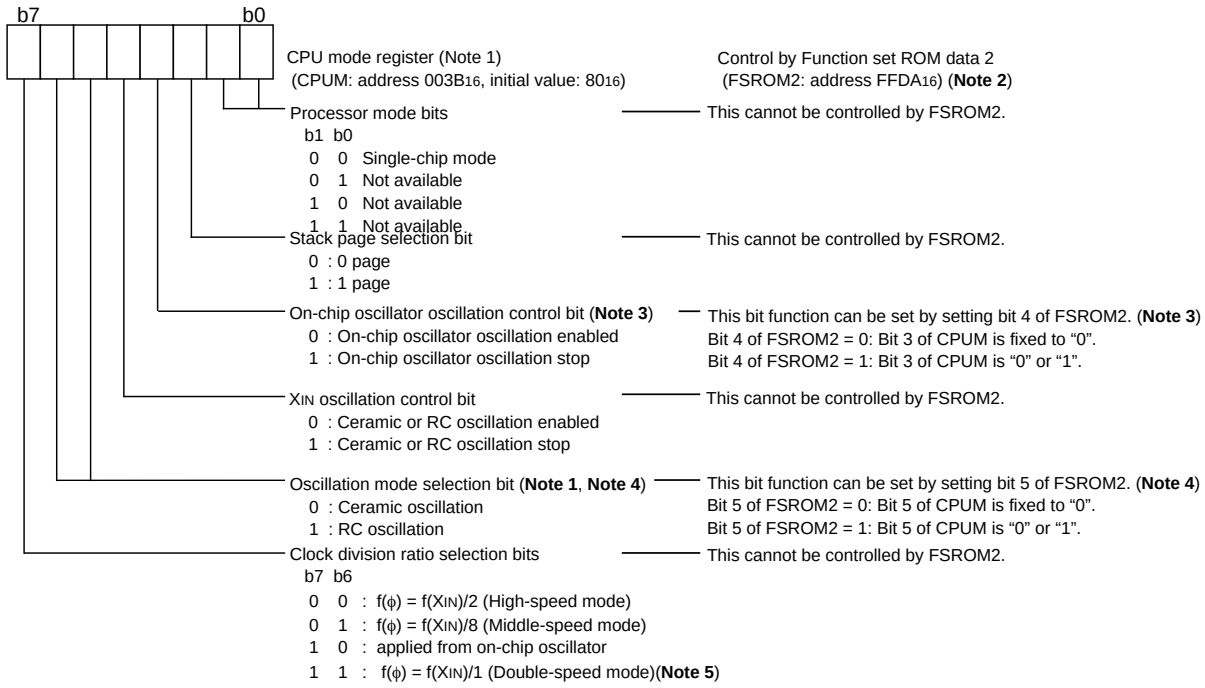
Fig. 6 Memory map diagram

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit, etc..
This register is allocated at address 003B16.
Some function of the CPU mode register can be controlled by the function set ROM data 2.

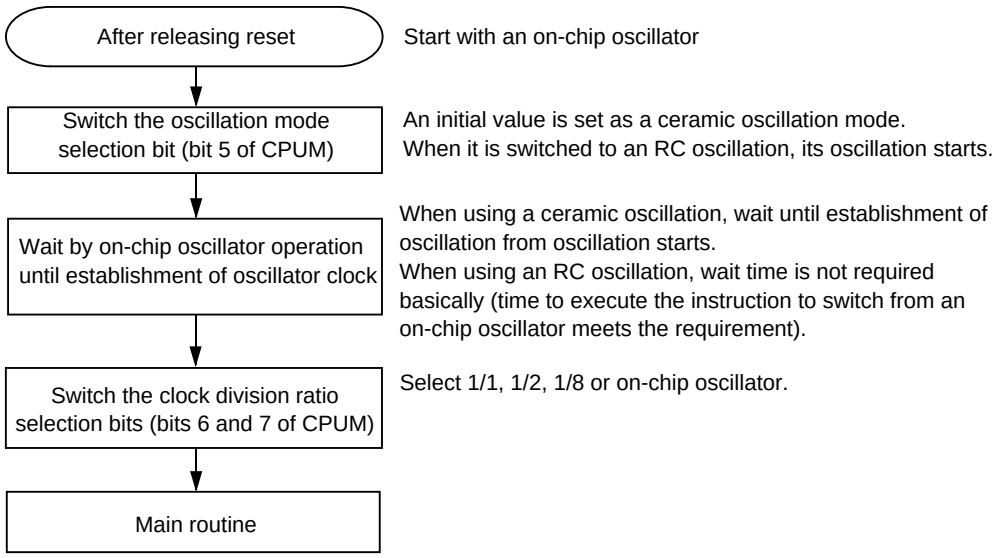
Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.



Note 1: When the setting by the function set ROM data 2 (FSROM2) is performed, the initial value of CPUM is changed after releasing reset since bit 5 of CPUM is fixed.
2: The setting values of FSROM2 become valid by setting "0" to bit 0 of function set ROM data 0 (FSROM0). The setting values of FSROM2 are invalid by setting "1" to this bit. (In order that FSROM2 is invalid, write to CPUM after releasing reset.)
3: When bit 4 of FSROM2 is set to "0", the operation of on-chip oscillator cannot be stopped. Since the on-chip oscillator is not stopped also in the stop mode, the dissipation current in the stop mode is increased.
4: The setting value of bit 5 of CPUM can be fixed after releasing reset by setting value of bit 5 of FSROM2. Also, when the setting of FSROM2 is invalid, this bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit. This bit is initialized by reset, and then, rewriting it is enabled.
5: This setting can be used only at ceramic oscillation. Do not use this at RC oscillation.

Fig. 7 Structure of CPU mode register



Note: After system is released from reset, an on-chip oscillator turns active automatically and system operation is started.

Fig. 8 Switching method of CPU mode register

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.

Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).

We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.

Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2	Termination 3	Termination 4
P0$_0$/CAP$_0$	I/O port	When selecting CAP function, perform termination of input port.	-	When selecting key-on wakeup function, perform termination of input port.
P0$_1$/CMP$_0$		When selecting CMP$_0$ function, perform termination of output port.	-	
P0$_2$/CMP$_1$		When selecting CMP$_1$ function, perform termination of output port.	-	
P0$_3$/TX$_{OUT}$		When selecting TX$_{OUT}$ function, perform termination of output port.	-	
P0$_4$/RxD$_2$		When selecting RxD$_2$ function, perform termination of input port.	-	
P0$_5$/TxD$_2$		When selecting TxD$_2$ function, perform termination of output port.	-	
P0$_6$/SCLK$_2$		When selecting external clock input, perform termination of output port.	When selecting internal clock output, perform termination of output port.	
P0$_7$/$\overline{\text{SRDY}_2}$		When selecting $\overline{\text{SRDY}_2}$ function, perform termination of output port.	-	
P1$_0$/RxD$_1$/CAP$_0$		When selecting RxD$_1$ function, perform termination of input port.	When selecting CAP function, perform termination of input port.	-
P1$_1$/TxD$_1$		When selecting TxD$_1$ function, perform termination of output port.	-	-
P1$_2$/SCLK$_1$		When selecting external clock input, perform termination of input port.	When selecting internal clock output, perform termination of output port.	-
P1$_3$/$\overline{\text{SRDY}_1}$		When selecting $\overline{\text{SRDY}_1}$ function, perform termination of output port.	-	-
P1$_4$/CNTR$_0$		When selecting CNTR input function, perform termination of input port.	When selecting CNTR output function, perform termination of output port.	-
P2$_0$/AN$_0$–P2$_7$/AN$_7$		When selecting AN function, perform termination of input port.	-	-
P3$_0$/CAP$_1$		When selecting CAP function, perform termination of input port.	-	-
P3$_1$/CMP$_2$		When selecting CMP$_2$ function, perform termination of output port.	-	-
P3$_2$/CMP$_3$		When selecting CMP$_3$ function, perform termination of output port.	-	-
P3$_3$/INT$_1$		When selecting INT function, perform termination of input port.	-	-
P3$_4$		-	-	-
P3$_5$		-	-	-
P3$_6$/INT$_1$		When selecting INT function, perform termination of input port.	-	-
P3$_7$/INT$_0$		When selecting INT function, perform termination of input port.	-	-
V$_{REF}$	Connect to Vss.	-	-	-
X$_{IN}$	When only on-chip oscillator is used, connect to V$_{CC}$ through a registor.	-	-	-
X$_{OUT}$	When external clock is input or when only on-chip oscillator is used, open.	-	-	-

Interrupts

The 7547 Group interrupts are vector interrupts with a fixed priority scheme, and generated by 16 sources among 18 sources: 6 external, 11 internal, and 1 software.
The interrupt sources, vector addresses(1) , and interrupt priority are shown in Table 8.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Fig. 16 shows an interrupt control diagram.

An interrupt request is accepted when all of the following conditions are satisfied:

- Interrupt disable flag.....“0”
- Interrupt request bit.....“1”
- Interrupt enable bit.....“1”

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 8 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	FFFD16	FFFC16	At reset input	Non-maskable
Serial I/O1 receive	2	FFFB16	FFFA16	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	3	FFF916	FFF816	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2 receive	4	FFF716	FFF616	At completion of serial I/O2 data receive	Valid only when serial I/O2 is selected
Serial I/O2 transmit	5	FFF516	FFF416	At completion of serial I/O2 transmit shift or when transmit buffer is empty	Valid only when serial I/O2 is selected
INT_0	6	FFF316	FFF216	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	7	FFF116	FFF016	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Key-on wake-up/ UART1 bus collision detection (Note 3)	8	FFEF16	FFEE16	At falling of conjunction of input logical level for port P0 (at input) At detection of UART1 bus collision detection	External interrupt (valid at falling) When UART1 bus collision detection interrupt is enabled.
$CNTR_0$	9	FFED16	FFEC16	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
Capture 0	10	FFEB16	FFEA16	At detection of either rising or falling edge of Capture 0 input	External interrupt (active edge selectable)
Capture 1	11	FFE916	FFE816	At detection of either rising or falling edge of Capture 1 input	External interrupt (active edge selectable)
Compare	12	FFE716	FFE616	At compare matched	Compare interrupt source is selected.
Timer X	13	FFE516	FFE416	At timer X underflow	
Timer A	14	FFE316	FFE216	At timer A underflow	
Timer B	15	FFE116	FFE016	At timer B underflow	
A/D conversion/ Timer 1 (Note 4)	16	FFDF16	FFDE16	At completion of A/D conversion At timer 1 underflow	STP release timer underflow
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.
3: Key-on wakeup interrupt and UART1 bus collision detection interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.
4: A/D conversion interrupt and Timer 1 interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to “1”.

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of the interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Fig. 18 shows the time up to execution in the interrupt processing routine, and Fig. 19 shows the interrupt sequence.
Fig. 20 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.
(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1.High-order bits of program counter (PCH)
2.Low-order bits of program counter (PCL)
3.Processor status register (PS)
(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.
(4) The interrupt request bit for the corresponding interrupt is set to “0”. Also, the interrupt disable flag is set to “1” and multiple interrupts are disabled.
(5) The interrupt routine is executed.
(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

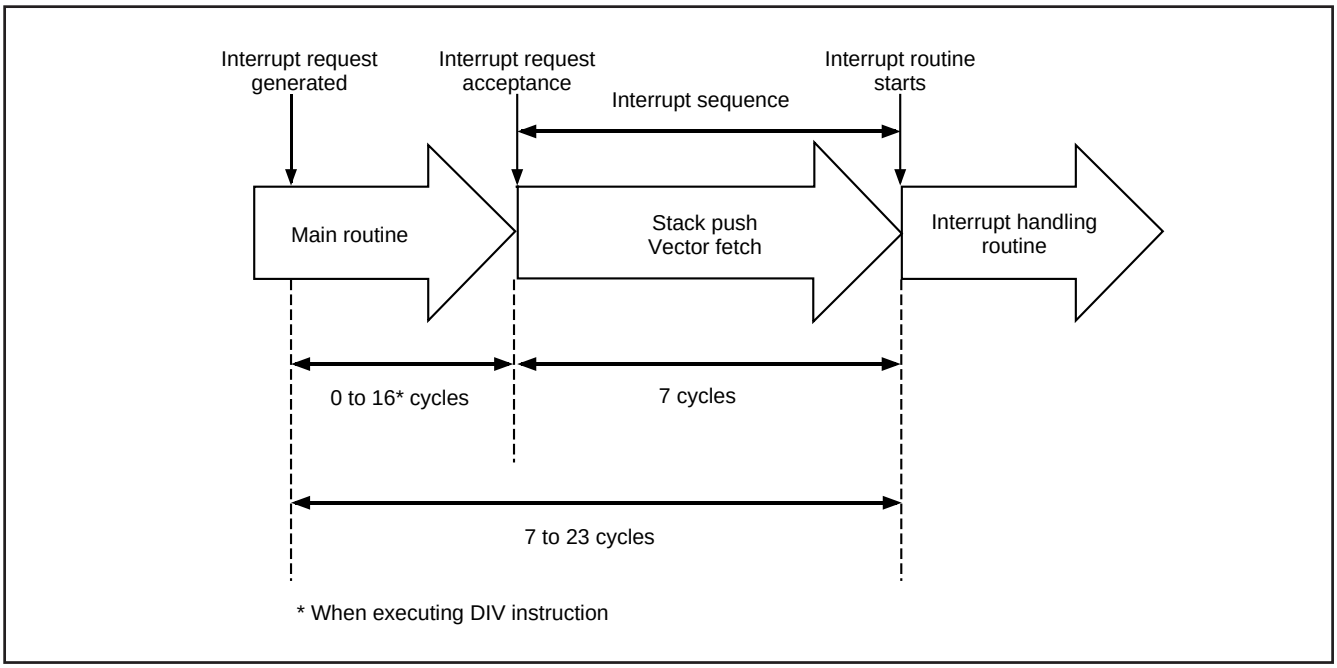


Fig. 18 Time up to execution in interrupt routine

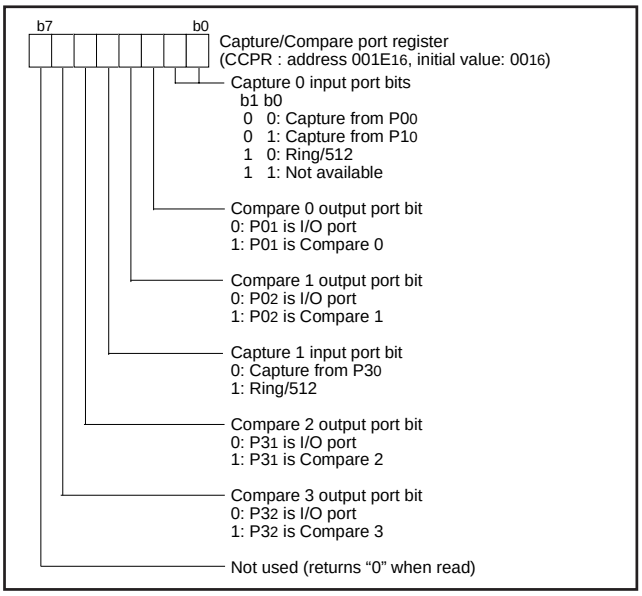


Fig. 30 Structure of capture/compare port register

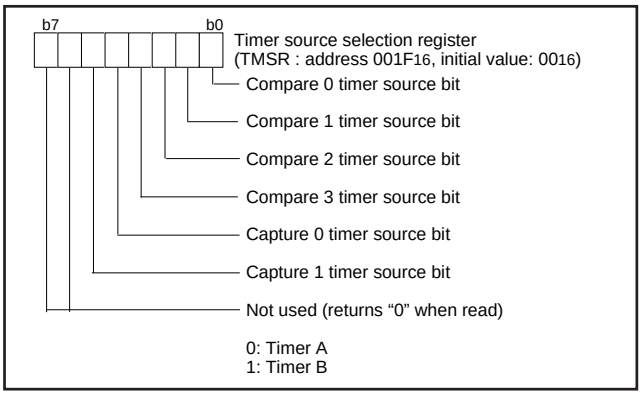


Fig. 31 Structure of timer source selection register

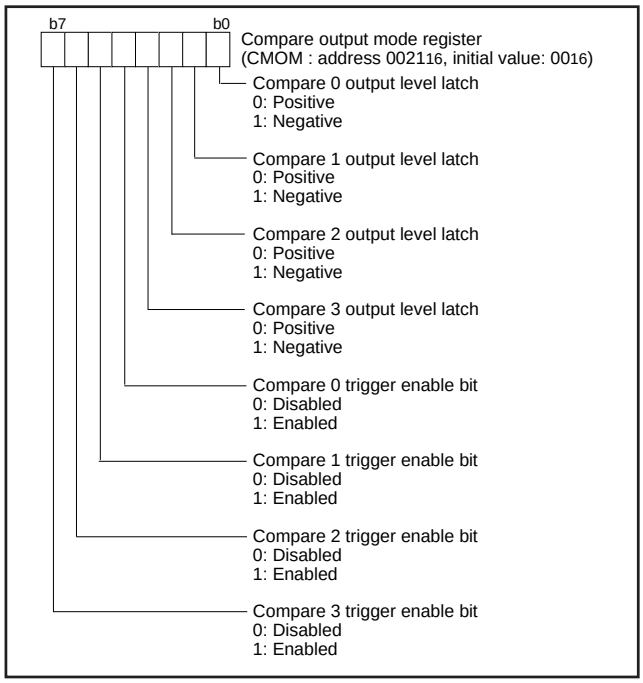


Fig. 32 Structure of compare output mode register

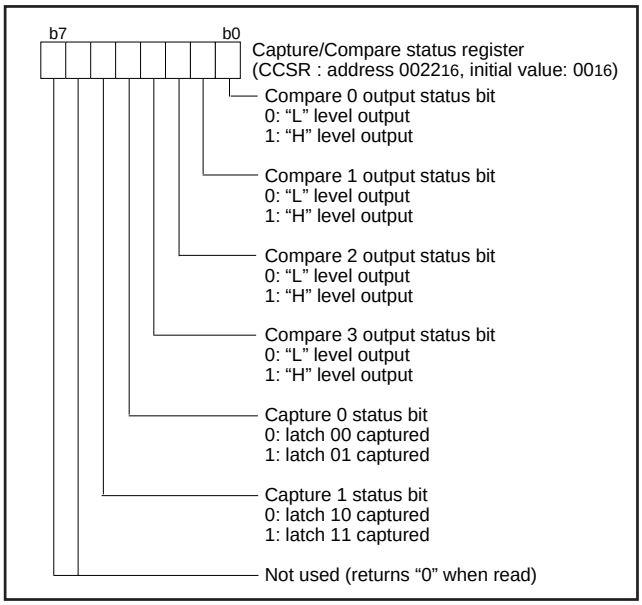


Fig. 33 Structure of capture/compare status register

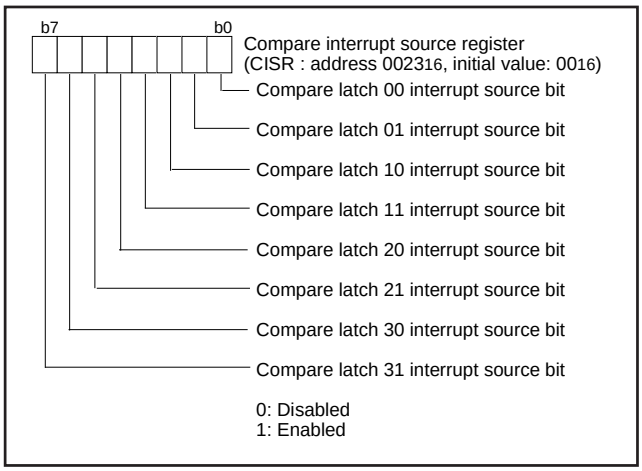


Fig. 34 Structure of compare interrupt source register

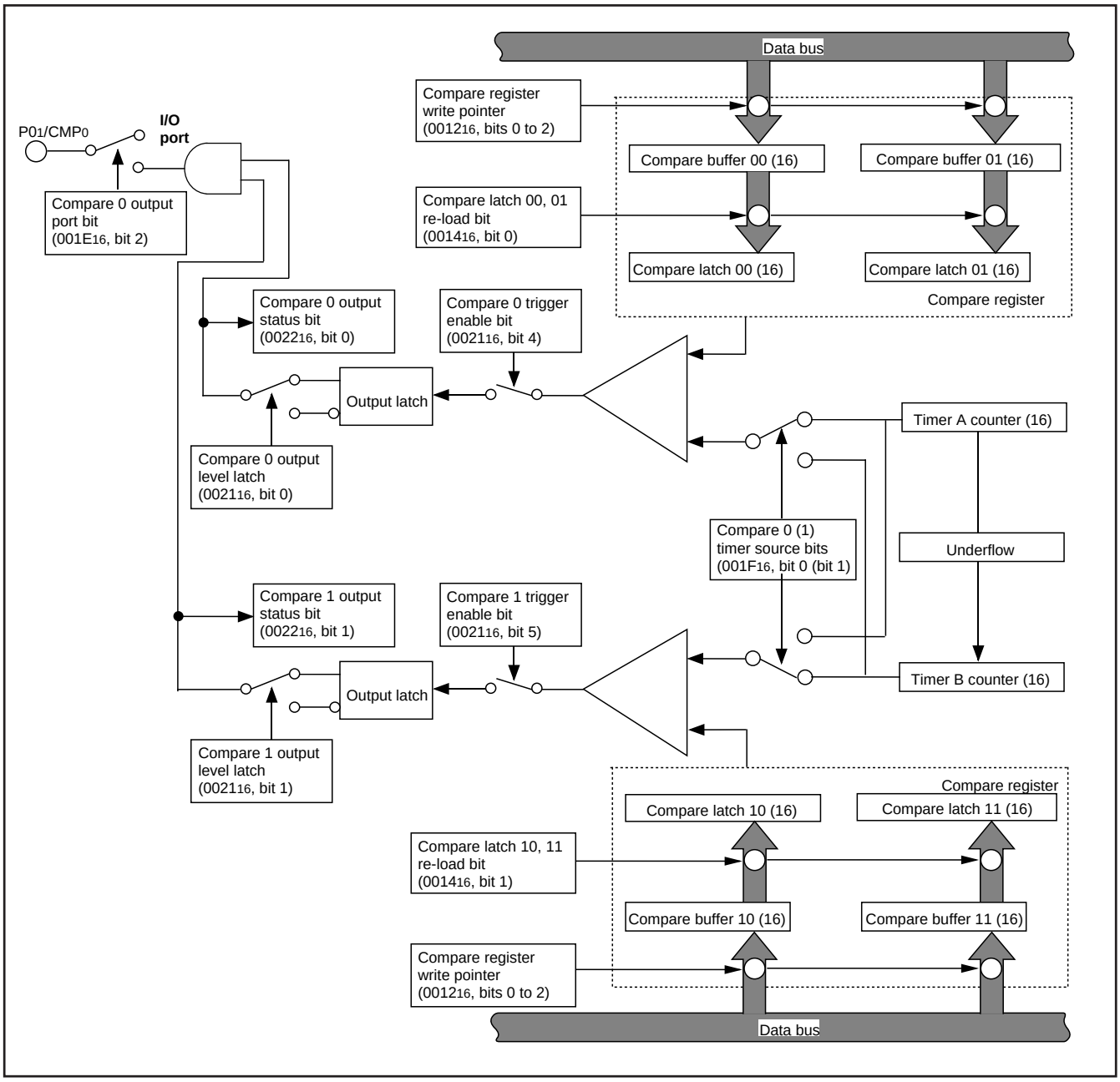


Fig. 37 Block diagram at modulation mode

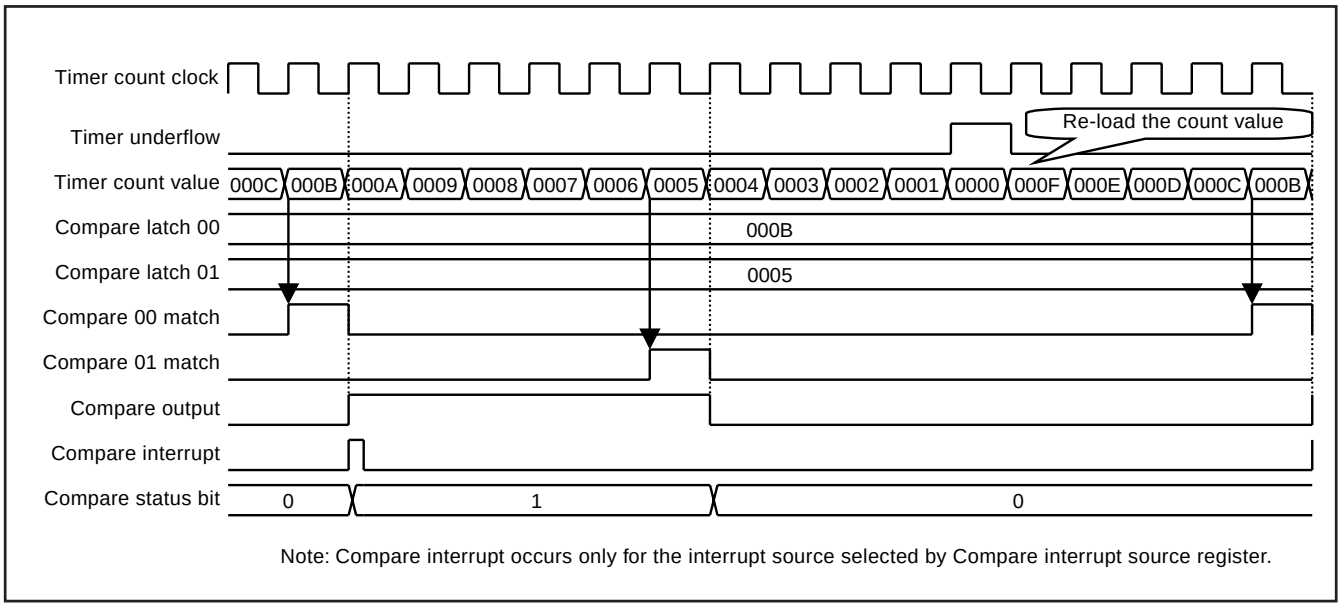


Fig. 38 Output compare mode (general waveform)

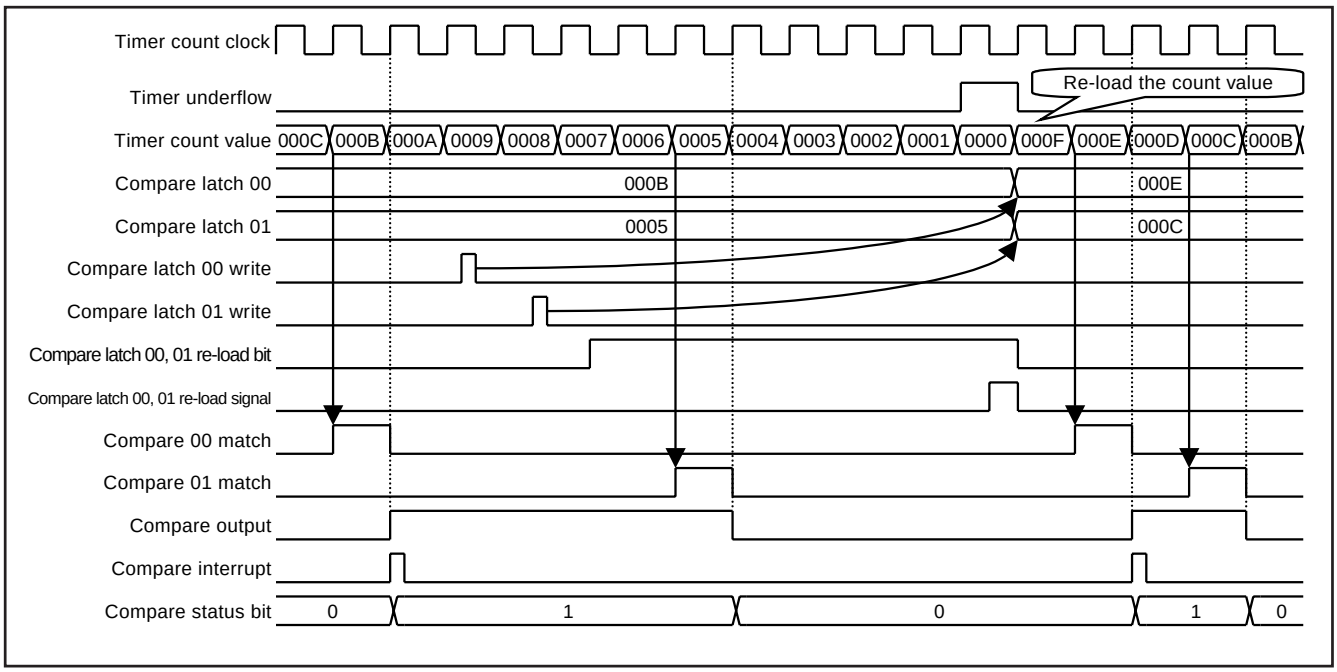


Fig. 39 Output compare mode (compare register write timing)

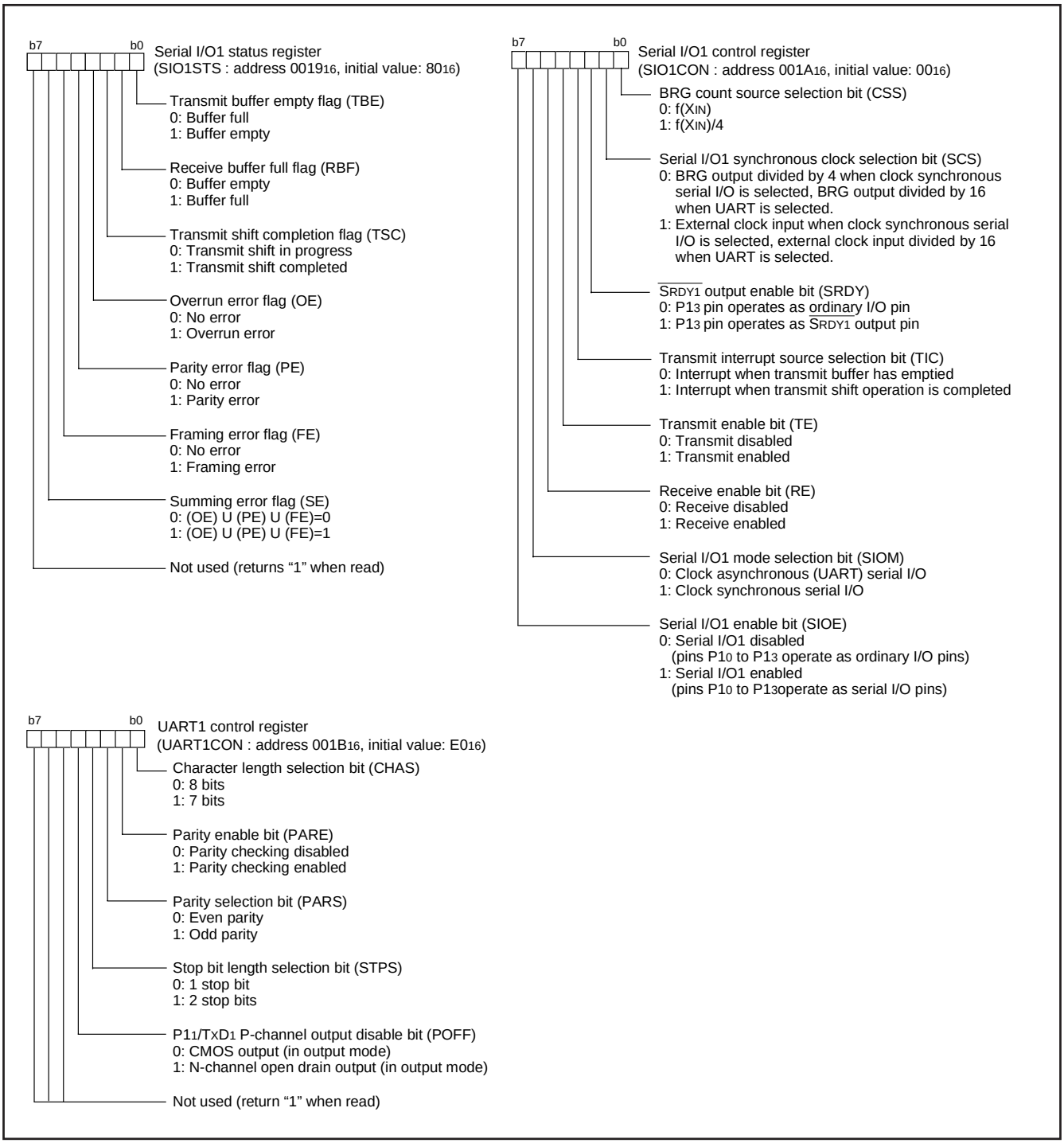


Fig. 52 Structure of serial I/O1-related registers

(2) Asynchronous Serial I/O2 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O2 mode selection bit of the serial I/O2 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

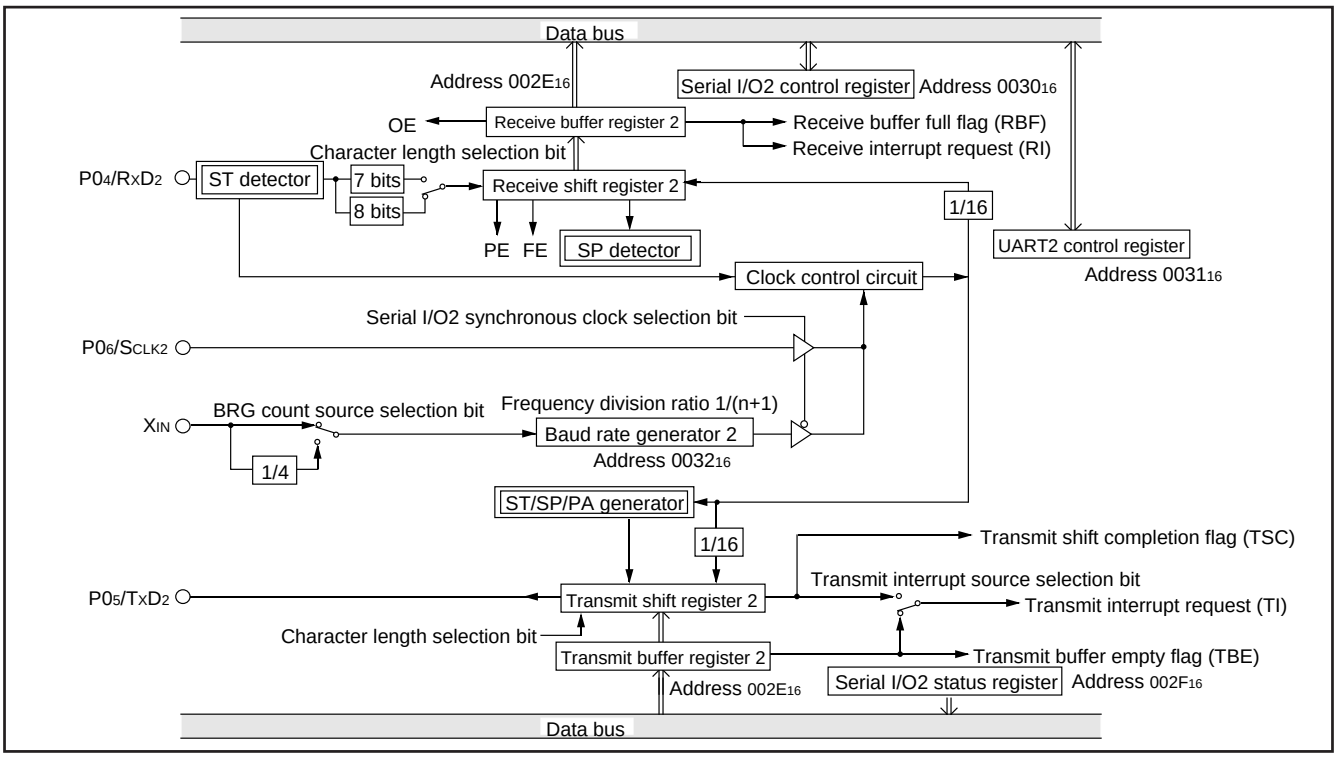
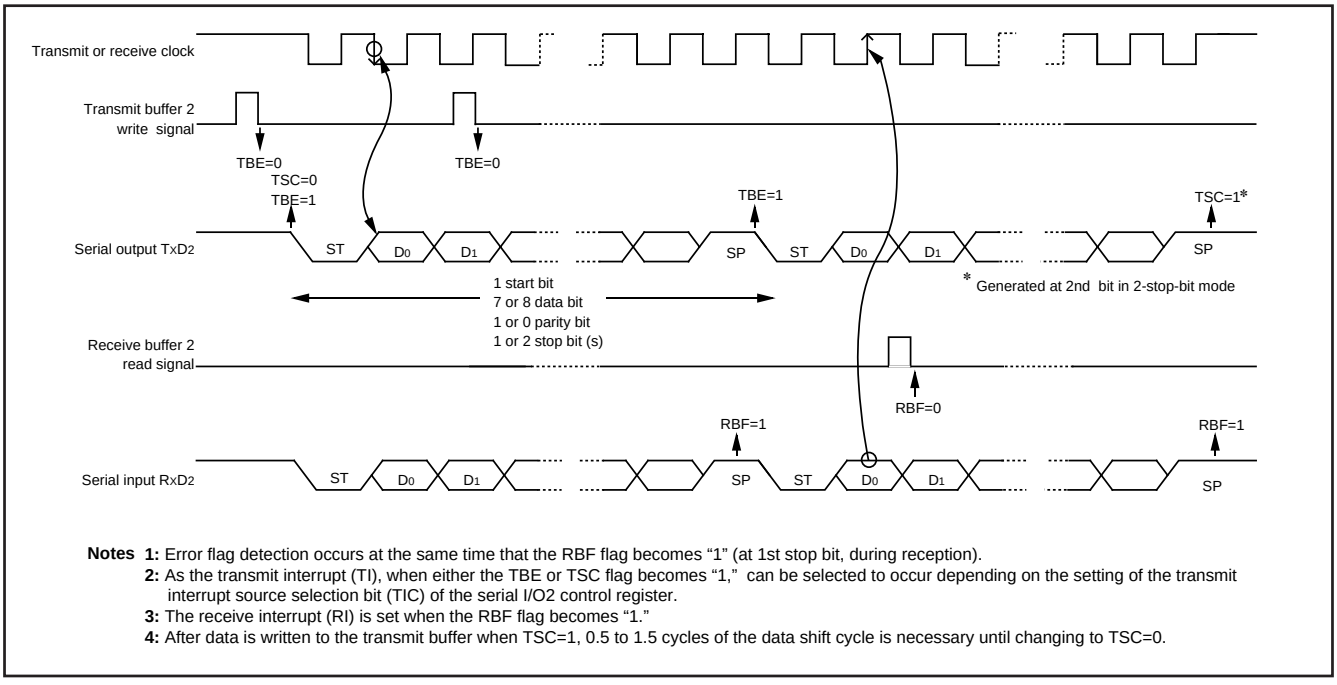


Fig. 58 Block diagram of UART serial I/O2



Notes
1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O2 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 59 Operation of UART serial I/O2 function

[Transmit buffer register 2/receive buffer register 2 (TB2/RB2)] 002E16

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O2 status register (SIO2STS)] 002F16

The read-only serial I/O2 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O2 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O2 enable bit SIOE (bit 7 of the serial I/O2 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O2 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O2 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O2 control register (SIO2CON)] 003016

The serial I/O2 control register consists of eight control bits for the serial I/O2 function.

[UART2 control register (UART2CON)] 003116

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer.

[Baud rate generator 2 (BRG2)] 003216

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes on Serial I/O2

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
② Set the transmit enable bit to "1".
③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O2 synchronous clock selection bit
"0" : P06 pin turns into an output pin of a synchronous clock.
"1" : P06 pin turns into an input pin of a synchronous clock.
Setup of a $\overline{\text{SRDY2}}$ output enable bit (SRDY)
"0" : P07 pin can be used as a normal I/O pin.
"1" : P07 pin turns into a $\overline{\text{SRDY2}}$ output pin.

(2) Serial I/O2 mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O2 synchronous clock selection bit
"0": P06 pin can be used as a normal I/O pin.
"1": P06 pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

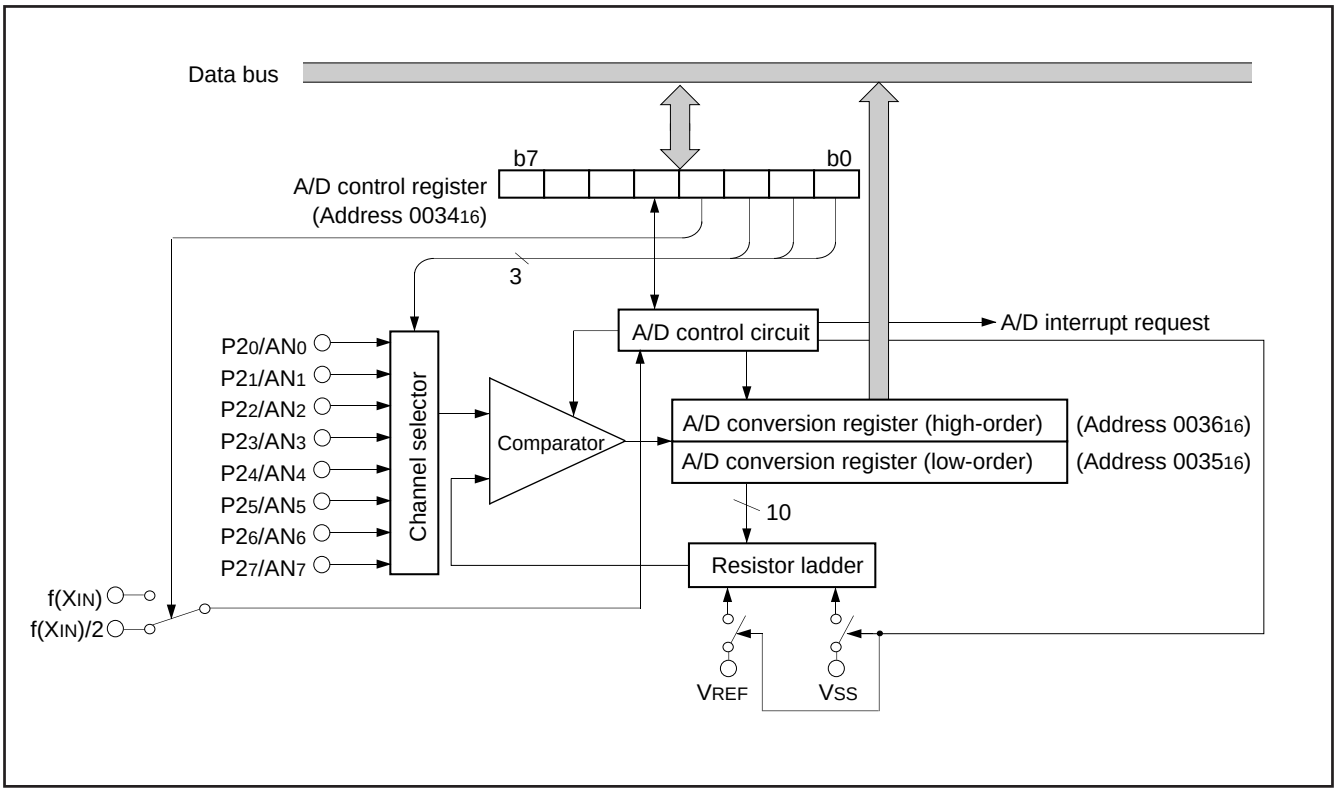


Fig. 63 Block diagram of A/D converter

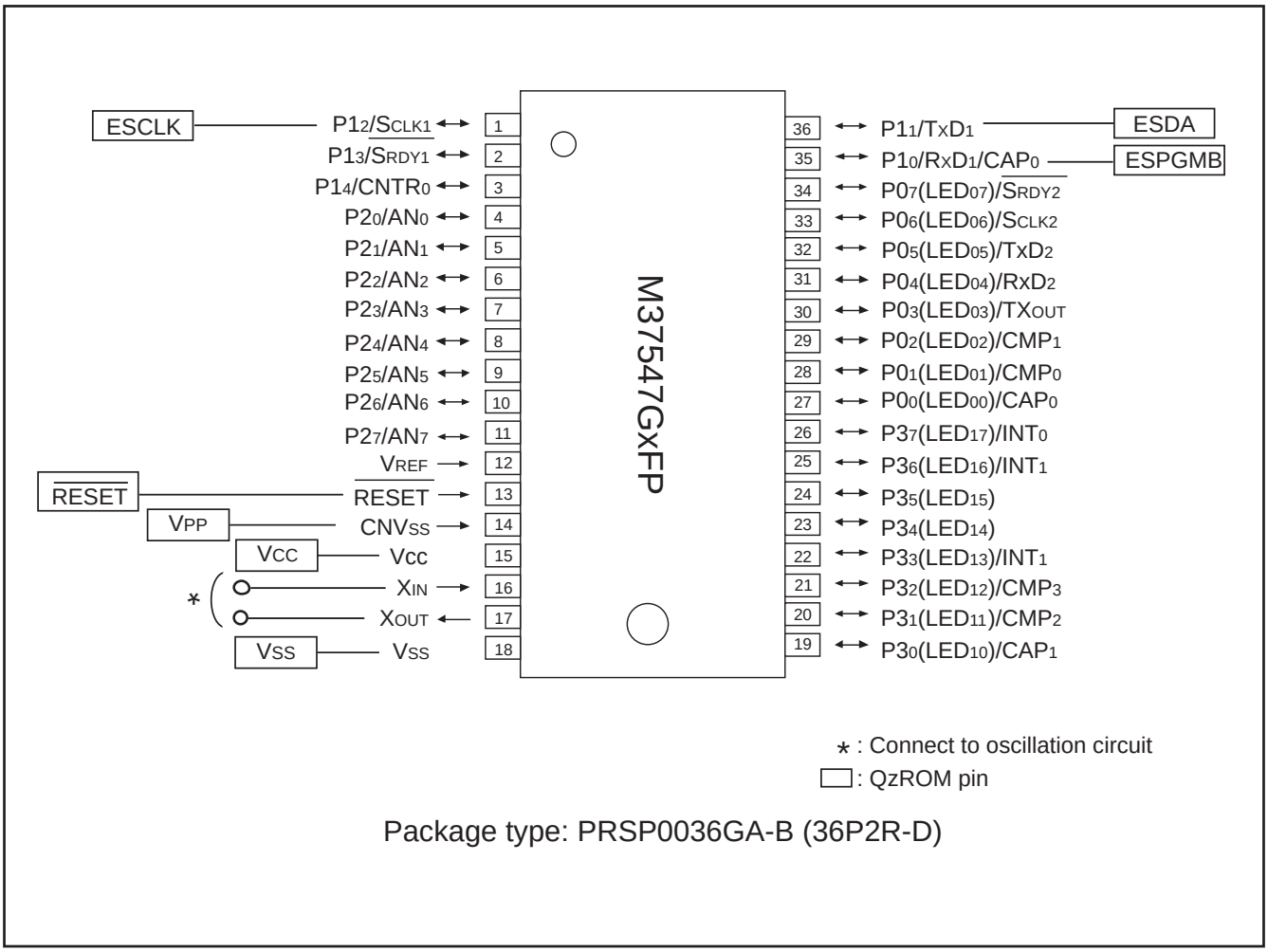


Fig. 85 Pin connection diagram (M37547GxFP)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is “1”. After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations. Initialize these flags at beginning of the program.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

• For calculations in decimal notation, set the decimal mode flag D to “1”, then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.

• In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

• The values of the port direction registers cannot be read.

That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is “1”, addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.

It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.

For setting direction registers, use the LDM instruction, STA instruction, etc.

A/D Conversion

Do not execute the STP instruction during A/D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)

When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

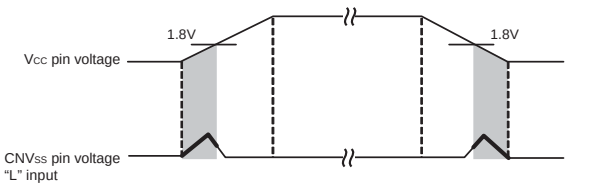
NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage

Make sure that voltage exceeding the V_{CC} pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for CNV_{SS} pin (V_{PP} power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.



(1) Input voltage to other MCU pins rises before V_{CC} pin voltage.
(2) Input voltage to other MCU pins falls after V_{CC} pin voltage.
Note: The internal circuitry is unstable when V_{CC} is below the minimum voltage specification of 1.8V (shaded portion), so particular care should be exercised regarding overvoltage.

Fig. 98 Timing Diagram (bold-lined periods are applicable)

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

Electrical characteristics (2)

(Vcc = 1.8 to 5.5V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
ICC	Power source current *LVD is valid (except at STP)	f(XIN) = 8 MHz Output transistors “off”	Double-speed mode		5.9	9.5	mA
			High-speed mode		3.9	7.0	mA
			Middle-speed mode		2.4	5.5	mA
		f(XIN) = 2 MHz, VCC = 2.2 V Output transistors “off”	High-speed mode		0.45	1.25	mA
		On-chip oscillator operation mode, Output transistors “off”	Frequency/1		1.55	3.3	mA
			Frequency/2		0.95	2.3	mA
			Frequency/8		0.4	1.1	mA
			Frequency/128		0.25	0.7	mA
		f(XIN) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors “off”			2.0	3.5	mA
		f(XIN) = 2 MHz, VCC = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.25		mA
		On-chip oscillator operation mode, (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.25	0.7	mA
		Increment when A/D conversion is executed f(XIN) = 8 MHz, VCC = 5 V			0.5		mA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	μA
			Ta = 85 °C			10	μA
		Low voltage detection circuit self consumption current	Ta = 25 °C VCC = 5 V		70		μA

Note: Increment when A/D conversion is executed includes the reference power source input current (IVREF).

Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

(1) I/O ports

Set the I/O ports for the input mode and connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.

When using the I/O ports as the output mode, open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) I/O ports setting as input mode

[1] Do not open in the input mode.

<Reason>

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) shown on the above "1. Terminate unused pins".

[2] Do not connect to V_{CC} or V_{SS} directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Change of relevant register settings

When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Figure 4.

- When switching external interrupt active edge
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

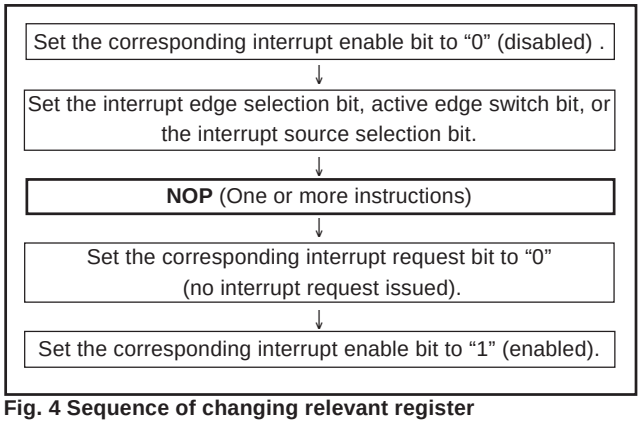


Fig. 4 Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".

- When switching external interrupt active edge
  - INT_0 interrupt edge selection bit
    (bit 0 of Interrupt edge selection register (address $003A_{16}$))
  - INT_1 interrupt edge selection bit
    (bit 1 of Interrupt edge selection register)
  - $CNTR_0$ active edge switch bit
    (bit 2 of timer X mode register (address $002B_{16}$))
  - Capture 0 interrupt edge selection bit
    (bits 1 and 0 of capture mode register (address 0020_{16}))
  - Capture 1 interrupt edge selection bit
    (bits 3 and 2 of capture mode register)

2. Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to determine an interrupt request bit immediately after this bit is set to "0", take the following sequence.

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

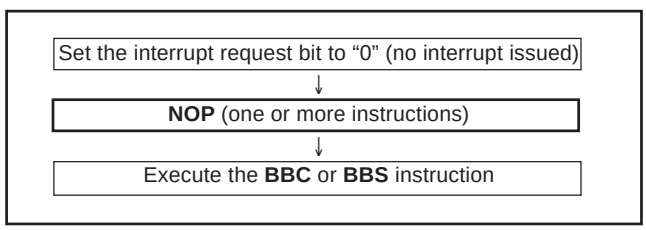


Fig. 5 Sequence of check of interrupt request bit

Notes on Oscillation Stop Detection Circuit

1. After the reset by the oscillation stop detection, the value of following bits are retained, not initialized.
- Ceramic or RC oscillation stop detection function active bit
  Bit 1 of MISRG (address $003B_{16}$)
- Oscillation stop detection status bit
  Bit 3 of MISRG

2. Oscillation stop detection status bit is initialized (“0”) by the following operation.
- External reset
- Write “0” data to the ceramic or RC oscillation stop detection function active bit.

3. The oscillation stop detection circuit is not included in the emulator MCU “M37542RSS”.

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

NOTES ON HARDWARE

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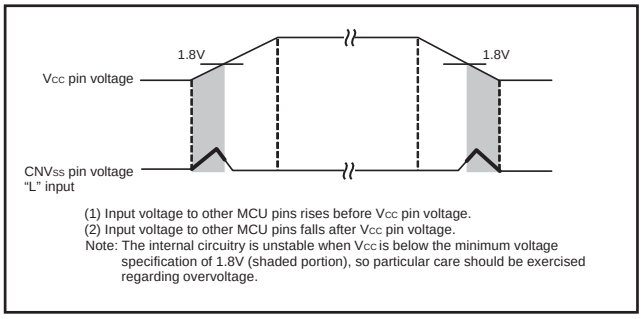

Fig. 7 Timing Diagram (bold-lined periods are applicable)

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