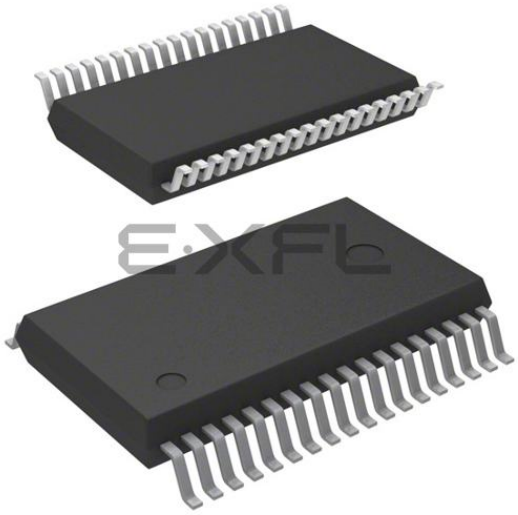

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Details	
Product Status	Obsolete
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Core Size	8-Bit
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Connectivity	SIO, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-SOP (0.330", 8.40mm Width)
Supplier Device Package	36-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m37547g4fp-u0

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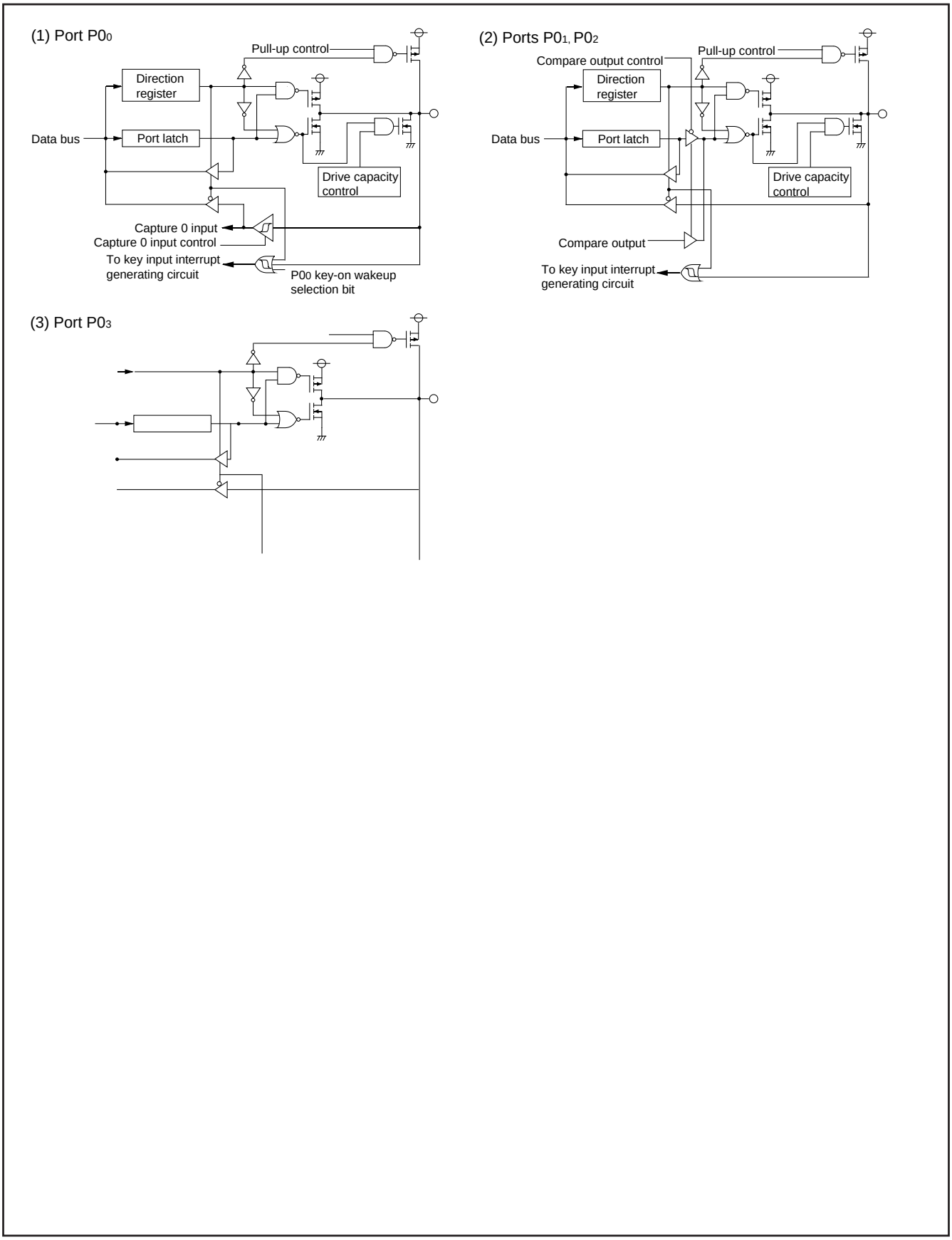

Fig. 13 Block diagram of ports (1)

Output compare

7547 group has 4-output compare channels. Each channel (0 to 3) has the same function and can be used to output waveform by using count value of either Timer A or Timer B.
The source timer for each channel is selected by setting value of the compare x (x = 0, 1, 2, 3) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each compare channel, set “1” to the compare x output port bit and set the port direction register corresponding to compare channel to output mode.

The compare value for each channel is set to the compare register (low-order) and compare register (high-order).
Writing to the register for each channel is controlled by setting value of compare register write pointer. Writing to each register is in the following order;

1. Set the value of corresponded output compare channel to the compare register write pointer.
2. Write a value to the compare register (low-order) and compare register (high-order).
3. Set “1” to the compare latch y (y = 00, 01, 10, 11, 20, 21, 30, 31) re-load bit.
   When “1” is set to the compare latch y re-load bit, the value set to the compare register is loaded to compare latch when the next timer underflow.

When count value of timer and setting value of compare latch is matched, compare output trigger occurs.
When “1: Enabled” is set to the compare trigger x enable bit, the output waveform from port is inverted by compare trigger.
When “0: Disabled” is set to the compare trigger x enable bit, the output waveform is not inverted, so port output can be fixed to “H” or “L”.

When “0: Positive” is set to the compare x output level latch, the compare output waveform is turned to “H level” at compare latch x0’s match and turned to “L level” at compare latch x1’s match.
When “1 :Negative” is set to the compare x output level latch, the compare output waveform is turned to “L level” at compare latch x0’s match and turned to “H level” at compare latch x1’s match.
The compare output level of each channel can be confirmed by reading the compare x output status bit.

Compare output interrupt is available when match of each compare channel and timer count value. The interrupt request from each channel can be disabled or enabled by setting value of compare latch y interrupt source bit.

Compare 0,1 (2,3) modulation mode

In compare modulation mode, modulation waveform can be generated by using compare channel 0 and 1, or compare channel 2 and 3.
To use this mode,

- Set “1: Enabled” to the compare 0,1 (2, 3) modulation mode bit.
- Set Timer A underflow for Timer B count source.
- Set Timer A for the timer source of compare channel 0 (2).
- Set Timer B for the timer source of compare channel 1 (3).

In this mode, AND waveform of compare 0 (1) and compare 2 (3) is generated from Port $P0_1$ and $P3_1$, respectively. Accordingly, in order to use this mode, set “1” to the compare 0 output port bit or compare 2 output port bit.

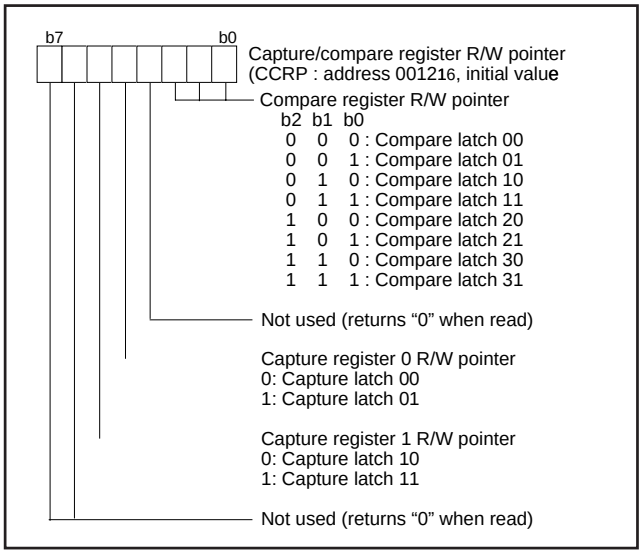

Fig. 28 Structure of capture/compare register R/W pointer

Fig. 29 Structure of compare register re-load register

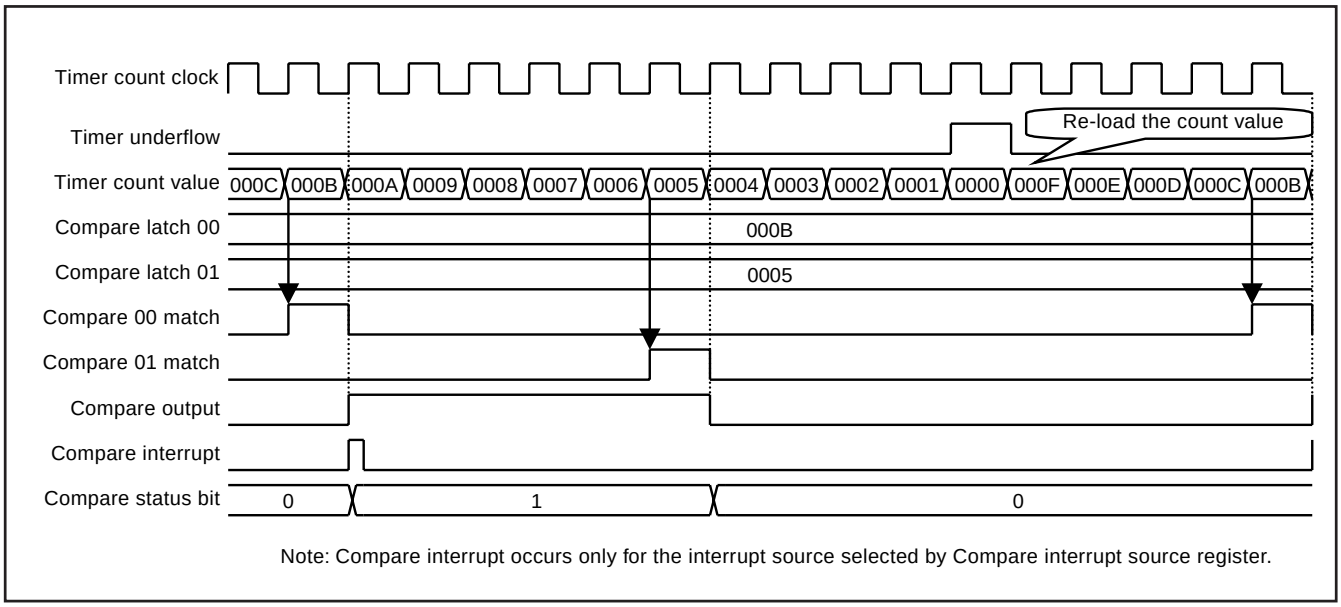

Fig. 38 Output compare mode (general waveform)

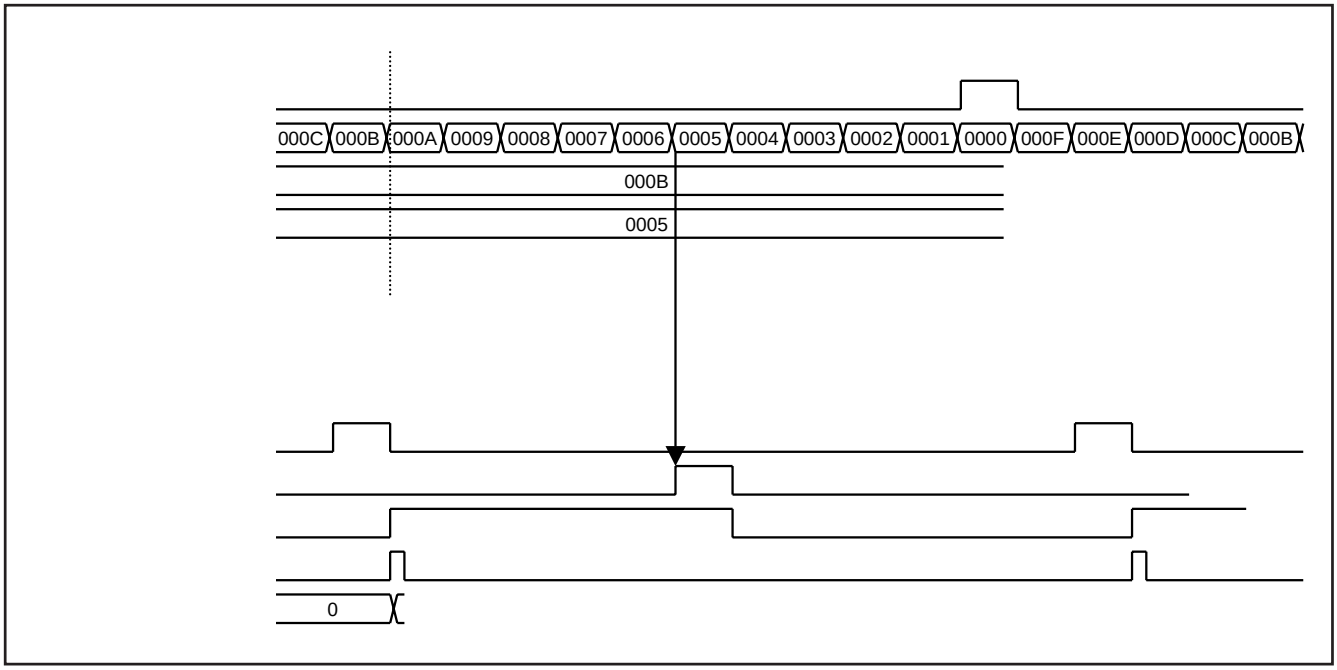

Fig. 39 Output compare mode (compare register write timing)

Notes on Clock Generating Circuit

1. Switch of ceramic and RC oscillations
After releasing reset, the oscillation mode selection bit (bit 5 of CPU mode register (address $003B_{16}$)) is “0” (ceramic oscillation selected). When the RC oscillation is used, after releasing reset, set this bit to “1”.

2. Double-speed mode
The double-speed mode can be used only when a ceramic oscillation is selected. Do not use it when an RC oscillation is selected.

3. CPU mode register
Oscillation mode selection bit (bit 5), processor mode bits (bits 1 and 0) of CPU mode register (address $003B_{16}$) are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by erroneously writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting, it is disabled to write any data to the bit. (The emulator MCU “M37542RSS” is excluded.)
Also, when the read-modify-write instructions (SEB, CLB, etc.) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

4. Clock division ratio, X_{IN} oscillation control, on-chip oscillator control
The state transition shown in Fig. 78 can be performed by setting the clock division ratio selection bits (bits 7 and 6), X_{IN} oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 78.

5. On-chip oscillator operation
When the MCU operates by the on-chip oscillator for the main clock, connect X_{IN} pin to V_{CC} through a 1 kΩ to 10 kΩ resistor and leave X_{OUT} pin open.
The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that this margin of frequencies when designing application products.

6. Ceramic resonator
When the ceramic resonator is used for the main clock, connect the ceramic resonator and the external circuit to pins X_{IN} and X_{OUT} at the shortest distance. Externally connect a damping resistor Rd depending on the oscillation frequency. A feedback resistor is built-in.
Use the resonator manufacturer’s recommended value because constants such as capacitance depend on the resonator.

7. RC oscillation
When the RC oscillation is used for the main clock, connect the X_{IN} pin and X_{OUT} pin to the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

8. External clock
When the external signal clock is used for the main clock, connect the X_{IN} pin to the clock source and leave X_{OUT} pin open.
Select “0” (ceramic oscillation) to oscillation mode selection bit.

9. Count source (Timer 1, Timer A, Timer B, Timer X, Serial I/O, Serial I/O2, A/D converter, Watchdog timer)
The count sources of these functions are affected by the clock division selection bit of the CPU mode register.
The f(X_{IN}) clock is supplied to the watchdog timer when selecting f(X_{IN}) as the CPU clock.
The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.
However, the watchdog timer is also affected by the function set ROM.

Notes on Oscillation Control

1. Oscillation stop detection circuit
(1) When the stop mode is used, set the oscillation stop detection function to “invalid”.

(2) When the ceramic or RC oscillation is stopped by the X_{IN} oscillation control bit (bit 4 of CPU mode register (address $003B_{16}$)), set the oscillation stop detection function to “invalid”.

2. Stop mode
(1) When the stop mode is used, set the oscillation stop detection function to “invalid”.

(2) When the stop mode is used, set “0” (**STP** instruction enabled) to the **STP** instruction function selection bit of the watchdog timer control register (bit 6 of watchdog timer control register (address 0039_{16})).

(3) The oscillation stabilizing time after release of **STP** instruction can be selected from “set automatically ”/“not set automatically” by the oscillation stabilizing time set bit after release of the **STP** instruction (bit 0 of MISRG (address 0038_{16})). When “0” is set to this bit, “01_{16}” is set to timer 1 and “FF_{16}” is set to prescaler 1 automatically at the execution of the STP instruction. When “1” is set to this bit, set the wait time to timer 1 and prescaler 1 according to the oscillation stabilizing time of the oscillation. Also, when timer 1 is used, set values again to timer 1 and prescaler 1 after system is returned from the stop mode.

(4) Do not execute the **STP** instruction during the A/D conversion.

Notes on On-chip Oscillation Division Ratio

- When the clock division ratio is switched from f(X_{IN}) to on-chip oscillator by the clock division ratio selection bits (bits 7 and 6 of CPU mode register (address $003B_{16}$)), the on-chip oscillator division ratio (bits 1 and 0 of on-chip oscillation division ratio selection register (address 0037_{16})) is “10_2” (on-chip oscillator middle-speed mode (R_{OSC}/8)).

REVISION HISTORY	7547 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.22	Mar 31, 2009	80	- Power-on reset circuit characteristics: TW(V_{POR}) Limits Max. and Min. values changed. - Low voltage detection circuit characteristics: TW(V_{LVD}) and TW (V_{LVD} -V_{DET}) eliminated. V_{DET-} → V_{DET}, V(V_{DET+}-V_{DET-}) deleted. - Fig. 99 revised.
		86	- “1. Processor Status Register” revised - The last Fig. 2 Sequence of PLP Instruction execution deleted. - Figure title of Fig. 3 revised
		87	“4. Modifying output data with bit managing instruction” revised.
		94	- “Precautions Regarding Overvoltage” added - “Notes On QzROM Writing Orders” revised.

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