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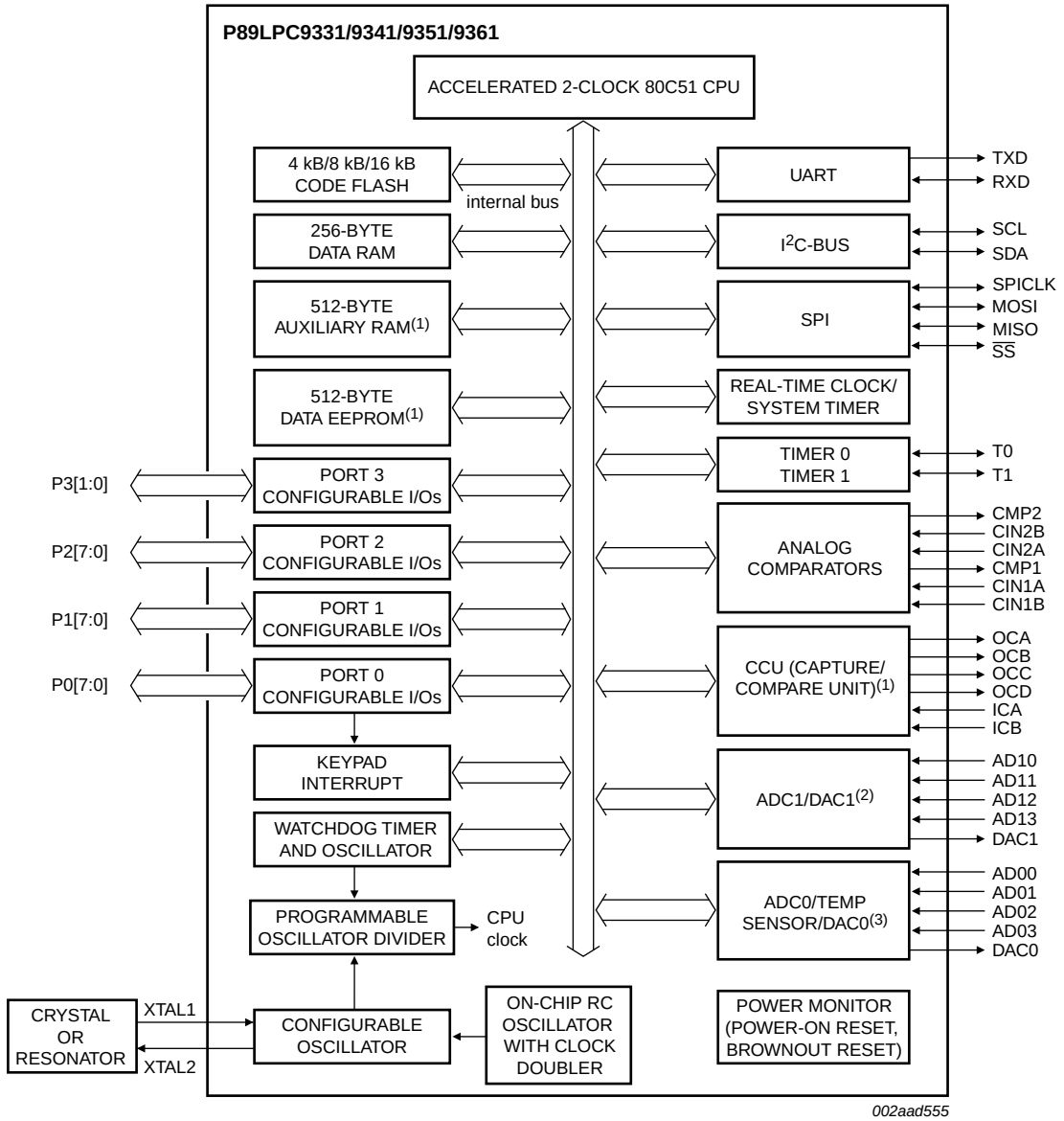
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9341fdh-512

4. Block diagram



(1) P89LPC9351/9361

(2) PGA1 on P89LPC9351/9361

(3) PGA0 on P89LPC9351/9361

Fig 1. Block diagram

5. Functional diagram

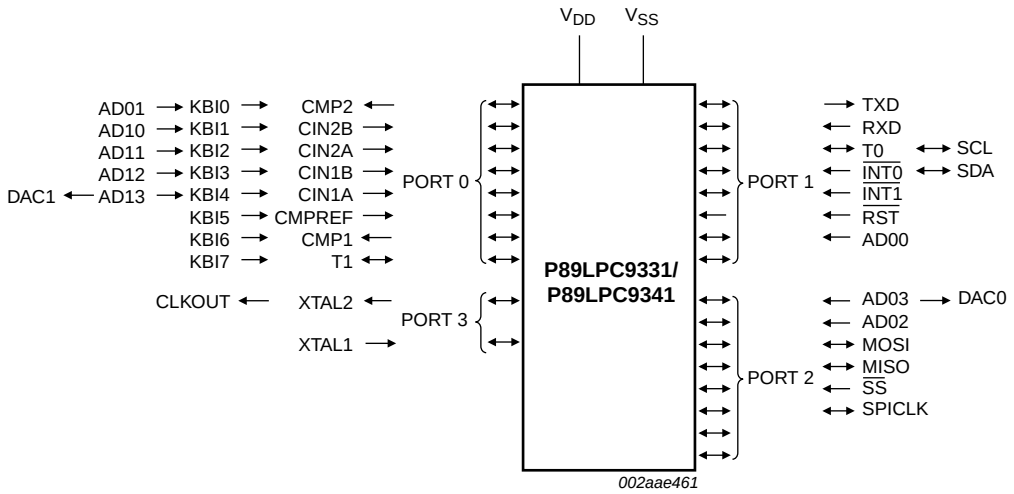


Fig 2. Functional diagram (P89LPC9331/9341)

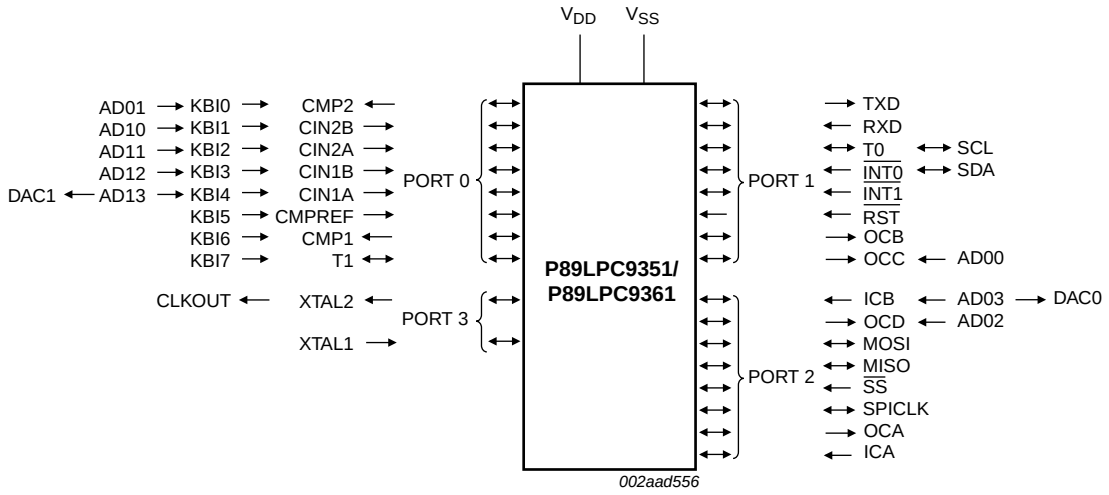


Fig 3. Functional diagram (P89LPC9351/9361)

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P0.6/CMP1/KBI6	20	I/O	**P0.6 —** Port 0 bit 6. High current source.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	19	I/O	**P0.7 —** Port 0 bit 7. High current source.
		I/O	**T1 —** Timer/counter 1 external count input or overflow output.
		I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7		I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.16.1 “Port configurations” and Table 12 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD	17	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
P1.2/T0/SCL	12	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{\text{INT0}}$/SDA	11	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{\text{INT1}}$	10	I/O	**P1.4 —** Port 1 bit 4. High current source.
		I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P1.5/$\overline{\text{RST}}$	6	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P1.6/OCB	5	I/O	**P1.6 —** Port 1 bit 6. High current source.
		O	**OCB —** Output Compare B. (P89LPC9351/9361)
P1.7/OCC/AD00	4	I/O	**P1.7 —** Port 1 bit 7. High current source.
		O	**OCC —** Output Compare C. (P89LPC9351/9361)
		I	**AD00 —** ADC0 channel 0 analog input.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P2.0 to P2.7		I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 12 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 2 also provides various special functions as described below:
P2.0/ICB/DAC0 /AD03	1	I/O	**P2.0 —** Port 2 bit 0.
		I	**ICB —** Input Capture B. (P89LPC9351/9361)
		O	**DAC0 —** Digital-to-analog converter output.
		I	**AD03 —** ADC0 channel 3 analog input.
P2.1/OCD/AD02	2	I/O	**P2.1 —** Port 2 bit 1.
		O	**OCD —** Output Compare D. (P89LPC9351/9361)
		I	**AD02 —** ADC0 channel 2 analog input.
P2.2/MOSI	13	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	15	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	16	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6/OCA	27	I/O	**P2.6 —** Port 2 bit 6.
		O	**OCA —** Output Compare A. (P89LPC9351/9361)
P2.7/ICA	28	I/O	**P2.7 —** Port 2 bit 7.
		I	**ICA —** Input Capture A. (P89LPC9351/9361)
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 12 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	9	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P3.1/XTAL1	8	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	7	I	**Ground:** 0 V reference.
V_{DD}	21	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

Table 4. Special function registers - P89LPC9331/9341 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	

Table 6. Special function registers - P89LPC9351/9361

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON0	A/D control register 0	8EH	ENBI0	ENADCI0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	ADI03	ADI02	ADI01	ADI00	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	BNDI0	BURST0	SCC0	SCAN0	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	INBND0	ENDAC1	ENDAC0	BSA1	BSA0	00	000x 0000
AD0BH	A/D_0 boundary high register	BBH									FF	1111 1111
AD0BL	A/D_0 boundary low register	A6H									00	0000 0000
AD0DAT0	A/D_0 data register 0	C5H									00	0000 0000
AD0DAT1	A/D_0 data register 1	C6H									00	0000 0000
AD0DAT2	A/D_0 data register 2	C7H									00	0000 0000
AD0DAT3	A/D_0 data register 3	F4H									00	0000 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000

Table 6. Special function registers - P89LPC9351/9361

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
TPCR2L	Prescaler control register low	CAH	TPCR2L.7	TPCR2L.6	TPCR2L.5	TPCR2L.4	TPCR2L.3	TPCR2L.2	TPCR2L.1	TPCR2L.0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high-impedance) state after power-up.

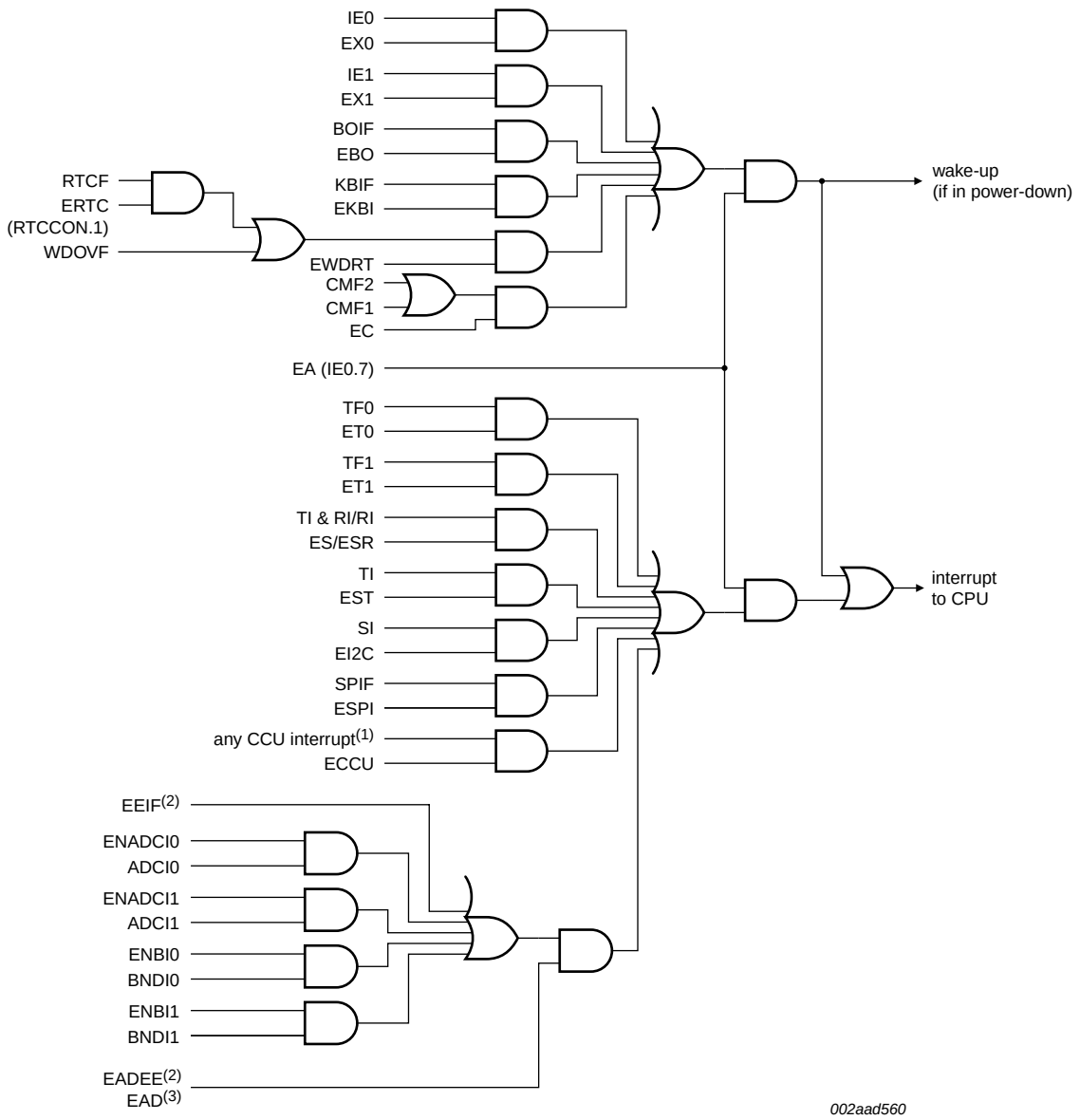
[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC9351/9361 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.



(1) See Section 7.22 “CCU (P89LPC9351/9361)”.

(2) P89LPC9351/9361

(3) P89LPC9331/9341

Fig 8. Interrupt sources, interrupt enables, and power-down wake-up sources

7.20.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.21 RTC/system timer

The P89LPC9331/9341/9351/9361 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

7.22 CCU (P89LPC9351/9361)

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four compare/PWM outputs with selectable polarity
- Symmetrical/asymmetrical PWM selection
- Two capture inputs with event counter and digital noise rejection filter
- Seven interrupts with common interrupt vector (one overflow, two capture, four compare)
- Safe 16-bit read/write via shadow registers.

7.22.1 CCU clock

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a PLL. The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

7.22.2 CCUCLK prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

7.22.3 Basic timer operation

The timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

7.23.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 7.23.5 “Baud rate generator and selection”).

7.23.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

7.23.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 7.23.5 “Baud rate generator and selection”).

7.23.5 Baud rate generator and selection

The P89LPC9331/9341/9351/9361 enhanced UART has an independent baud rate generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 13). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent baud rate generators use OSCCLK.

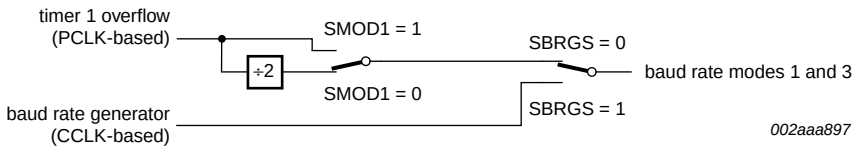


Fig 13. Baud rate sources for UART (Modes 1, 3)

7.23.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

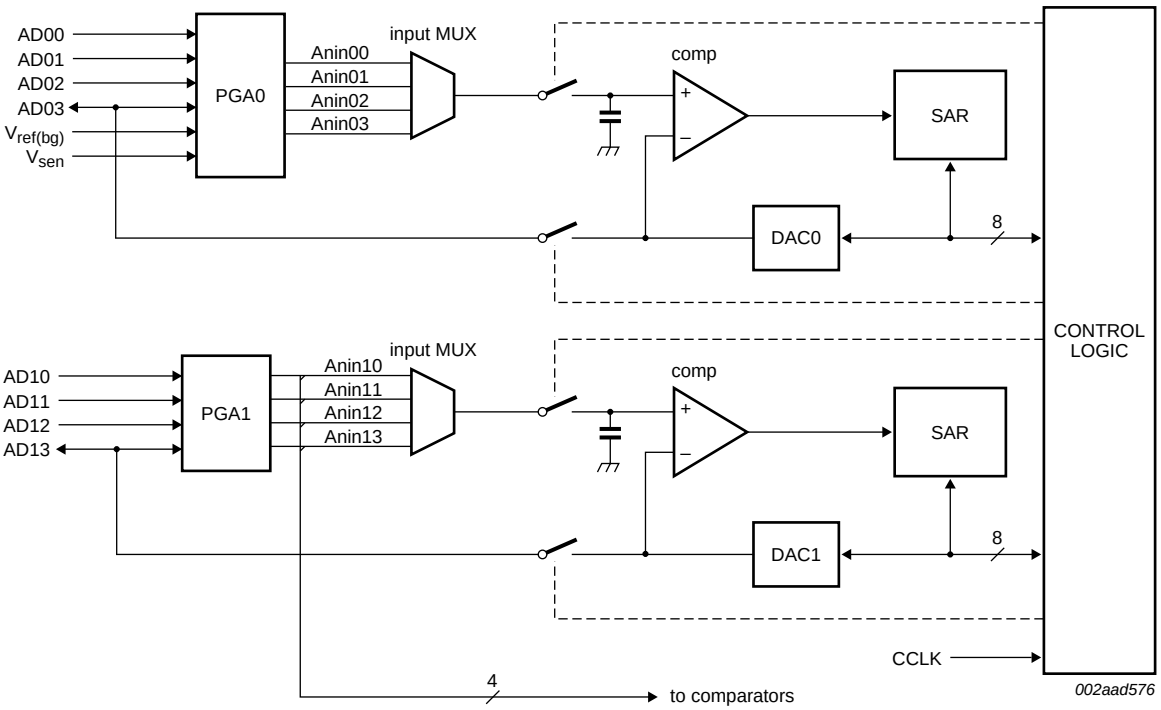


Fig 24. P89LPC9351/9361 ADC block diagram

8.4 PGA (P89LPC9351/9361)

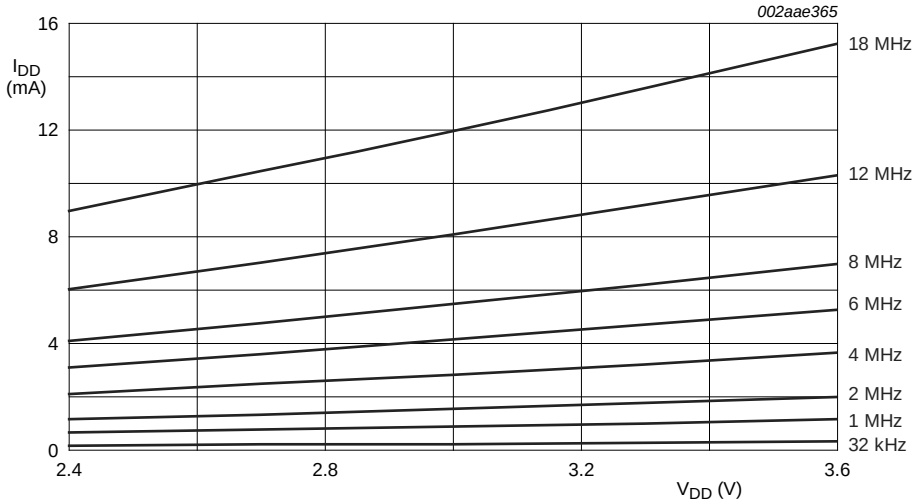
Additional PGA module is integrated in each ADC module to improve the effective resolution of the ADC. A single channel can be selected for amplification. The gain of PGA can be programmable to 2, 4, 8 and 16. Please refer to Table 12 “Static characteristics” for detailed specifications.

Register PGACONx and PGACONxB are used to for PGA configuration. Register PGAxTRIM2X4X and PGAxTRIM8X16X provide trim value of PGA gain level. As power-on, default trim value for each gain setting is loaded into the PGA trim registers. For accurate measurements, offset calibration is required.

Please see the *P89LPC9331/9341/9351/9361 User manual* for detail configuration, calibration, and usage information.

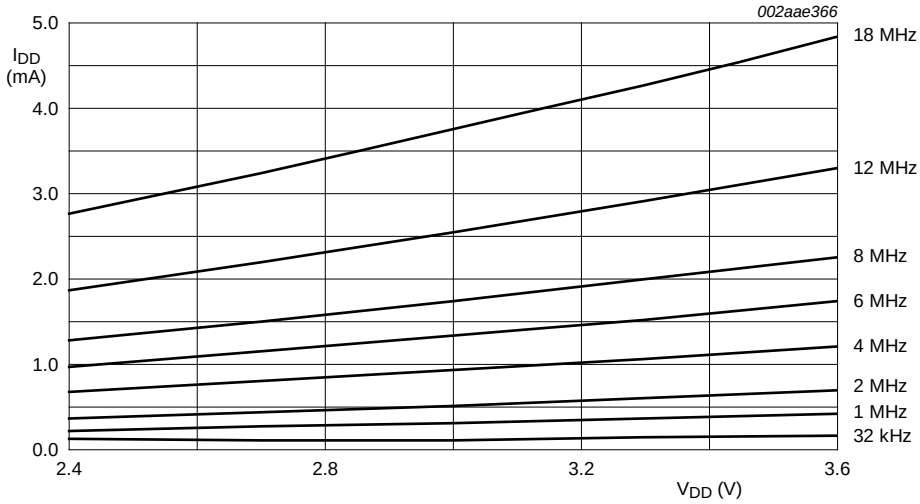
8.5 Temperature sensor

An on-chip wide-temperature range temperature sensor is integrated with ADC0 module. It provides temperature sensing capability of −40 °C ~ 85 °C. It is necessary to measure the 1.2 V reference voltage via the ADC before measuring temperature. In P89LPC9351/9361, the reference voltage, temperature sensor and AD03 input pin multiplex one input to PGA0. Please see the *P89LPC9331/9341/9351/9361 User manual* for detail usage of temperature sensor.



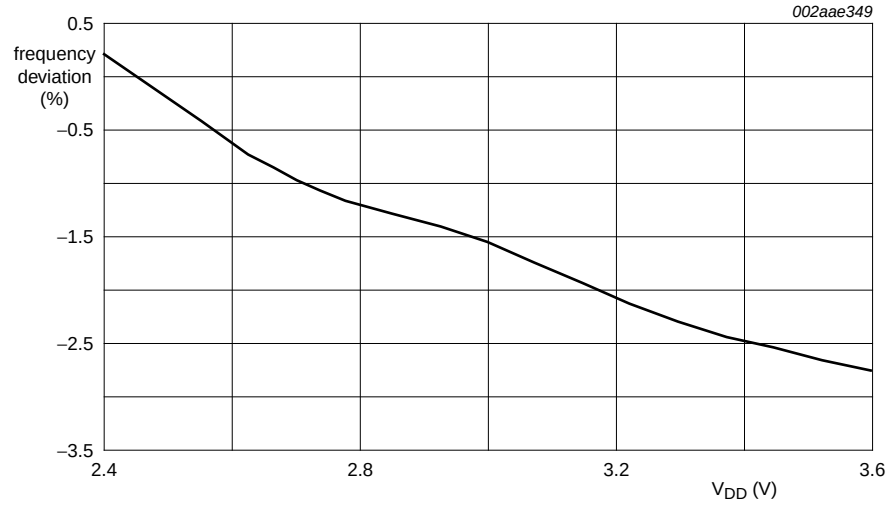
Test conditions: normal mode, code while(1) {} executed from on-chip flash; using an external clock.

Fig 28. $I_{DD(oper)}$ vs. frequency at +85 °C



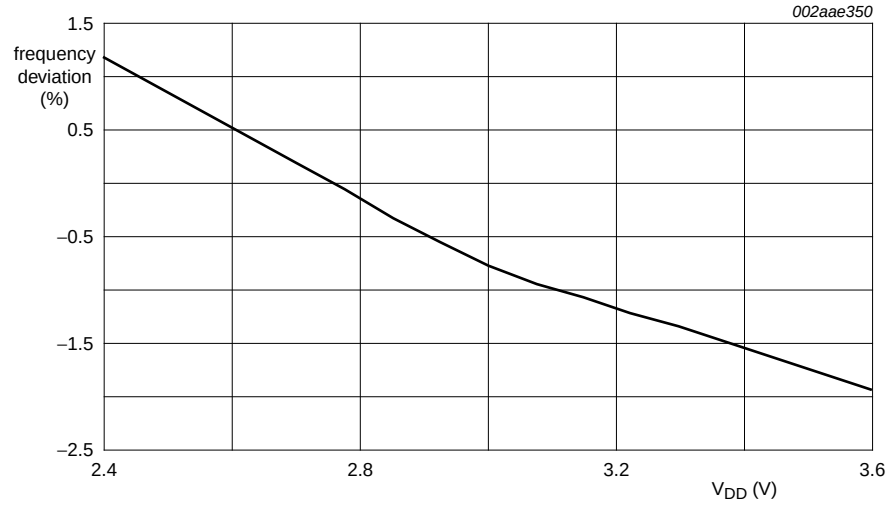
Test conditions: idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

Fig 29. $I_{DD(idle)}$ vs. frequency at +25 °C



Central frequency of watchdog oscillator = 400 KHz

Fig 38. Average watchdog oscillator frequency vs. V_{DD} at –40 °C



Central frequency of watchdog oscillator = 400 KHz

Fig 39. Average watchdog oscillator frequency vs. V_{DD} at +85 °C

10.3 BOD characteristics

Table 13. BOD static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
BOD interrupt						
V_{trip}	trip voltage	falling stage				
		BOICFG1, BOICFG0 = 01	2.25	-	2.55	V
		BOICFG1, BOICFG0 = 10	2.60	-	2.80	V
		BOICFG1, BOICFG0 = 11	3.10	-	3.40	V
		rising stage				
		BOICFG1, BOICFG0 = 01	2.40	-	2.60	V
		BOICFG1, BOICFG0 = 10	2.70	-	2.90	V
		BOICFG1, BOICFG0 = 11	3.10	-	3.40	V
BOD reset						
V_{trip}	trip voltage	falling stage				
		BOE1, BOE0 = 01	2.10	-	2.30	V
		BOE1, BOE0 = 10	2.35	-	2.50	V
		BOE1, BOE0 = 11	2.90	-	3.20	V
		rising stage				
		BOE1, BOE0 = 01	2.20	-	2.40	V
		BOE1, BOE0 = 10	2.45	-	2.60	V
		BOE1, BOE0 = 11	2.90	-	3.30	V
BOD EEPROM/FLASH						
V_{trip}	trip voltage	falling stage	2.25	-	2.60	V
		rising stage	2.35	-	2.65	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

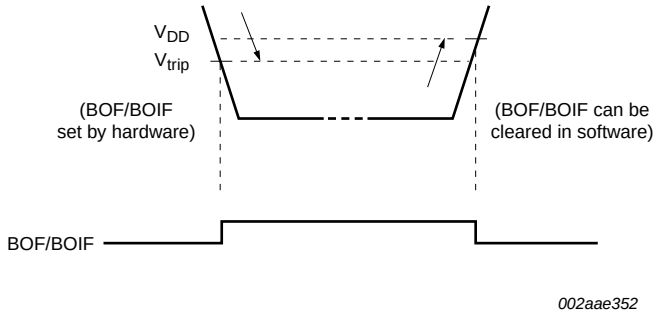


Fig 40. BOD interrupt/reset characteristics

Table 15. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 45, 46					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 45, 46					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 43, 44, 45, 46					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 43, 44, 45, 46					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 43, 44, 45, 46					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 43, 44, 45, 46					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 45, 46					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 45, 46					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 43, 44, 45, 46					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 43, 44, 45, 46	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 43, 44, 45, 46					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 43, 44, 45, 46					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

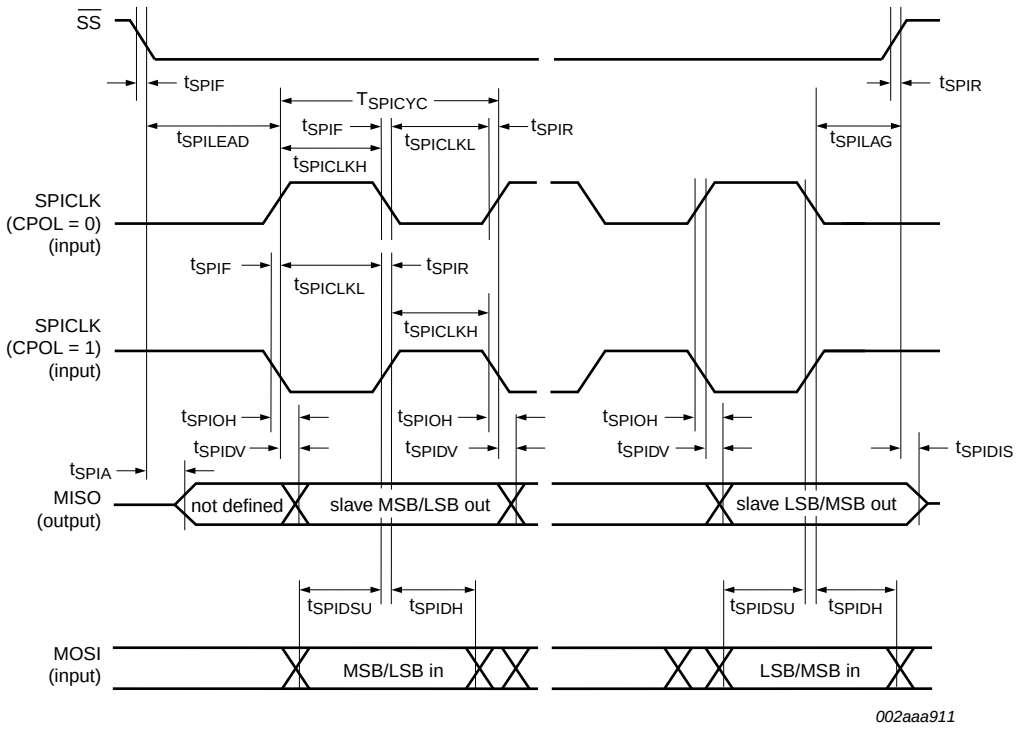


Fig 46. SPI slave timing (CPHA = 1)

11.2 ISP entry mode

Table 16. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	V_{DD} active to $\overline{RST}$ active delay time	pin $\overline{RST}$	50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time	pin $\overline{RST}$	1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time	pin $\overline{RST}$	1	-	-	µs

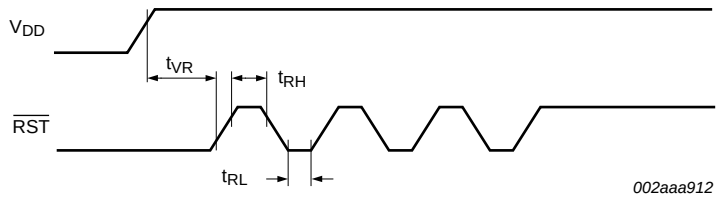


Fig 47. ISP entry waveform

15. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC9331_9341_9351_9361 v.5.1	20120820	Product data sheet	-	P89LPC9331_9341_9351_ 9361 v.5
Modifications:	• Table 6 “Special function registers - P89LPC9351/9361”: Corrected reset value for DEECON register.			
P89LPC9331_9341_9351_9361 v.5	20110110	Product data sheet	-	P89LPC9331_9341_9351_ 9361 v.4
Modifications:	• Table 12 “Static characteristics”: Added V_{POR}. • Section 7.19 “Reset”: Added sentence “When this pin functions as a reset input...”.			
P89LPC9331_9341_9351_9361 v.4	20100910	Product data sheet	-	P89LPC9331_9341_9351_ 9361 v.3
P89LPC9331_9341_9351_9361 v.3	20090602	Product data sheet	-	P89LPC9331_9341_9351 v.2
P89LPC9331_9341_9351 v.2	20090505	Product data sheet	-	P89LPC9351 v.1
P89LPC9351 v.1	20081119	Preliminary data sheet	-	-

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