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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9351fa-112

2.2 Additional features

- Â A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Â Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Â Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- Â In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Â Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to ±5 %, requiring no external components. The watchdog prescaler is selectable from eight values.
- Â High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- Â Clock switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.
- Â Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Â Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Â Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Â Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Â Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Â High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Â Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Â Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Â Only power and ground connections are required to operate the P89LPC9331/9341/9351/9361 when internal reset option is selected.
- Â Four interrupt priority levels.
- Â Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Â Schmitt trigger port inputs.
- Â Second data pointer.
- Â Emulation support.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC9331FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC9331HDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC9341FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC9351FA	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2
P89LPC9351FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC9361FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC9331FDH	4 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9331HDH	4 kB	−40 °C to +125 °C	0 MHz to 18 MHz
P89LPC9341FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9351FA	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9351FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9361FDH	16 kB	−40 °C to +85 °C	0 MHz to 18 MHz

5. Functional diagram

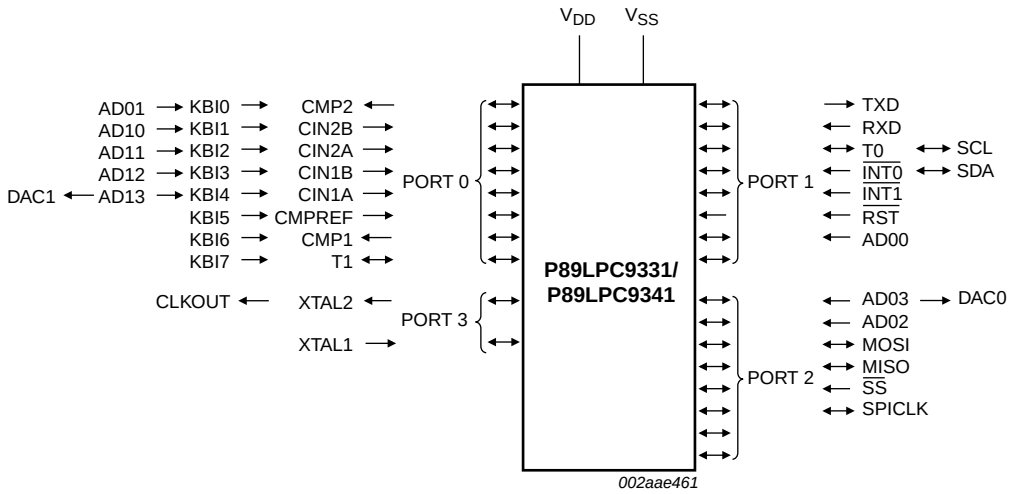


Fig 2. Functional diagram (P89LPC9331/9341)

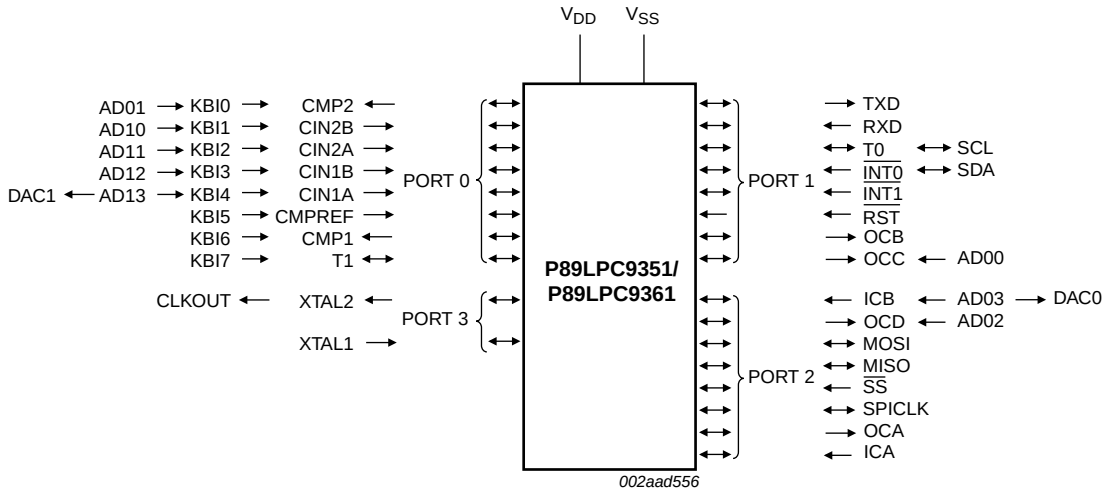


Fig 3. Functional diagram (P89LPC9351/9361)

Table 6. Special function registers - P89LPC9351/9361

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator 0 rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1	OCMA0	00	0000 0000
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1	OCMB0	00	0000 0000
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1	OCMC0	00	xxxx x000
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1	OCMD0	00	xxxx x000
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx00 0000
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	EWERR1	EWERR0	EADR8	80	1000 0000
DEEDAT	Data EEPROM data register	F2H									00	0000 0000
DEEADR	Data EEPROM address register	F3H									00	0000 0000

Table 6. Special function registers - P89LPC9351/9361

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCD	ALTAB	TDIR2	TMOD21	TMOD20	00	0000 0000
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1	PLLDV.0	00	0xxx 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TH2	CCU timer high	CDH									00	0000 0000
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2D	TOCIE2C	TOCIE2B	TOCIE2A	-	TICIE2B	TICIE2A	00	0000 0x00
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B	TICF2A	00	0000 0x00
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1	ENCINT.0	00	xxxx x000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TL2	CCU timer low	CCH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TOR2H	CCU reload register high	CFH									00	0000 0000
TOR2L	CCU reload register low	CEH									00	0000 0000
TPCR2H	Prescaler control register high	CBH	-	-	-	-	-	-	TPCR2H.1	TPCR2H.0	00	xxxx xx00

7.2 Enhanced CPU

The P89LPC9331/9341/9351/9361 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC9331/9341/9351/9361 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 7) and can also be optionally divided to a slower frequency (see Section 7.11 “CCLK modification: DIVM register”).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC9331/9341/9351/9361 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 Crystal oscillator option

The crystal oscillator option can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK, and RTC. Low speed oscillator option can be the clock source of WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

7.13 Memory organization

The various P89LPC9331/9341/9351/9361 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA (P89LPC9351/9361)

  'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC9351/9361 has 512 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9331/9341/9351/9361 has 4 kB/8 kB/16 kB of on-chip Code memory.

The P89LPC9351/9361 also has 512 bytes of on-chip data EEPROM that is accessed via SFRs (see Section 7.14).

7.14 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 8.

Table 8. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (External Data) on-chip memory that is accessed using the MOVX instructions (P89LPC9351/9361)	512

7.15 Interrupts

The P89LPC9331/9341/9351/9361 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9331/9341/9351/9361 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, I^2C-bus, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write/ADC completion.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.18.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.19 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit. When this pin functions as a reset input, an internal pull-up resistance is connected (see Table 12 “Static characteristics”).

Note: During a power cycle, V_{DD} must fall below V_{POR} before power is reapplied, in order to ensure a power-on reset (see Table 12 “Static characteristics”).

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A Watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

Since N ranges from 0 to 15, the CCLK frequency can be in the range of PCLK to PCLK/16.

7.22.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

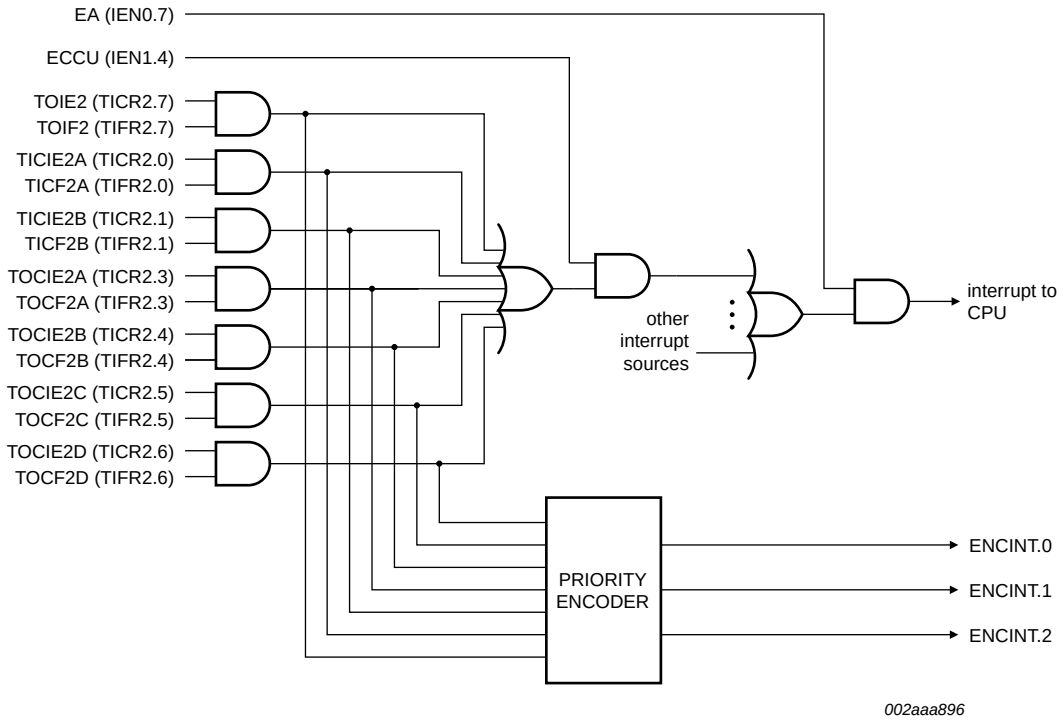


Fig 12. Capture/compare unit interrupts

7.23 UART

The P89LPC9331/9341/9351/9361 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC9331/9341/9351/9361 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.23.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

7.25 SPI

The P89LPC9331/9341/9351/9361 provides another high-speed serial communication interface: the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master mode or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

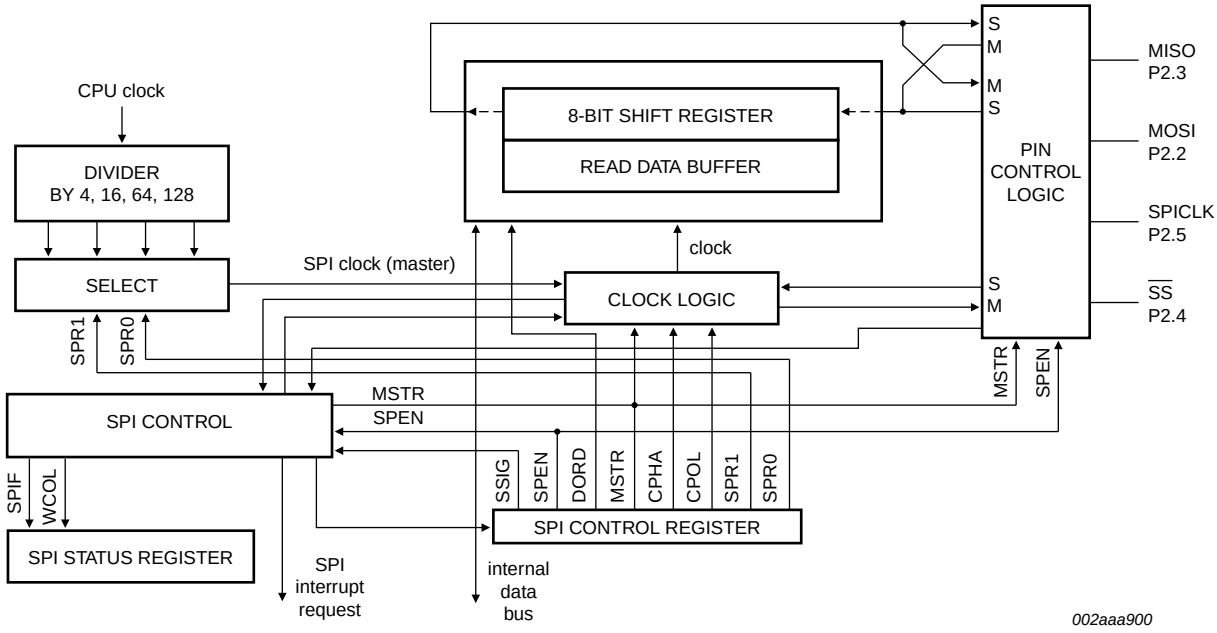


Fig 16. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 17 through Figure 19.

9. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature			−55	+125	°C
T_{stg}	storage temperature			−65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin			-	20	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin			-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current			-	100	mA
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pin to V_{SS}		-	V_{DD} + 0.5	V
V_n	voltage on any other pin	except XTAL1, XTAL2 to V_{SS}		−0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[2]	−3000	+3000	V
		charged device model; all pins		−700	+700	V

[1] The following applies to Table 11:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

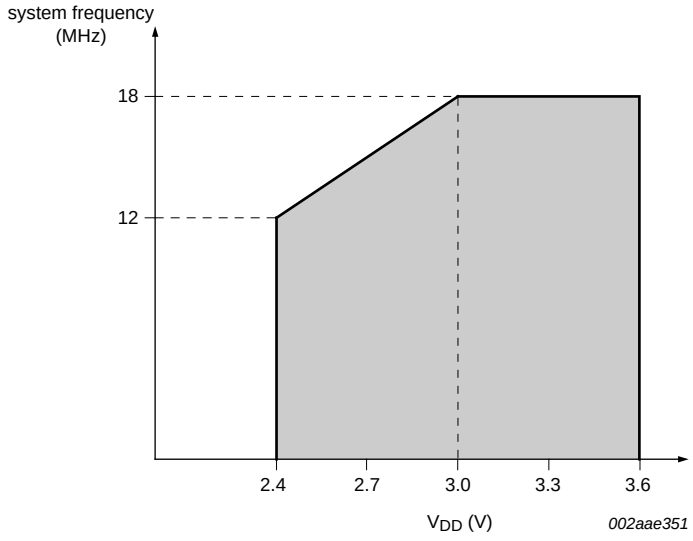
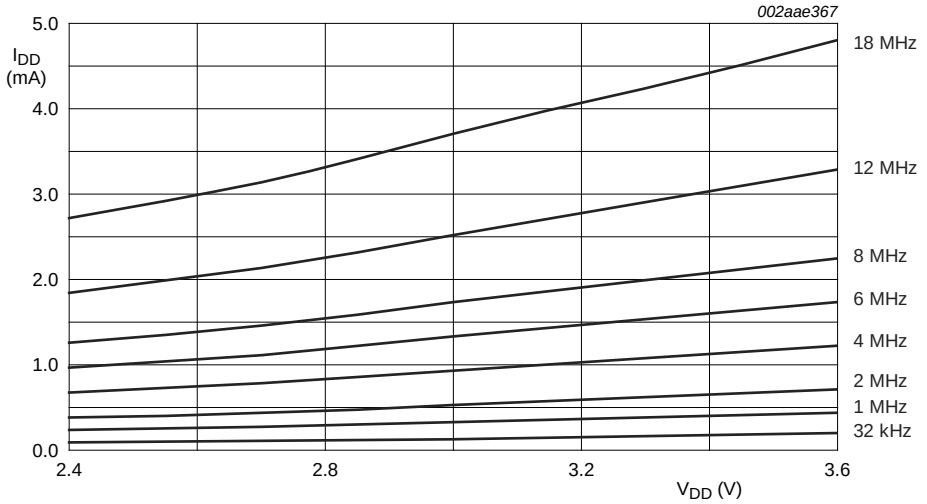
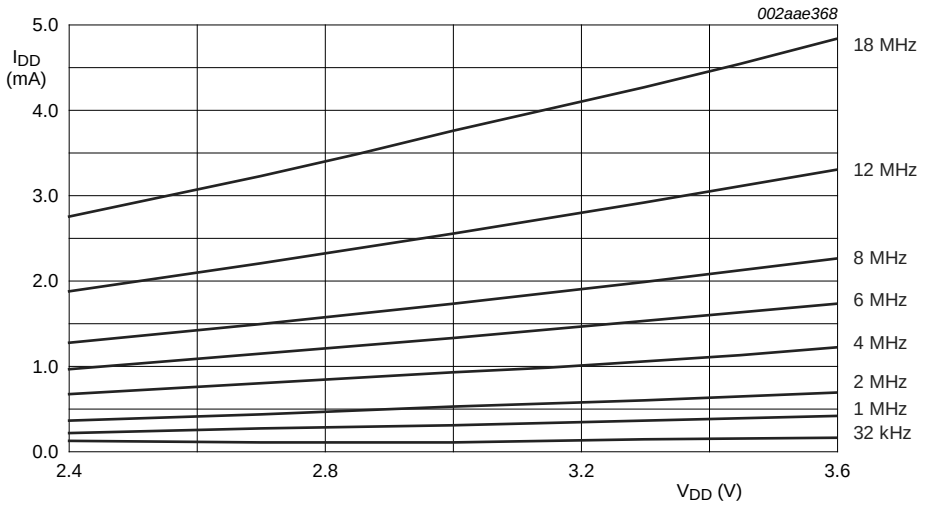


Fig 25. Frequency vs. supply voltage



Test conditions: idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

Fig 30. $I_{DD(idle)}$ vs. frequency at –40 °C



Test conditions: idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

Fig 31. $I_{DD(idle)}$ vs. frequency at +85 °C

10.3 BOD characteristics

Table 13. BOD static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
BOD interrupt						
V_{trip}	trip voltage	falling stage				
		BOICFG1, BOICFG0 = 01	2.25	-	2.55	V
		BOICFG1, BOICFG0 = 10	2.60	-	2.80	V
		BOICFG1, BOICFG0 = 11	3.10	-	3.40	V
		rising stage				
		BOICFG1, BOICFG0 = 01	2.40	-	2.60	V
		BOICFG1, BOICFG0 = 10	2.70	-	2.90	V
		BOICFG1, BOICFG0 = 11	3.10	-	3.40	V
BOD reset						
V_{trip}	trip voltage	falling stage				
		BOE1, BOE0 = 01	2.10	-	2.30	V
		BOE1, BOE0 = 10	2.35	-	2.50	V
		BOE1, BOE0 = 11	2.90	-	3.20	V
		rising stage				
		BOE1, BOE0 = 01	2.20	-	2.40	V
		BOE1, BOE0 = 10	2.45	-	2.60	V
		BOE1, BOE0 = 11	2.90	-	3.30	V
BOD EEPROM/FLASH						
V_{trip}	trip voltage	falling stage	2.25	-	2.60	V
		rising stage	2.35	-	2.65	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

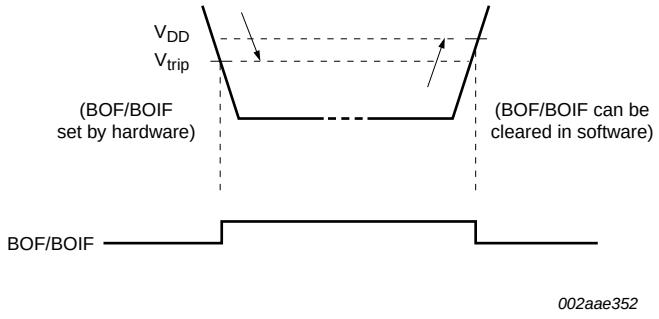


Fig 40. BOD interrupt/reset characteristics

11. Dynamic characteristics

Table 14. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	T_{amb} = 25 °C	380	420	380	420	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 41	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 41	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 41	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 41	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 41	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 42	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 42	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 42	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 42	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 42	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	2.0	MHz
	master		-	$^{CCLK}/_{4}$	-	3.0	MHz

Table 15. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	T_{amb} = 25 °C	380	420	380	420	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 41	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 41	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 41	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 41	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 41	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 42	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 42	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 42	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 42	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 42	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 43, 44, 45, 46					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns

Table 15. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, −40 °C to +125 °C extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 45, 46					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 45, 46					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 43, 44, 45, 46					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 43, 44, 45, 46					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 43, 44, 45, 46					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 43, 44, 45, 46					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 45, 46					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 45, 46					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 43, 44, 45, 46					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 43, 44, 45, 46	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 43, 44, 45, 46					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 43, 44, 45, 46					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

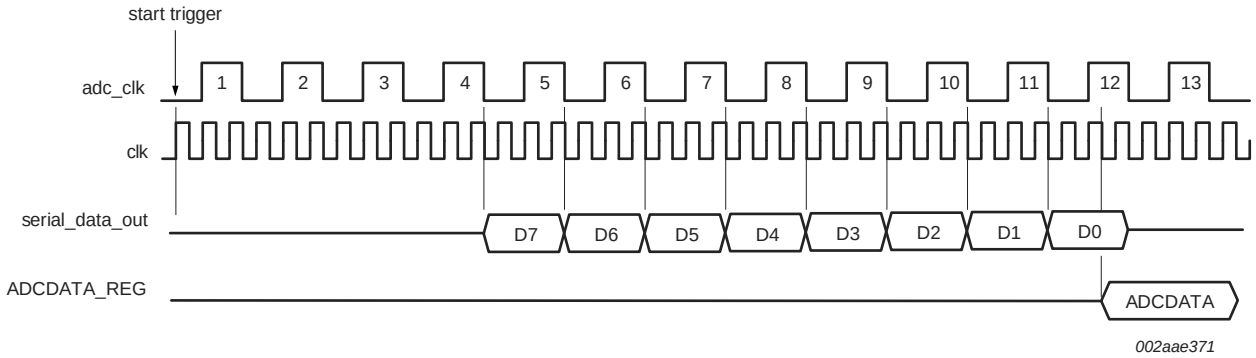


Fig 48. ADC conversion timing

15. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC9331_9341_9351_9361 v.5.1	20120820	Product data sheet	-	P89LPC9331_9341_9351_ 9361 v.5
Modifications:	• Table 6 “Special function registers - P89LPC9351/9361”: Corrected reset value for DEECON register.			
P89LPC9331_9341_9351_9361 v.5	20110110	Product data sheet	-	P89LPC9331_9341_9351_ 9361 v.4
Modifications:	• Table 12 “Static characteristics”: Added V_{POR}. • Section 7.19 “Reset”: Added sentence “When this pin functions as a reset input...”.			
P89LPC9331_9341_9351_9361 v.4	20100910	Product data sheet	-	P89LPC9331_9341_9351_ 9361 v.3
P89LPC9331_9341_9351_9361 v.3	20090602	Product data sheet	-	P89LPC9331_9341_9351 v.2
P89LPC9331_9341_9351 v.2	20090505	Product data sheet	-	P89LPC9351 v.1
P89LPC9351 v.1	20081119	Preliminary data sheet	-	-

18. Contents

continued >>

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