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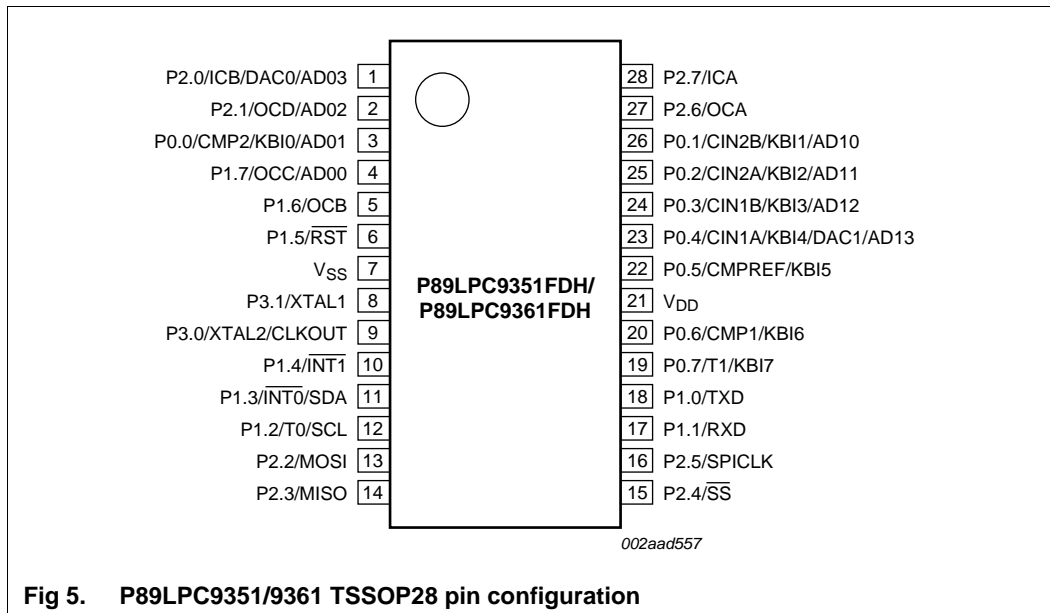
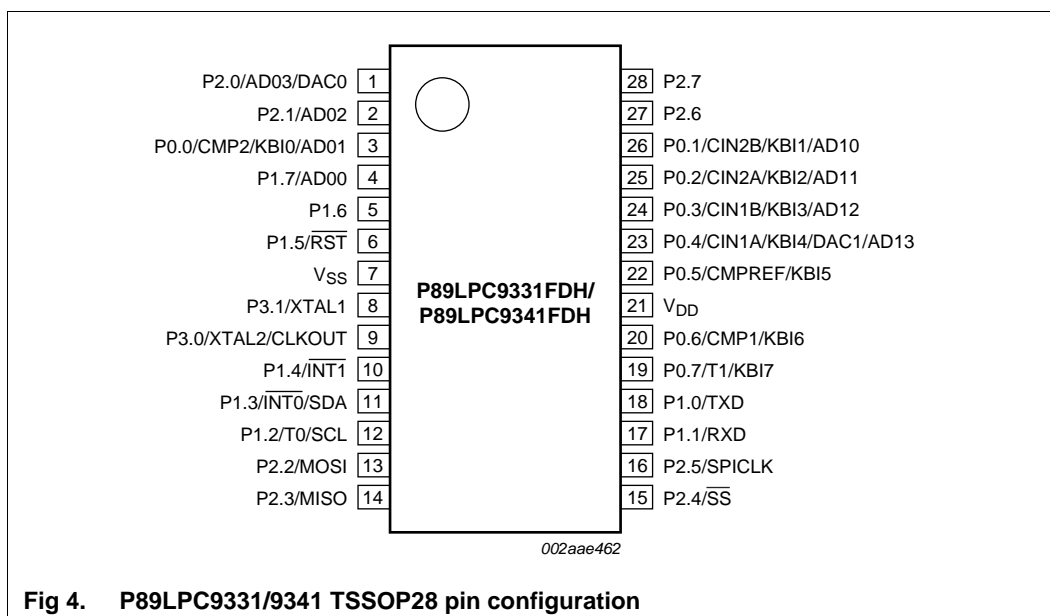
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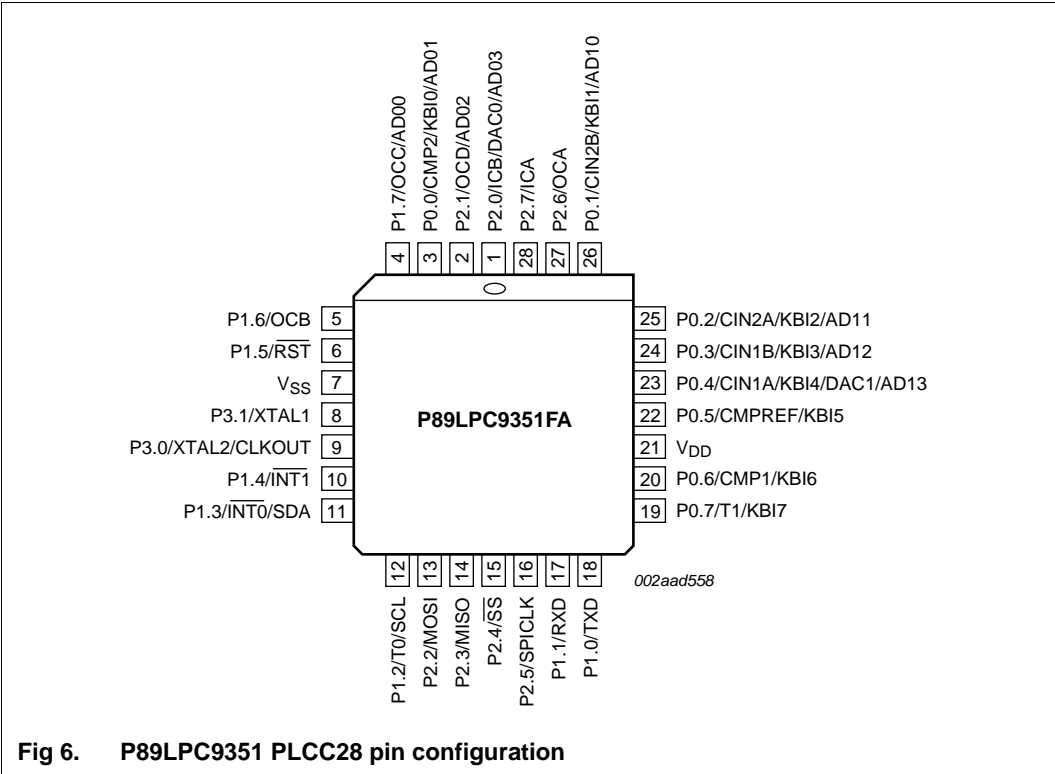
Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9351fa-529

6. Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P0.0 to P0.7		I/O	<p>Port 0: Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 12 “Static characteristics” for details.</p> <p>The Keypad Interrupt feature operates with Port 0 pins.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 0 also provides various special functions as described below:</p>
P0.0/CMP2/ KBI0/AD01	3	I/O	P0.0 — Port 0 bit 0.
		O	CMP2 — Comparator 2 output
		I	KBI0 — Keyboard input 0.
		I	AD01 — ADC0 channel 1 analog input.
P0.1/CIN2B/ KBI1/AD10	26	I/O	P0.1 — Port 0 bit 1.
		I	CIN2B — Comparator 2 positive input B.
		I	KBI1 — Keyboard input 1.
		I	AD10 — ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	25	I/O	P0.2 — Port 0 bit 2.
		I	CIN2A — Comparator 2 positive input A.
		I	KBI2 — Keyboard input 2.
		I	AD11 — ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	24	I/O	P0.3 — Port 0 bit 3. High current source.
		I	CIN1B — Comparator 1 positive input B.
		I	KBI3 — Keyboard input 3.
		I	AD12 — ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/AD13	23	I/O	P0.4 — Port 0 bit 4. High current source.
		I	CIN1A — Comparator 1 positive input A.
		I	KBI4 — Keyboard input 4.
		O	DAC1 — Digital-to-analog converter output 1.
		I	AD13 — ADC1 channel 3 analog input.
P0.5/CMPREF/ KBI5	22	I/O	P0.5 — Port 0 bit 5. High current source.
		I	CMPREF — Comparator reference (negative) input.
		I	KBI5 — Keyboard input 5.

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P0.6/CMP1/KBI6	20	I/O	P0.6 — Port 0 bit 6. High current source.
		O	CMP1 — Comparator 1 output.
		I	KBI6 — Keyboard input 6.
P0.7/T1/KBI7	19	I/O	P0.7 — Port 0 bit 7. High current source.
		I/O	T1 — Timer/counter 1 external count input or overflow output.
		I	KBI7 — Keyboard input 7.
P1.0 to P1.7		I/O, I ^[1]	Port 1: Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.16.1 "Port configurations" and Table 12 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	I/O	P1.0 — Port 1 bit 0.
		O	TXD — Transmitter output for serial port.
P1.1/RXD	17	I/O	P1.1 — Port 1 bit 1.
		I	RXD — Receiver input for serial port.
P1.2/T0/SCL	12	I/O	P1.2 — Port 1 bit 2 (open-drain when used as output).
		I/O	T0 — Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	SCL — I ² C-bus serial clock input/output.
P1.3/INT0/SDA	11	I/O	P1.3 — Port 1 bit 3 (open-drain when used as output).
		I	INT0 — External interrupt 0 input.
		I/O	SDA — I ² C-bus serial data input/output.
P1.4/INT1	10	I/O	P1.4 — Port 1 bit 4. High current source.
		I	INT1 — External interrupt 1 input.
P1.5/RST	6	I	P1.5 — Port 1 bit 5 (input only).
		I	RST — External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P1.6/OCB	5	I/O	P1.6 — Port 1 bit 6. High current source.
		O	OCB — Output Compare B. (P89LPC9351/9361)
P1.7/OCC/AD00	4	I/O	P1.7 — Port 1 bit 7. High current source.
		O	OCC — Output Compare C. (P89LPC9351/9361)
		I	AD00 — ADC0 channel 0 analog input.

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P2.0 to P2.7		I/O	<p>Port 2: Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 12 "Static characteristics" for details.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 2 also provides various special functions as described below:</p>
P2.0/ICB/DAC0 /AD03	1	I/O	P2.0 — Port 2 bit 0.
		I	ICB — Input Capture B. (P89LPC9351/9361)
		O	DAC0 — Digital-to-analog converter output.
		I	AD03 — ADC0 channel 3 analog input.
P2.1/OCD/AD02	2	I/O	P2.1 — Port 2 bit 1.
		O	OCD — Output Compare D. (P89LPC9351/9361)
		I	AD02 — ADC0 channel 2 analog input.
P2.2/MOSI	13	I/O	P2.2 — Port 2 bit 2.
		I/O	MOSI — SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	I/O	P2.3 — Port 2 bit 3.
		I/O	MISO — When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/ $\overline{\text{SS}}$	15	I/O	P2.4 — Port 2 bit 4.
		I	$\overline{\text{SS}}$ — SPI Slave select.
P2.5/SPICLK	16	I/O	P2.5 — Port 2 bit 5.
		I/O	SPICLK — SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6/OCA	27	I/O	P2.6 — Port 2 bit 6.
		O	OCA — Output Compare A. (P89LPC9351/9361)
P2.7/ICA	28	I/O	P2.7 — Port 2 bit 7.
		I	ICA — Input Capture A. (P89LPC9351/9361)
P3.0 to P3.1		I/O	<p>Port 3: Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 12 "Static characteristics" for details.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 3 also provides various special functions as described below:</p>
P3.0/XTAL2/ CLKOUT	9	I/O	P3.0 — Port 3 bit 0.
		O	XTAL2 — Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	CLKOUT — CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.

Table 4. Special function registers - P89LPC9331/9341 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	ESPI	EC	EKBI	EI2C	00 ^[1]	00x0 0000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00 ^[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00 ^[1]	x000 0000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	PSPI	PC	PKBI	PI2C	00 ^[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00 ^[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00 ^[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
	Bit address		87	86	85	84	83	82	81	80		
P0*	Port 0	80H	T1/KB7	CMP1/KB6	CMPREF/KB5	CIN1A/KB4	CIN1B/KB3	CIN2A/KB2	CIN2B/KB1	CMP2/KB0	^[1]	
	Bit address		97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	RST	INT1	INT0/SDA	T0/SCL	RXD	TXD	^[1]	
	Bit address		A7	A6	A5	A4	A3	A2	A1	A0		
P2*	Port 2	A0H	-	-	SPICKL	SS	MISO	MOSI	-	-	^[1]	
	Bit address		B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	^[1]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF ^[1]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00 ^[1]	0000 0000

Table 4. Special function registers - P89LPC9331/9341 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
WDL	Watchdog load	C1H			FF	1111 1111
WFEED1	Watchdog feed 1	C2H				
WFEED2	Watchdog feed 2	C3H				

- [1] All ports are in input only (high-impedance) state after power-up.
- [2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.
- [3] The RSTSRC register reflects the cause of the P89LPC9331/9341 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.
- [4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.
- [5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.
- [6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

Table 5. Extended special function registers - P89LPC9331/9341^[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	^[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	^[3]	
TPSCON	Temperature sensor control register	FFCAH	-	-	-	-	TSEL1	TSEL0	-	-	00	0000 0000
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A, @DPTR and MOVX @DPTR, A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

7.13 Memory organization

The various P89LPC9331/9341/9351/9361 memory spaces are as follows:

- **DATA**
128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.
- **IDATA**
Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- **SFR**
Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.
- **XDATA (P89LPC9351/9361)**
'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC9351/9361 has 512 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.
- **CODE**
64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9331/9341/9351/9361 has 4 kB/8 kB/16 kB of on-chip Code memory.

The P89LPC9351/9361 also has 512 bytes of on-chip data EEPROM that is accessed via SFRs (see [Section 7.14](#)).

7.14 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in [Table 8](#).

Table 8. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (External Data) on-chip memory that is accessed using the MOVX instructions (P89LPC9351/9361)	512

7.15 Interrupts

The P89LPC9331/9341/9351/9361 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9331/9341/9351/9361 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, I²C-bus, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write/ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.15.1 External interrupt inputs

The P89LPC9331/9341/9351/9361 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC9331/9341/9351/9361 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to [Section 7.18 "Power reduction modes"](#) for details.

7.17.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD EEPROM/FLASH.

BOD reset is always on except in total Power-down mode. It could not be disabled in software. BOD interrupt may be enabled or disabled in software. BOD EEPROM/FLASH is always on, except in Power-down modes and could not be disabled in software.

BOD reset and BOD interrupt, each has four trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt. BOD reset voltage should be lower than BOD interrupt trip point. BOD EEPROM/FLASH is used for flash/Data EEPROM programming/erase protection and has only 1 trip voltage of 2.4 V. Please refer to *P89LPC9331/9341/9351/9361 User manual* for detail configurations.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage and is negated when V_{DD} rises above the brownout trip voltage.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see [Table 12 "Static characteristics"](#) for specifications.

7.17.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.18 Power reduction modes

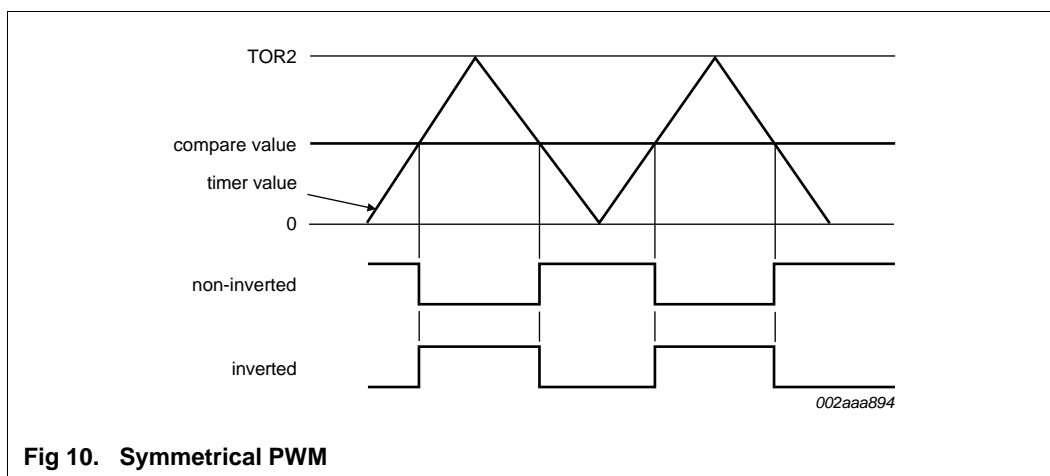
The P89LPC9331/9341/9351/9361 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.18.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

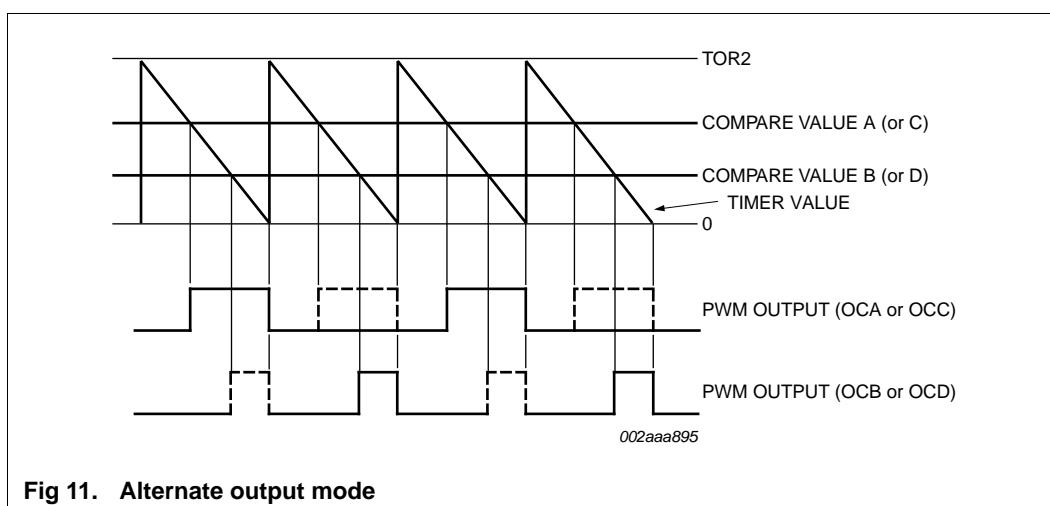
7.18.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9331/9341/9351/9361 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention supply voltage V_{DDR} . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR} , therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.



7.22.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.



7.22.8 PLL operation

The PWM module features a Phase Locked Loop that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal from 0.5 MHz to 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor from 1 to 16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in [Equation 1](#):

$$\text{PLL frequency} = \frac{\text{PCLK}}{(N + 1)} \quad (1)$$

Where: N is the value of PLLDV3:0.

7.23.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.23.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.23.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI interrupt is generated when the double buffer is ready to receive new data.

7.23.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TI interrupt.

If double buffering is enabled, TB **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.24 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in [Figure 14](#). The P89LPC9331/9341/9351/9361 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

7.25 SPI

The P89LPC9331/9341/9351/9361 provides another high-speed serial communication interface: the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master mode or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

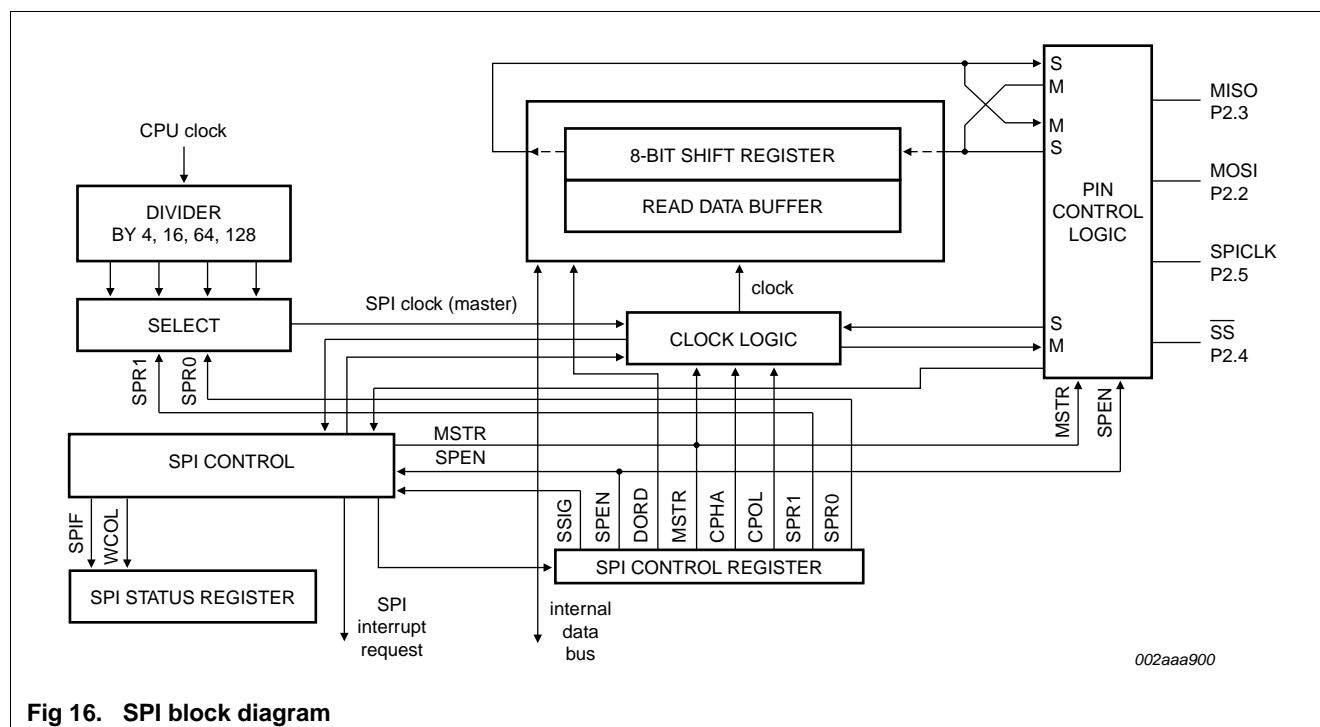


Fig 16. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and \overline{SS} :

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- \overline{SS} is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its \overline{SS} pin to determine whether it is selected.

Typical connections are shown in [Figure 17](#) through [Figure 19](#).

in result register, ADxDAT1. The first channel is again converted and its result stored in ADxDAT2. The second channel is again converted and its result placed in ADxDAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

In P89LPC9351/9361, in dual channel mode, the PGA channel selection is independent and can be different to A/D conversion channel selection. If different, the gain of the selected ADC channel is 1.

8.6.6 Single step mode

This special mode allows 'single-stepping' in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

In P89LPC9351/9361, in single step mode, the PGA channel selection is independent and can be different to A/D conversion channel selection. If different, the gain of the selected ADC channel is 1.

8.7 Conversion start modes

8.7.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all ADC operating modes.

8.7.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all ADC operating modes.

8.7.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all ADC operating modes.

8.7.4 Dual start immediately

Programming this mode starts a synchronized conversion of both A/D converters. This start mode is available in all A/D operating modes. Both A/D converters must be in the same operating mode. In the continuous conversion modes, both A/D converters must select an identical number of channels. Any trigger of either A/D will start a simultaneous conversion of both A/Ds.

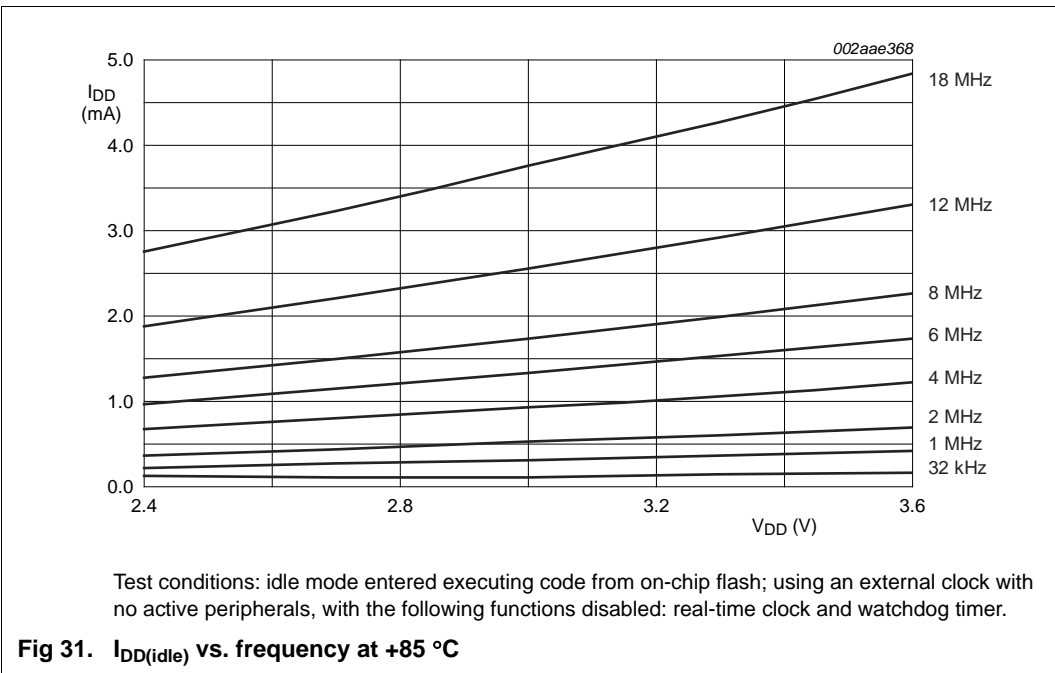
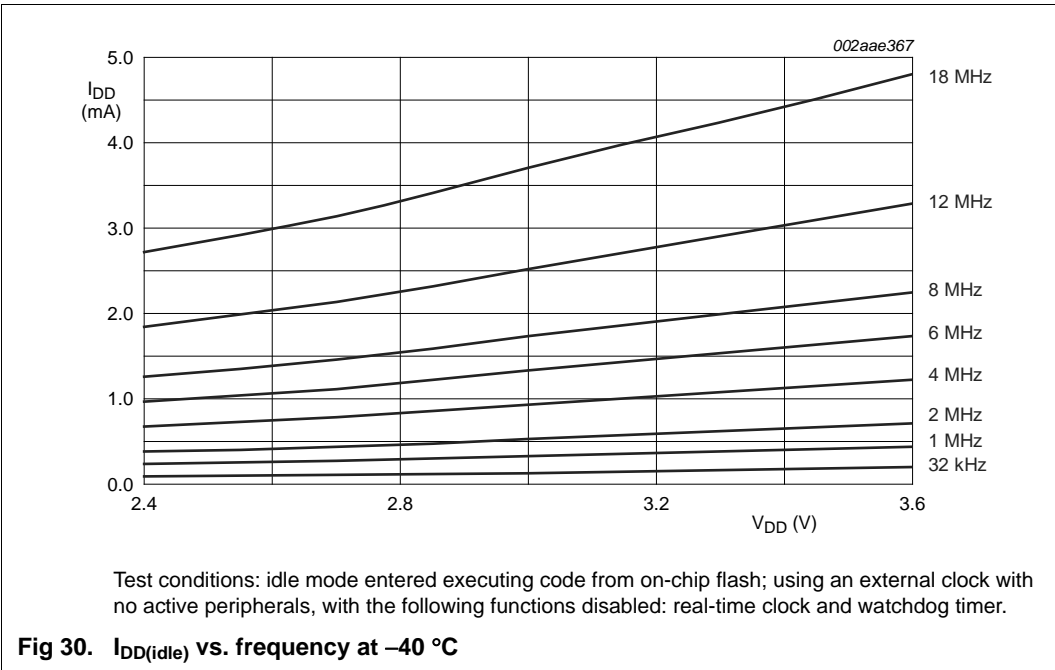
8.8 Boundary limits interrupt

Each of the A/D converters has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

Table 12. Static characteristics ...continued $V_{DD} = 2.4\text{ V to }3.6\text{ V unless otherwise specified.}$ $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C for industrial applications, }-40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C extended, unless otherwise specified.}$

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{IL}	LOW-level input current	$V_I = 0.4\text{ V}$	[9] -	-	-80	μA
I_{LI}	input leakage current	$V_I = V_{IL}, V_{IH}, \text{ or } V_{th(HL)}$	[10] -	-	± 1	μA
I_{THL}	HIGH-LOW transition current	all ports; $V_I = 1.5\text{ V}$ at $V_{DD} = 3.6\text{ V}$	[11] -30	-	-450	μA
$R_{RST_N(int)}$	internal pull-up resistance on pin \overline{RST}	pin \overline{RST}	10	-	30	$\text{k}\Omega$
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	$\text{ppm}/^{\circ}\text{C}$

- [1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.
- [2] The $I_{DD(oper)}$ specification is measured using an external clock with code while(1) {} executed from on-chip flash.
- [3] The $I_{DD(idle)}$ specification is measured using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.
- [4] The $I_{DD(pd)}$ specification is measured using internal RC oscillator with the following functions disabled: comparators, real-time clock, and watchdog timer.
- [5] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.
- [6] See Section 9 "Limiting values" for steady state (non-transient) limits on I_{OL} or I_{OH} . If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.
- [7] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS} .
- [8] Pin capacitance is characterized but not tested.
- [9] Measured with port in quasi-bidirectional mode.
- [10] Measured with port in high-impedance mode.
- [11] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.



11. Dynamic characteristics

Table 14. Dynamic characteristics (12 MHz)
 $V_{DD} = 2.4\text{ V to }3.6\text{ V unless otherwise specified.}$
 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C for industrial applications, }-40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C extended, unless otherwise specified. [1][2]}$

Symbol	Parameter	Conditions	Variable clock		f _{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
f _{osc(RC)}	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ± 1 % at T _{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V _{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
f _{osc(WD)}	internal watchdog oscillator frequency	T _{amb} = 25 °C	380	420	380	420	kHz
f _{osc}	oscillator frequency		0	12	-	-	MHz
T _{cy(clk)}	clock cycle time	see Figure 41	83	-	-	-	ns
f _{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t _{gr}	glitch rejection time	P1.5/ $\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/ $\overline{\text{RST}}$	-	15	-	15	ns
t _{sa}	signal acceptance time	P1.5/ $\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/ $\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t _{CHCX}	clock HIGH time	see Figure 41	33	T _{cy(clk)} – t _{CLCX}	33	-	ns
t _{CLCX}	clock LOW time	see Figure 41	33	T _{cy(clk)} – t _{CHCX}	33	-	ns
t _{CLCH}	clock rise time	see Figure 41	-	8	-	8	ns
t _{CHCL}	clock fall time	see Figure 41	-	8	-	8	ns
Shift register (UART mode 0)							
T _{XLXL}	serial port clock cycle time	see Figure 42	16T _{cy(clk)}	-	1333	-	ns
t _{QVXH}	output data set-up to clock rising edge time	see Figure 42	13T _{cy(clk)}	-	1083	-	ns
t _{XHQX}	output data hold after clock rising edge time	see Figure 42	-	T _{cy(clk)} + 20	-	103	ns
t _{XHDX}	input data hold after clock rising edge time	see Figure 42	-	0	-	0	ns
t _{XHDV}	input data valid to clock rising edge time	see Figure 42	150	-	150	-	ns
SPI interface							
f _{SPI}	SPI operating frequency						
	slave		0	CCLK/6	0	2.0	MHz
	master		-	CCLK/4	-	3.0	MHz

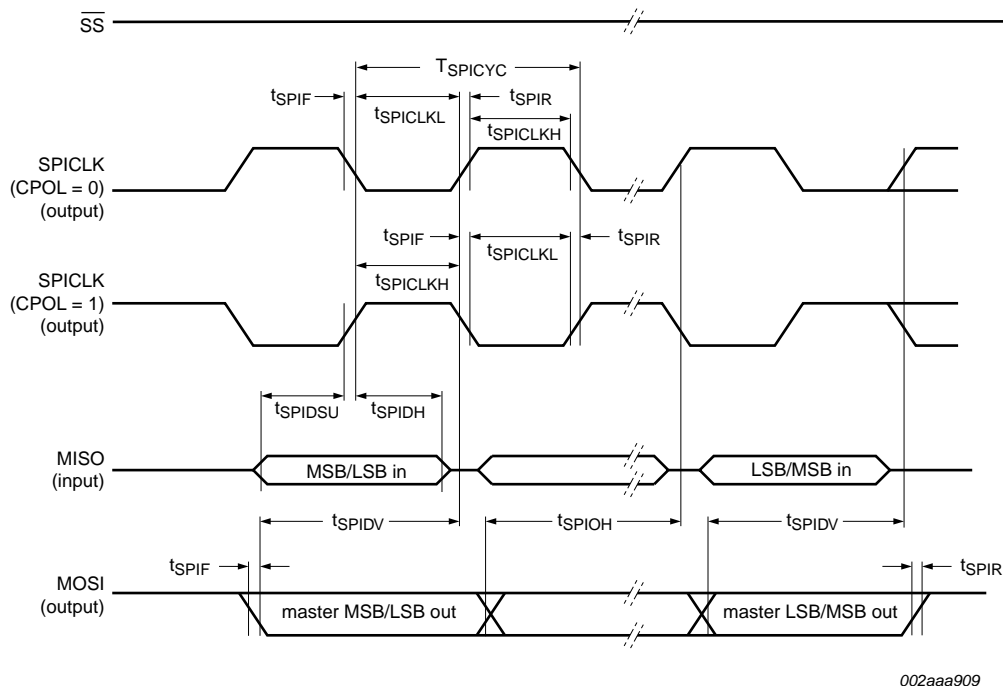


Fig 44. SPI master timing (CPHA = 1)

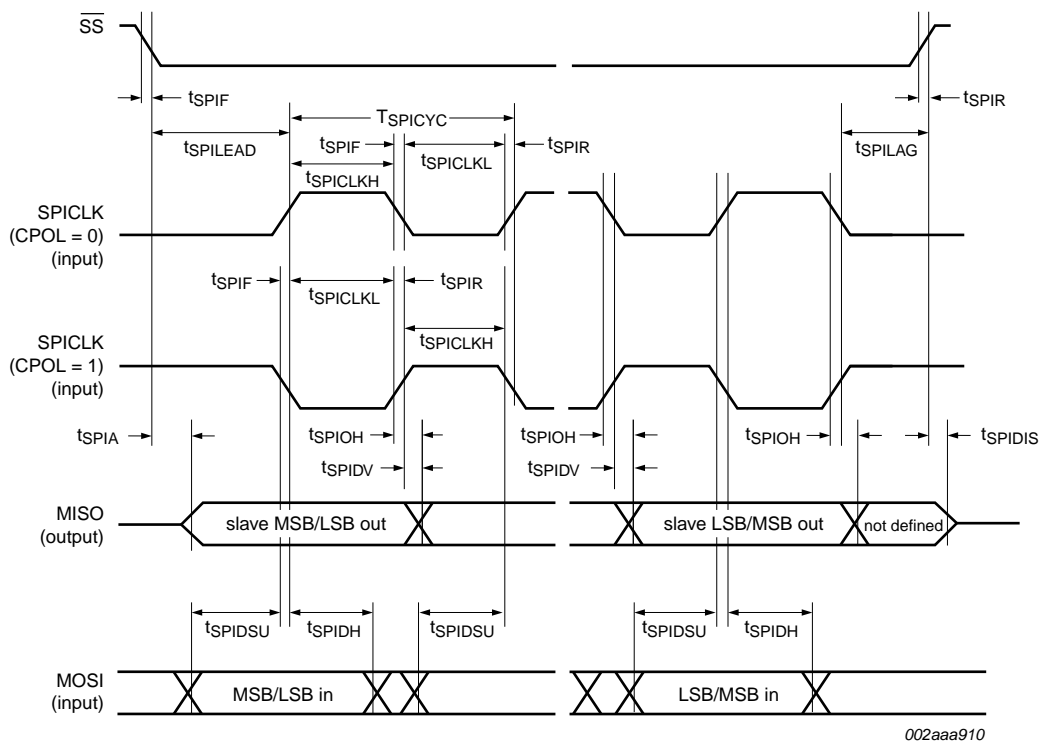


Fig 45. SPI slave timing (CPHA = 0)

12. Other characteristics

12.1 Comparator electrical characteristics

Table 17. Comparator electrical characteristics*V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.**T_{amb} = -40 °C to +85 °C for industrial applications, -40 °C to +125 °C extended, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IO}	input offset voltage		-	-	±10	mV
V _{IC}	common-mode input voltage		0	-	V _{DD} - 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	-50	dB
t _{res(tot)}	total response time		-	250	500	ns
t _(CE-OV)	chip enable to output valid time		-	-	10	µs
I _{LI}	input leakage current	0 V < V _I < V _{DD}	-	-	±1	µA

[1] This parameter is characterized, but not tested in production.