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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5642af2mlu1r

- Calibration support allowing an external tool to modify address mapping

1.5.2 Crossbar switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 4 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
- 4 slave ports
  - Flash
  - Calibration bus interface
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation minimizes overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

VSS	VSS	VSS					VRC33	NC	NC	VDDEH6AB	M
VSS	VSS	VSS					NC	SCI_A_TX	VSS	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							NC	NC	NC	RESET	R
							VSS	BOOTCFG0	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG1	EXTAL	U
							SCI_C_RX	CAN_C_RX	PLLREF	XTAL	V
ETPUA1	EMIOS1	VDDEH4AB	EMIOS8	EMIOS15	EMIOS16	EMIOS23	SCI_C_TX	VDD	CAN_B_RX	VDDPLL	W
ETPUA0	EMIOS2	EMIOS5	EMIOS9	EMIOS14	EMIOS17	EMIOS22	CAN_A_RX	VSS	VDD	CAN_B_TX	Y
EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS18	EMIOS21	VDDEH4AB	WKPCFG	VSS	VDD	AA
TCRCLKA	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS19	EMIOS20	CAN_A_TX	SCI_B_RX	SCI_B_TX	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin TEPBGA package ballmap (southeast, viewed from above)

2.4 Signal summary

Table 3. MPC5642A signal properties

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
GPIO											
FR_A_TX GPIO[12]	FlexRay transmit data channel A GPIO	A1 G	010 000	12	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	P3
FR_A_TX_EN GPIO[13]	FlexRay ch. A tx data enable GPIO	A1 G	010 000	13	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	P4
FR_A_RX GPIO[14]	FlexRay receive data ch. A GPIO	A1 G	010 000	14	I I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R1
FR_B_TX GPIO[15]	FlexRay transmit data ch. B GPIO	A1 G	010 000	15	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R2
FR_B_TX_EN GPIO[16]	FlexRay tx data enable for ch. B GPIO	A1 G	010 000	16	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R4
FR_B_RX GPIO[17]	FlexRay receive data channel B GPIO	A1 G	010 000	17	I I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	T1
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[9]	VDDEH7 / Slow[10]	— / Up	— / Up	143	R4	C14
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[9]	VDDEH7 / Slow	— / Up	— / Up	144	P5	B14
GPIO[219]	GPIO	G	000	219[11]	I/O	VDDEH7 / MultV	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 / Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 / Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF IRQ[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 / Slow	— / Up	PLLREF / Up	83	M14	V21
PLLCFG1[12] IRQ[5] DSPI_D_SOUT GPIO[209]	— External interrupt request DSPI D data output GPIO	— A1 A2 G	— 010 100 000	209	— I O I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	U20
RSTCFG GPIO[210]	RSTCFG GPIO	P G	01 00	210	I I/O	VDDEH6 / Slow	— / Down	—	—	—	P22

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration data bus	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[0]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[1]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A1	01 10	343	O O	VDDE12 / Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[11] / —	—	—	—

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
NEXUS[13]											
$\overline{\text{EVTI}}$	Nexus event in	P	01	231	I	VDDEH7 / MultiV	— / Up	$\overline{\text{EVTI}}$ / Up	116	E15	H20
$\overline{\text{EVTO}}$[14]	Nexus event out	P	01	227	O	VDDEH7 / MultiV	ABR/Up	$\overline{\text{EVTO}}$ / —	120	D15	G20
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 / Fast	—	MCKO / —	14	F15	F1
MDO[0]	Nexus message data out	P	01	220	O	VRC33 / Fast	—	MDO[0] / —	17	A14	F3
MDO[1]	Nexus message data out	P	01	221	O	VRC33 / Fast	—	MDO[1] / —	18	B14	G2
MDO[2]	Nexus message data out	P	01	222	O	VRC33 / Fast	—	MDO[2] / —	19	A13	G3
MDO[3]	Nexus message data out	P	01	223	O	VRC33 / Fast	—	MDO[3] / —	20	B13	G4
MDO[4] ETPUA2_O GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	75	O O I/O	VDDEH7 / MultiV	—	— / —	126	P10	B19
MDO[5] ETPUA4_O GPIO[76]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	76	O O I/O	VDDEH7 / MultiV	—	— / —	129	T10	B20
MDO[6] ETPUA13_O GPIO[77]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	77	O O I/O	VDDEH7 / MultiV	—	— / —	135	T11	C18
MDO[7] ETPUA19_O GPIO[78]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	78	O O I/O	VDDEH7 / MultiV	—	— / —	136	N11	B18
MDO[8] ETPUA21_O GPIO[79]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	79	O O I/O	VDDEH7 / MultiV	—	— / —	137	P11	A18
MDO[9] ETPUA25_O PIO[80]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	80	O O I/O	VDDEH7 / MultiV	—	— / —	139	T7	D18
MDO[10] ETPUA27_O GPIO[81]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	81	O O I/O	VDDEH7 / MultiV	—	— / —	134	R10	A19
MDO[11] ETPUA29_O GPIO[82]	Nexus message data out eTPU A channel (output only) GPIO[82]	P A1 G	01 10 00	82	O O I/O	VDDEH7 / MultiV	—	— / —	124	P9	C19

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AB18
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AA18
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	—	—	Y18
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	80	R11	W18
EMIOS14[15] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	A15
EMIOS15[15] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	D14
Clock Synthesizer											
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 / Analog	—	—	93	P16	V22
EXTAL	Crystal oscillator input	P	01	—	I	VDDEH6 / Analog	—	—	92	N16	U22
CLKOUT	System clock output	P	01	229	O	VDDE12 / Fast	—	CLKOUT	—	—	AB9
ENGCLK	Engineering clock output	P	01	214	O	VDDE12 / Fast	—	ENGCLK	—	T14	W10
Power / Ground											
VDDREG	Voltage regulator supply	—		—	I	5 V	I / —	VDDREG	10	K16	F4
VRCCTL	Voltage regulator control output	—		—	O	—	O / —	VRCCTL	11	N14	F2
VRC33[17]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	B1, M19, P11
	Input for external 3.3 V supply	—		—	I	3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	A4, B11	E3, A6
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	A5, A11	A7, E2
VDDPLL	FMPLL supply voltage	—		—	I	1.2 V	I / —	VDDPLL	91	R16	W22
VSTBY	Power supply for standby RAM	—		—	I	0.9 V – 6 V	I / —	VSTBY	12	C1	E4

[7] See Table 4 for details on pad types.

[8] The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is O (output), I (input), Up (weak pull up enabled), Down (weak pull down enabled), Low (output driven low), High (output driven high). A dash for the function in this column denotes that both the input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.

[9] When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.

[10] Maximum frequency is 50 kHz

[11] PCR219 controls two different pins: MCKO and GPIO[219]. Please refer to Pad Configuration Register 219 section in SIU chapter of device reference manual for details.

[12] On 176 LQFP and 208 MAPBGA packages, this pin is tied low internally.

[13] These pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of this pin once enabled.

[14] The BAM uses this pin to select if auto baud rate is on or off.

[15] Output only

[16] This signal name is used to support legacy naming.

[17] Do not use VRC33 to drive external circuits.

[18] VDDEH1A, VDDEH1B and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[19] VDDEH4, VDDEH4A, VDDEH4B and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[20] VDDEH6, VDDEH6A, VDDEH6B and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[21] VDDEH7, VDDEH7A and VDDE7B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

Table 15. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
5d	Idd3p3	CC	C	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[6]	—	3.090	—	V
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[7]	Lvi3p3 – 6%	Lvi3p3	Lvi3p3 + 6%	V
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[7]	Lvi3p3 – 3%	Lvi3p3	Lvi3p3 + 3%	V
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply[8]	—	2.07	—	V
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r – 35%	Por3.3V_r	Por3.3V_r + 35%	V
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f – 35%	Por3.3V_f	Por3.3V_f + 35%	V
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply	—	4.290	—	V
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset	Lvi5p0 – 6%	Lvi5p0	Lvi5p0 + 6%	V
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset	Lvi5p0 – 3%	Lvi5p0	Lvi5p0 + 3%	V
8c	—	CC	C	Trimming step LVI 5 V	—	20	—	mV
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis	—	60	—	mV
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 35%	V
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 35%	V

1 Using external ballast transistor.

2 Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.

3 LVI for falling supply is calculated as LVI rising – LVI hysteresis.

4 Lvi1p2 tracks DC target variation of internal V_{DD} regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum V_{DD} DC target respectively.

5 With internal load up to Idd3p3

6 The Lvi3p3 specs are also valid for the V_{DDEH} LVI

7 Lvi3p3 tracks DC target variation of internal V_{DD33} regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum V_{DD33} DC target respectively.

[18] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.

[19] Applies to CLKOUT, external bus pins, and Nexus pins

[20] Applies to the FCK, SDI, SDO, and SDS pins

[21] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 21 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 21.

Table 21. I/O pad average I_{DDE} specifications[1]

Pad type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.25	11	9	—
		CC	D	30	50	5.25	01	6.1	—
		CC	D	117	50	5.25	00	2.3	—
		CC	D	212	200	5.25	00	5.8	—
MultiV (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.25	11	3.4	—

[1] Numbers from simulations at best case process, 150 °C

[2] All loads are lumped.

[3] Average current is for pad configured as output only

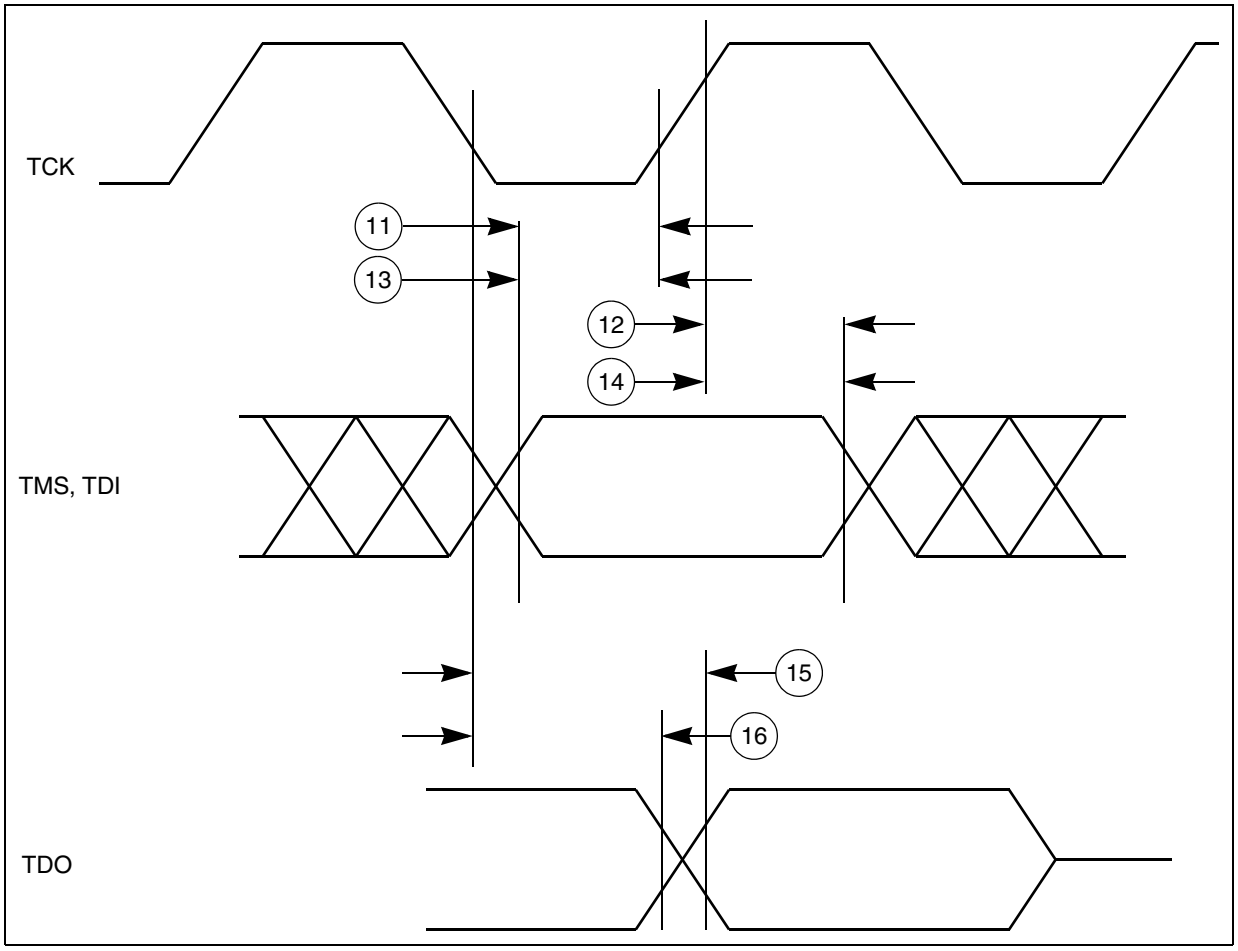

Figure 18. Nexus TDI, TMS, TDO timing

Table 39. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
176 LQFP 208 BGA 324 BGA	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
496 CSP	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
		Route to CAL_MDO[7]	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz[3]

1 NPC_PCR[FPM] = 0

2 NPC_PCR[NEXCFG] = 0

3.17.4 Calibration bus interface timing

Table 40. Calibration bus interface maximum operating frequency

Port width	Multiplexed mode	Pin usage			Max. operating frequency
		CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz[1]
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz[1]
32-bit	Yes	CAL_WE/BE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz[1]

[1] Set SIU_ECCR[EBDF] to either divide by two or divide by four if the system frequency is greater than 66 MHz.

Table 41. Calibration bus operation timing[1]

#	Symbol		C	Characteristic	66 MHz[2]		Unit
					Min	Max	
1	T_C	CC	P	CLKOUT period[3]	15.2	—	ns
2	t_{CDC}	CC	T	CLKOUT duty cycle	45%	55%	T_C
3	t_{CRT}	CC	T	CLKOUT rise time	—	[4]	ns
4	t_{CFT}	CC	T	CLKOUT fall time	—	[4]	ns
5	t_{COH}	CC	P	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.3	—	ns
6	t_{COV}	CC	P	CLKOUT Posedge to Output Signal Valid (Output Delay) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	—	9	ns
7	t_{CIS}	CC	P	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	6.0	—	ns
8	t_{CIH}	CC	P	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns
9	t_{APW}	CC	P	ALE Pulse Width[5]	6.5	—	ns
10	t_{AAI}	CC	P	ALE Negated to Address Invalid[5]	1.5[6]	—	ns

1 Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The calibration bus is limited to half the speed of the internal bus. The maximum calibration bus frequency is 66 MHz. The bus division factor should be set accordingly based on the internal frequency being used.

3 Signals are measured at 50% V_{DDE}

4 Refer to fast pad timing in Table 34 and Table 35 (different values for 1.8 V vs. 3.3 V).

5 Measured at 50% of ALE

6 When CAL_TS pad is used for CAL_ALE function the hold time is 1 ns instead of 1.5 ns.

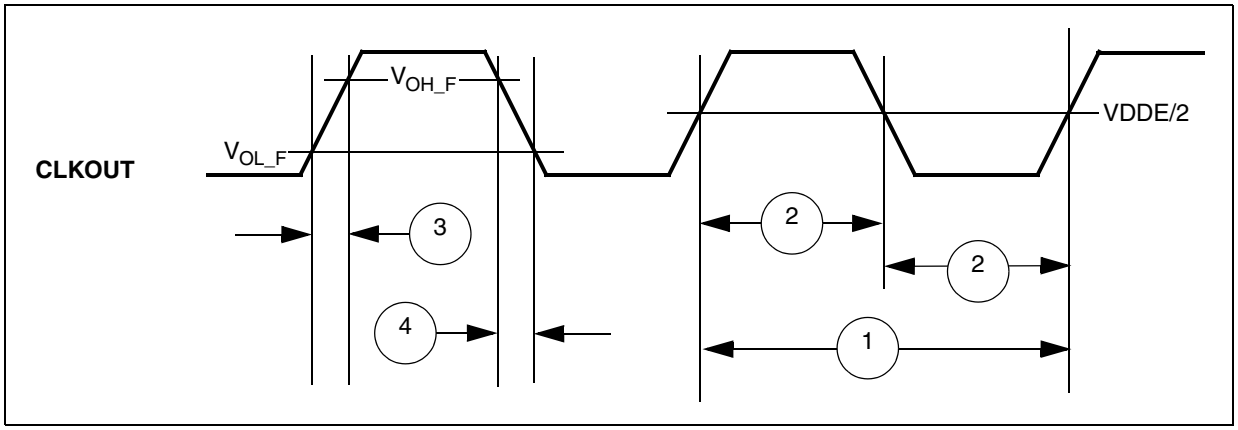

Figure 19. CLKOUT timing

3.17.7 eMIOS timing

Table 44. eMIOS timing[1]

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

[1] eMIOS timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the MPC5642A MCU is shown in Table 45. Timing specifications are in Table 46.

Table 45. DSPI channel frequency support

System clock (MHz)	DSPI Use Mode	Maximum usable frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio
	Non-LVDS	18.75	Use sysclock /8 divide ratio
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR = 0b1 (double baud rate), BR = 0b0000 (scaler value 2) and PBR = 0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio
80	LVDS	40	Use sysclock /2 divide ratio
	Non-LVDS	20	Use sysclock /4 divide ratio

Table 46. DSPI timing[1,2]

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
1	t_{SCK}	CC	D	SCK Cycle Time[3,4,5]		24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay[6]		22[7]	—	ns
3	t_{ASC}	CC	D	After SCK Delay[8]		21[9]	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle		$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)		—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)		—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time		4[10]	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time		5[11]	—	ns

7 Timing met when PCSSCK = 3 (01), and CSSCK = 2 (0000)
8 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9 Timing met when ASC = 2 (0000), and PASC = 3 (01)
10 Timing met when PCSSCK = 3
11 Timing met when ASC = 3
12 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

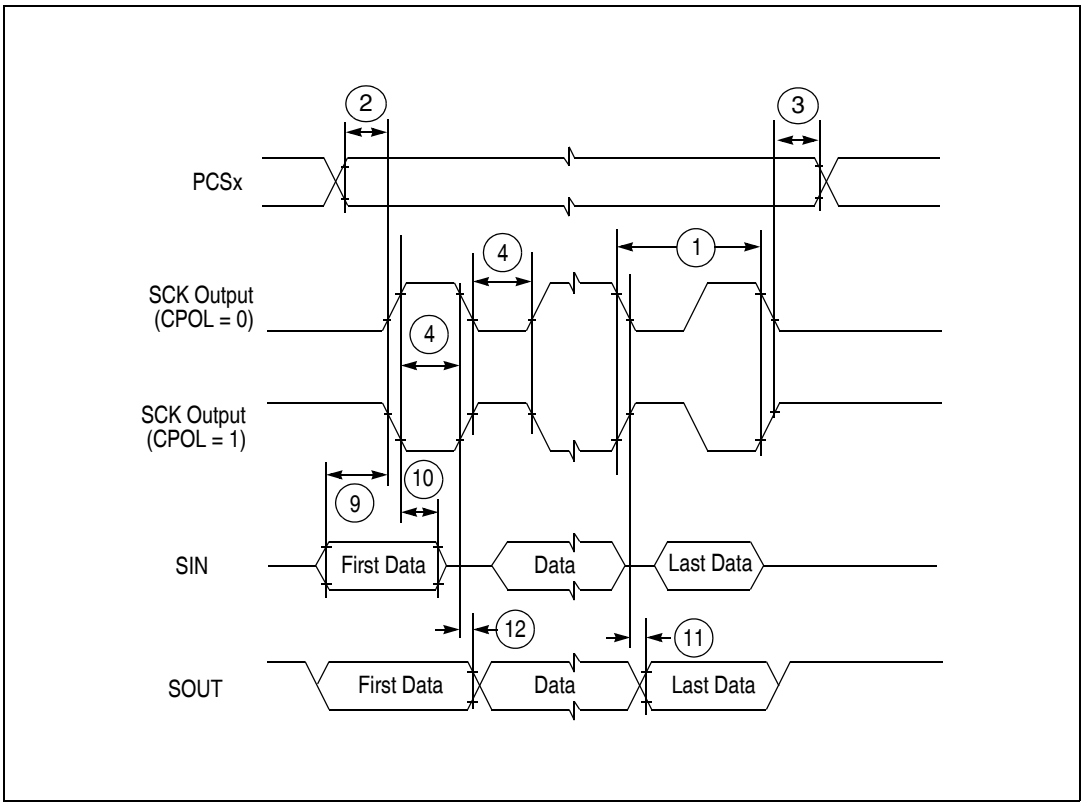

Figure 24. DSPI classic SPI timing (master, CPHA = 0)

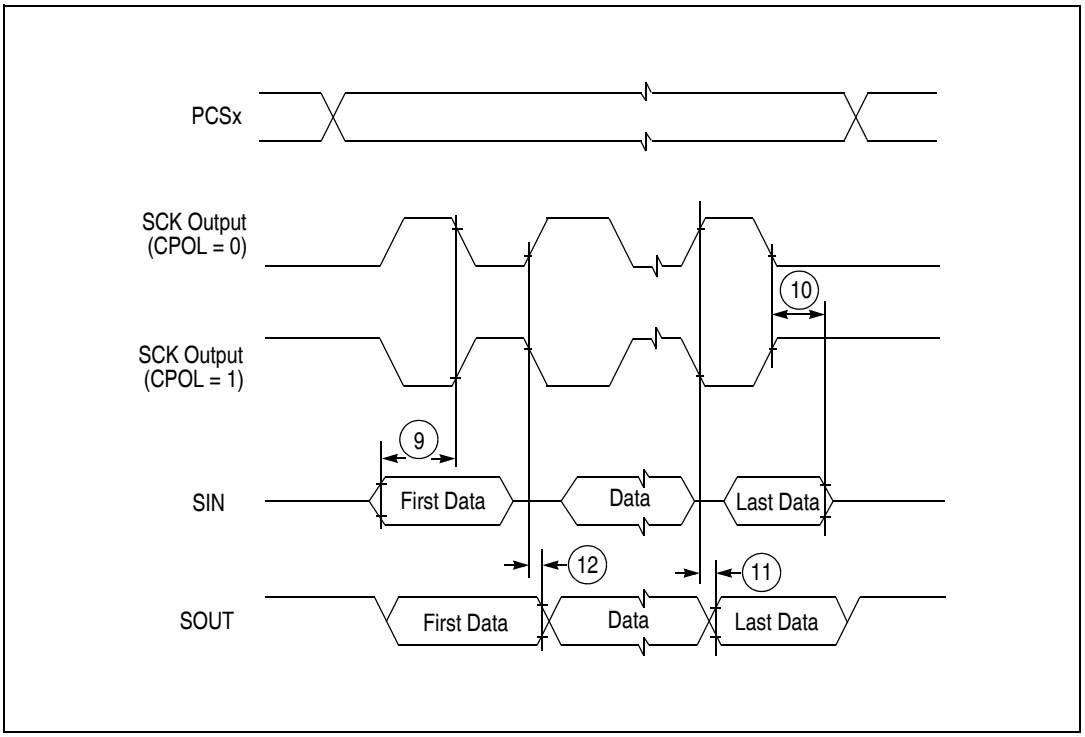

Figure 25. DSPI classic SPI timing (master, CPHA = 1)

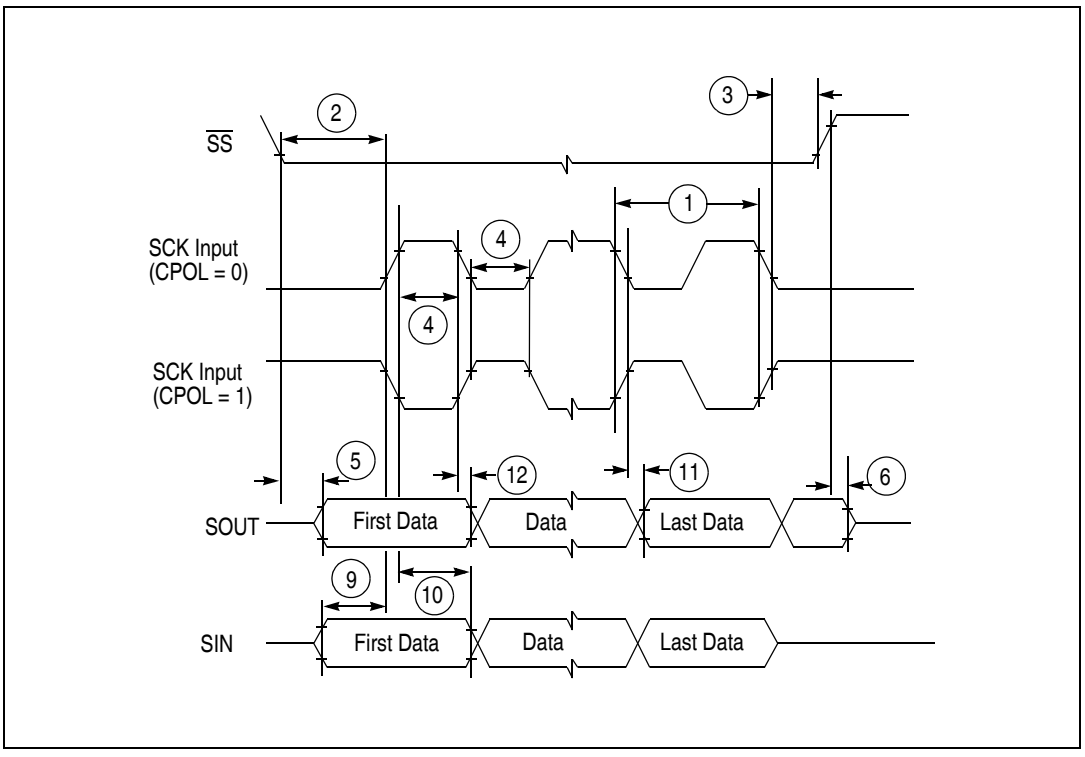

Figure 26. DSPI classic SPI timing (slave, CPHA = 0)

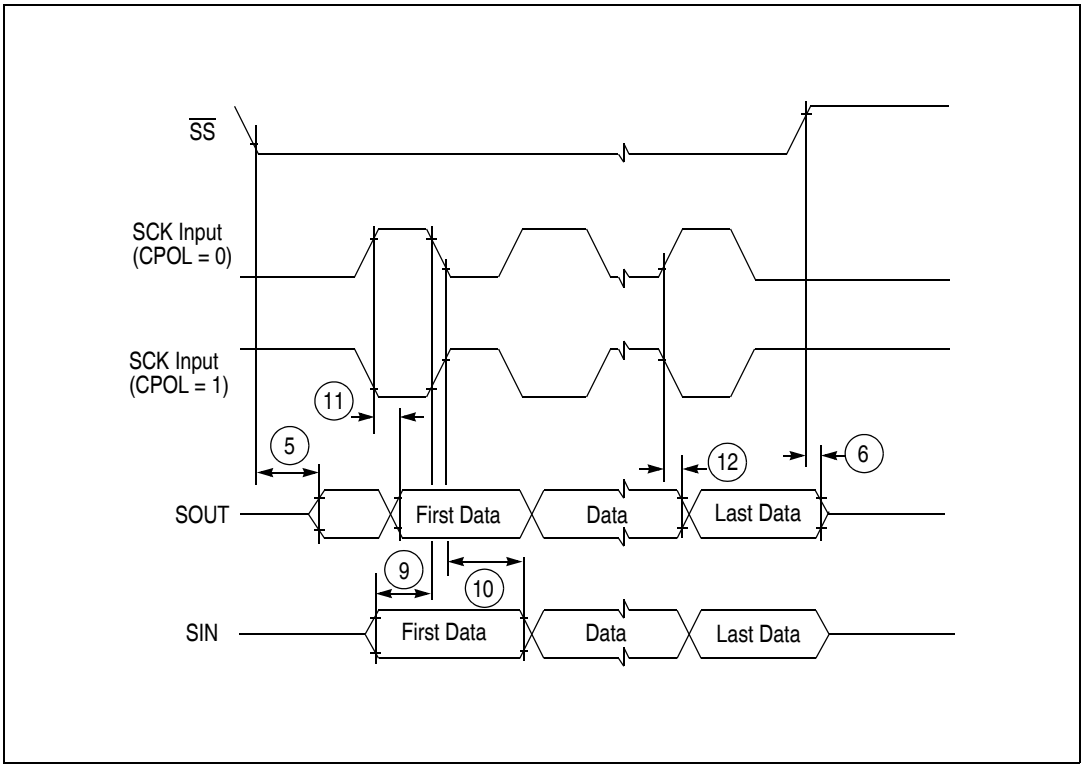

Figure 31. DSPI modified transfer format timing (slave, CPHA = 1)

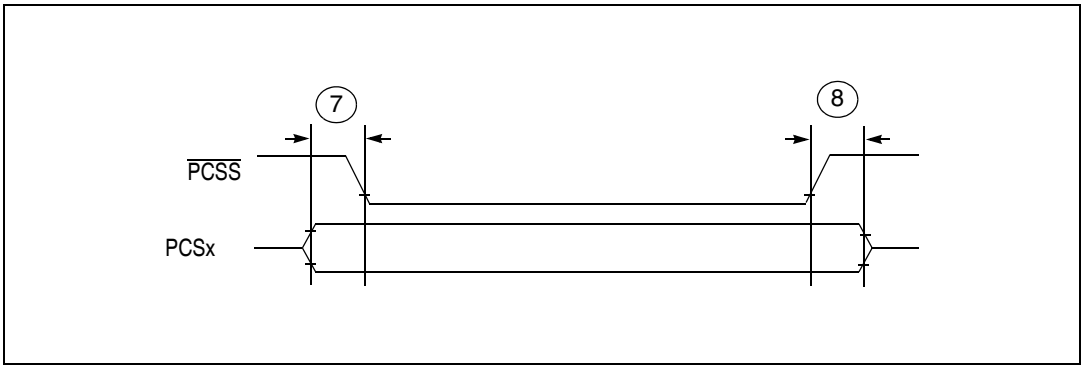

Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

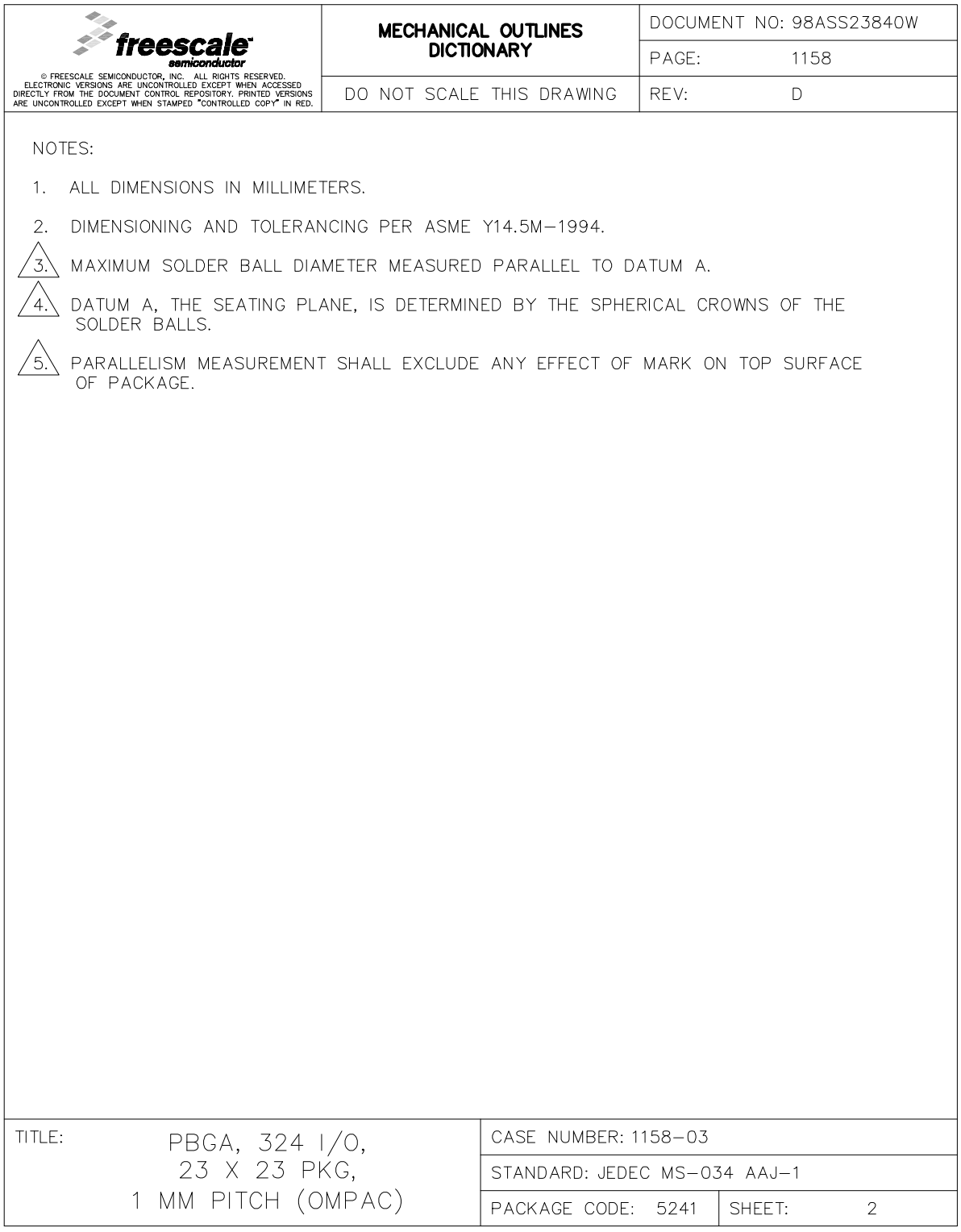

Figure 40. 324 BGA package mechanical drawing (part 2)

Table 51. Revision history (continued)

Date	Revision	Substantive changes
26 Mar 2012	2 (cont'd)	Merged "DSPI timing (V_{DDEH} = 3.0 to 3.6 V)" and "DSPI timing (V_{DDEH} = 4.5 to 5.5V)" tables into Table 46 (DSPI timing) and changed all parameter classification to D Table 47 (eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)) changed all parameter classification to D
04 May 2012	3	Minor editorial changes and improvements throughout. In Section 2.4, Signal summary, Table 3 (MPC5642A signal properties), updated the following properties for the Nexus pins: • Added a footnote to the "Nexus" title for this pin group. • Added a footnote to the "Name" entry for $\overline{\text{EVTO}}$. • Updated the "Status During reset" entry for $\overline{\text{EVTO}}$. In Section 3.2, Maximum ratings, Table 8 (Absolute maximum ratings), removed the "TBD - To be defined" footnote. In Section 3.6, Power management control (PMC) and power on reset (POR) electrical specifications, removed the "Voltage regulator controller (VRC) electrical specifications" subsection. In Section 3.8, DC electrical specifications, Table 20 (DC electrical specifications), removed the "TBD - To be defined" footnote. In Section 3.9, I/O pad current specifications, Table 21 (I/O pad average I_{DDE} specifications): • Updated values and replaced TBDs with numerical data. • Removed the "TBD - To be defined" footnote. In Section 3.9.1, I/O pad V_{RC33} current specifications, Table 22 (I/O pad V_{RC33} average I_{DDE} specifications): • Updated values and replaced TBDs with numerical data. • Removed the "TBD - To be defined" footnote. In Section 3.14, Platform flash controller electrical characteristics, Table 31 (APC, RWSC, WWSC settings vs. frequency of operation), removed the "TBD - To be defined" footnote. In Section 5, Ordering information, Table 50 (Orderable part number summary): • Changed all part numbers from "MPC5642AF0..." to "SPC5642AF2...". • Changed "MPC5642AF0MMG1" to "SC667201MMG1". • Changed "MPC5642AF0MMG2" to "SC667201MMG2". • Changed "MPC5642AF0MMG3" to "SC667201MMG3". In Table 51 (Revision history), removed several erroneous items from the Revision 2 entry.
29 Jun 2012	3.1	No content changes, technical or editorial, were made in this revision. Removed the "preliminary" footers throughout. Changed "Data Sheet: Advance Information" to "Data Sheet: Technical Data" on page 1. Removed the "product under development" disclaimer on page 1.

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