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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5642af2mlu2

Freescale Semiconductor
Datasheet Addendum

MPC5642A_AD
Rev. 1, 12/2014

MPC5642A Microcontroller Datasheet Addendum

This addendum describes corrections to the *MPC5642A Microcontroller Datasheet*, order number MPC5642A. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/powerarchitecture for the latest updates.

The current version available of the *MPC5642A Microcontroller Datasheet* is Revision 3.1.

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freescale™ semiconductor

  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI
  - From a set of eTPU output channels, allows selection of source signals for decimation filter integrators

1.5.8 Flash memory

The MPC5642A provides 2 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support
  - 4-entry 128-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (4 words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is 2 consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC

  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full-featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wakeup on bus activity

1.5.18 FlexRay

The MPC5642A includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
  - Receive message buffer
  - Single-buffered transmit message buffer
  - Double-buffered transmit message buffer (combines two single-buffered message buffers)
- 2 independent receive FIFOs
  - 1 receive FIFO per channel
  - Up to 255 entries for each FIFO
- ECC support

1.5.19 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

1.5.19.1 Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system ‘tick’ signals to the operating system, as well as periodic

triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

1.5.19.2 System timer module (STM)

The STM is designed to implement the software task monitor as defined by AUTOSAR[1]. It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.20 Software watchdog timer (SWT)

The SWT is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

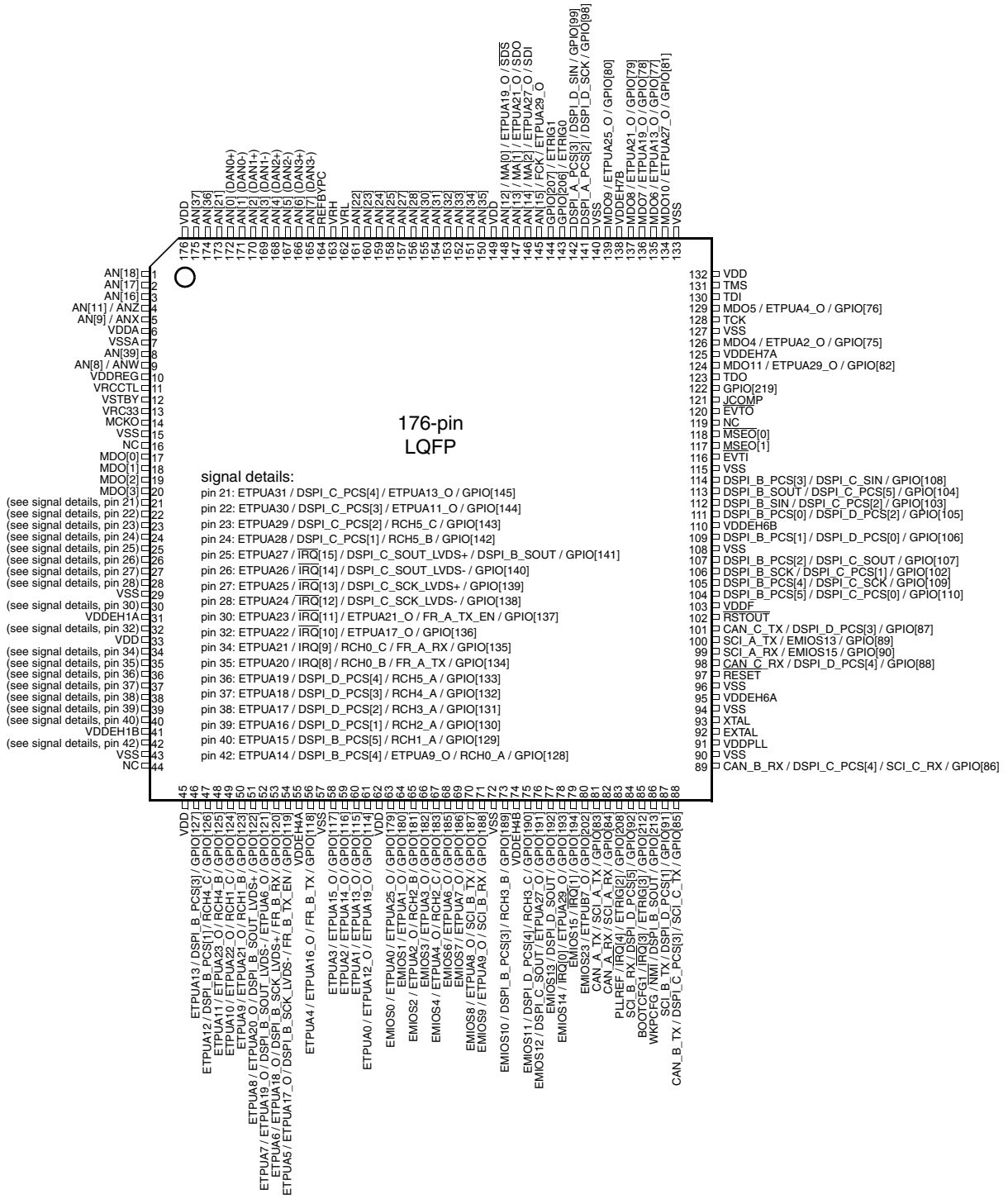
1.5.21 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT ($x25$ protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

1. AUTOSAR: AUTomotive Open System ARchitecture (see http://www.autosar.org)

2.1 176 LQFP pinout



Note: Pin 96 (VSS) should be tied low.

Figure 2. 176-pin LQFP pinout (top view)

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
VDDEH7[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7	—	D12	B22, C21, D15, D20, E19, F19, H19, J14
VDDEH7A[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D17, D19, F21, H21, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, L21, M11, M12, M13, M14, N9, N10, N12, N13, N14, N21, P9, P10, P12, P13, P14, T19, T21, T22, W4, Y3, Y20, AA21, AB1, AB22

1 The suffix "_O" identifies an output-only eTPU channel

2 For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.

3 The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.

4 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

5 Values in the PCR column refer to registers in the System Integration Unit (SIU). The actual register name is "SIU_PCR" suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.

6 The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (–10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/– 10%).

[7] See Table 4 for details on pad types.

[8] The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is O (output), I (input), Up (weak pull up enabled), Down (weak pull down enabled), Low (output driven low), High (output driven high). A dash for the function in this column denotes that both the input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.

[9] When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.

[10] Maximum frequency is 50 kHz

[11] PCR219 controls two different pins: MCKO and GPIO[219]. Please refer to Pad Configuration Register 219 section in SIU chapter of device reference manual for details.

[12] On 176 LQFP and 208 MAPBGA packages, this pin is tied low internally.

[13] These pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of this pin once enabled.

[14] The BAM uses this pin to select if auto baud rate is on or off.

[15] Output only

[16] This signal name is used to support legacy naming.

[17] Do not use VRC33 to drive external circuits.

[18] VDDEH1A, VDDEH1B and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[19] VDDEH4, VDDEH4A, VDDEH4B and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[20] VDDEH6, VDDEH6A, VDDEH6B and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[21] VDDEH7, VDDEH7A and VDDE7B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

Table 5. Signal details (continued)

Signal	Module or function	Description
BOOTCFG[0:1]	SIU – Configuration	Two BOOTCFG signals are implemented in MPC5642A MCUs. The BAM program uses the BOOTCFG0 bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode. See reference manual section “Reset Configuration Half Word (RCHW)” for details on the RCHW. The table “Boot Modes” in reference manual section “BAM Program Operation” defines the boot modes specified by the BOOTCFG1 pin. The following values are for BOOTCFG[0:1}: 00: Boot from internal flash memory 01: FlexCAN/eSCI boot 10: Boot from external memory using calibration bus 11: Reserved Note: For the 176-pin QFP and 208-ball BGA packages BOOTCFG[0] is always 0 since the EBI interface is not available.
WKPCFG	SIU – Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled four clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0: Weak pulldown applied to eTPU and eMIOS pins at reset 1: Weak pullup applied to eTPU and eMIOS pins at reset
ETRIG[2:3]	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[206] ETRIG0 (Input)	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[207] ETRIG1 (Input)	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
IRQ[0:5] IRQ[7:15]	SIU – External Interrupts	The IRQ[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the IRQ[0:15] pins as inputs to the IRQs. See reference manual section “External IRQ Input Select Register (SIU_EIISR)” for more information.
NMI	SIU – External Interrupts	Non-Maskable Interrupt

[6] All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

[7] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[8] AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

[9] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[11] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Lifetime operation at these specification limits is not guaranteed.

[14] Solder profile per IPC/JEDEC J-STD-020D

[15] Moisture sensitivity per JEDEC test method A112

[8] The 3.3V POR specs are also valid for the V_{DDEH} POR

3.6.1 Regulator example

In designs where the MPC5642A microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

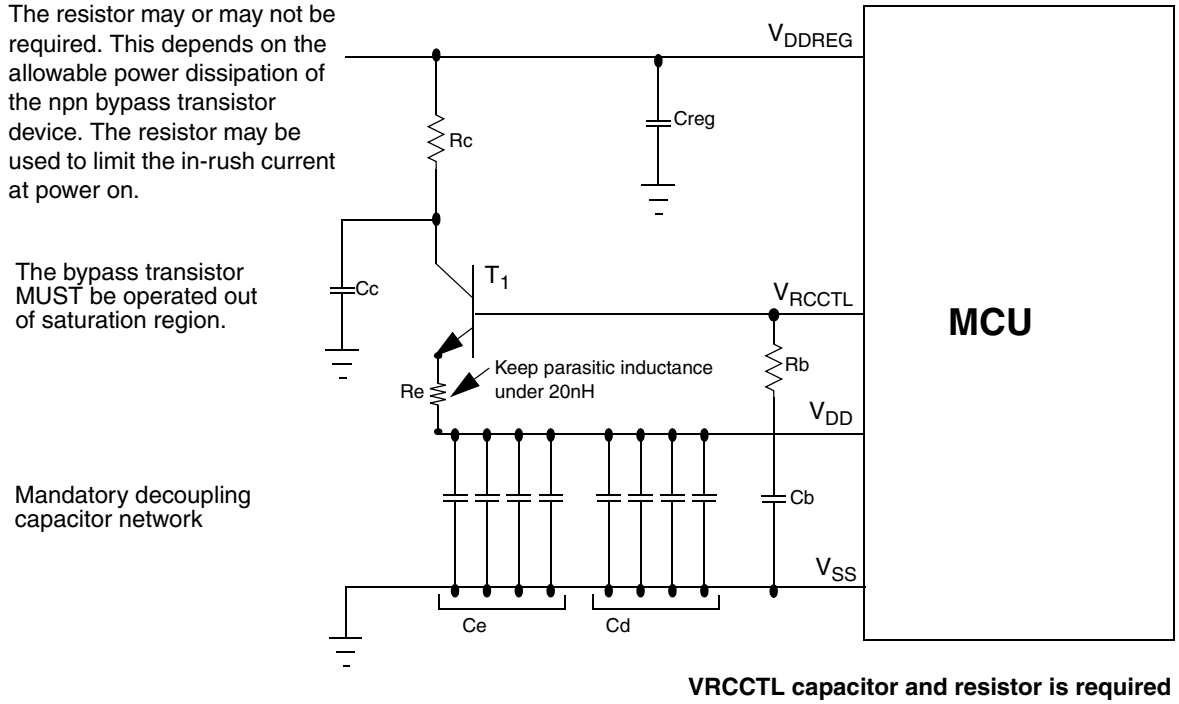


Figure 8. Core voltage regulator controller external components preferred configuration

Table 16. MPC5642A External network specification

External Network Parameter	Min	Typ	Max	Comment
T1	—	—	—	NJD2873 or BCP68 only
Cb	1.1 µF	2.2µF	2.97µF	X7R,-50%/+35%
Ce	3*2.35µF+5µF	3*4.7µF+10µF	3*6.35µF+13.5µF	X7R, -50%/+35%
Equivalent ESR of Ce capacitors	5mΩ	—	50mΩ	—
Cd	4*50nF	4*100nF	4*135nF	X7R, -50%/+35%
Rb	9Ω	10Ω	11Ω	+/-10%

Table 20. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IL_LS}	SR	P	Multi-voltage I/O pad input low voltage in Low-swing-mode[7,8,9,10]	Hysteresis enabled	V_{SS} – 0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.9	
V_{IL_HS}	SR	P	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS} – 0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.4 V_{DDEH}	
V_{IH_S}	SR	P	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{IH_F}	SR	P	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE} + 0.3	
V_{IH_LS}	SR	P	Multi-voltage pad I/O input high voltage in low-swing-mode[7,8,9,10]	Hysteresis enabled	2.5	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDE} + 0.3	
V_{IH_HS}	SR	P	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage[11]	—	—	—	0.2 * V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage[11]	—	—	—	0.2 * V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[7,8,9,10,11]	—	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode[11]	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium I/O output high voltage[11]	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage[11]	—	0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[7,8,9,10,11]	—	2.3	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[11]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	P	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	P	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-swing-mode multi-voltage I/O input hysteresis	Hysteresis enabled	0.25	—	—	v

Table 20. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$I_{DD}+I_{DDPLL}$	CC	P	Operating current 1.2 V supplies	V_{DD} @1.32 V @ 80 MHz	—	—	300	mA
		P		V_{DD} @ 1.32 V @ 120 MHz	—	—	360	mA
		P		V_{DD} @ 1.32 V @ 150 MHz	—	—	400	mA
I_{DDSTBY}	CC	T	Operating current 0.95-1.2 V	V_{STBY} at 55 °C	—	35	100	µA
		T	Operating current 2–5.5 V	V_{STBY} at 55 °C	—	45	110	µA
$I_{DDSTBY27}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 27 °C	—	25	90	µA
		P	Operating current 2-5.5 V	V_{STBY} 27 °C	—	35	100	µA
$I_{DDSTBY150}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 150 °C	—	790	2000	µA
		P	Operating current 2–5.5 V	V_{STBY} at 150 °C	—	760	2000	µA
I_{DDPLL}	CC	P	Operating current 1.2 V supplies	V_{DDPLL}, 80 MHz, V_{DD}=1.2 V	—	—	15	mA
I_{DDSLOW} I_{DDSTOP}	CC	C	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[12]	—	—	191	mA
		C		Stop mode[13]	—	—	190	
I_{DD33}	CC	P	Operating current 3.3 V supplies	V_{RC33}[2]	—	—	60	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies	V_{DDA}	—	—	30.0	mA
		P		Analog reference supply current (transient)	—	—	1.0	
		P		V_{DDREG}	—	—	70[14]	
I_{DDH1} I_{DDH4} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	P	Operating current V_{DDE}[15] supplies	V_{DDEH1}	—	—	See note [15]	mA
		P		V_{DDEH4}	—	—		
		P		V_{DDEH6}	—	—		
		P		V_{DDEH7}	—	—		
		P		V_{DDE7}	—	—		
		P		V_{DDEH9}	—	—		
		P		V_{DDE12}	—	—		

Table 23. V_{RC33} pad average DC current[1]

Pad type	Symbol		C	Period (ns)	Load[2] (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 24. DSPI LVDS pad specification

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
Data rate								
$f_{LVDSCLK}$	CC	D	Data frequency	—	—	50	—	MHz
Driver specifications								
V_{OD}	CC	P	Differential output voltage	SRC = 0b00 or 0b11	150	—	400	mV
	CC	P		SRC = 0b01	90	—	320	
	CC	P		SRC = 0b10	160	—	480	
V_{OC}	CC	P	Common mode voltage (LVDS), VOS	—	1.06	1.2	1.39	V
T_R/T_F	CC	D	Rise/Fall time	—	—	2	—	ns
T_{PLH}	CC	D	Propagation delay (Low to High)	—	—	4	—	ns
T_{PHL}	CC	D	Propagation delay (High to Low)	—	—	4	—	ns
t_{PDSYNC}	CC	D	Delay (H/L), sync mode	—	—	4	—	ns
T_{DZ}	CC	D	Delay, Z to Normal (High/Low)	—	—	500	—	ns

Table 29. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)[5]	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[5]	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1 Applies only to differential channels.

2 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

3 At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4 Guaranteed 10-bit mono tonicity.

5 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 30. Cutoff frequency for additional SRAM wait state

1	SWSC Value
98	0
153	1

1 Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

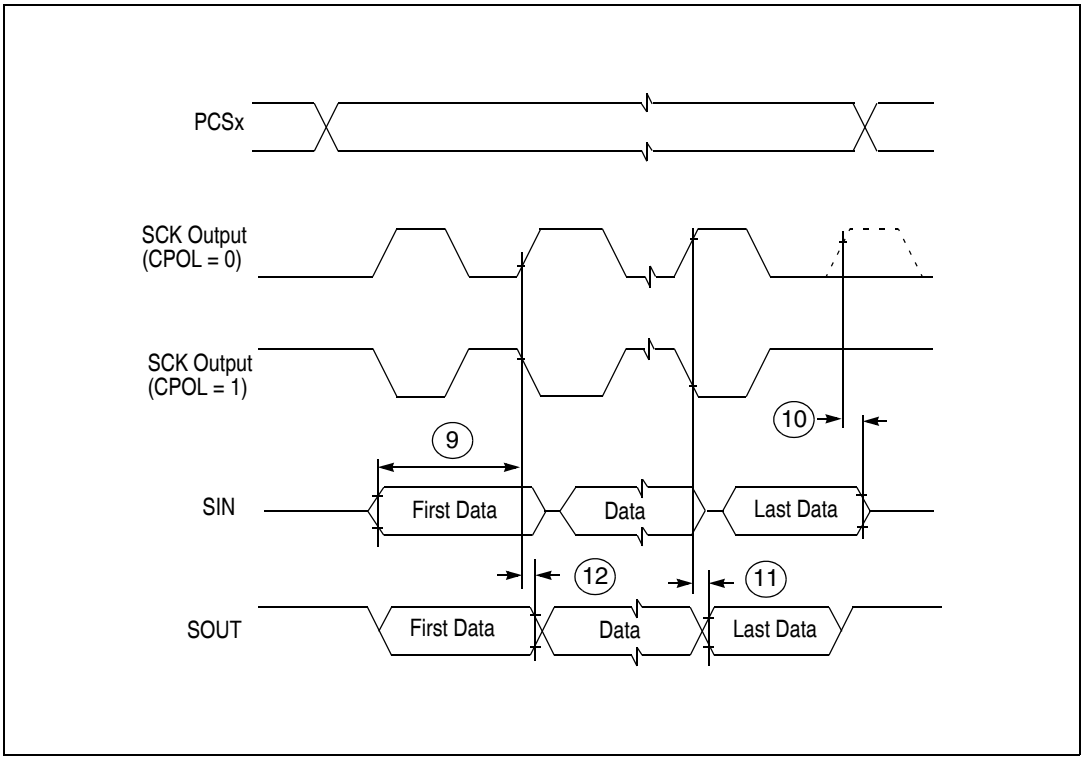


Figure 29. DSPI modified transfer format timing (master, CPHA = 1)

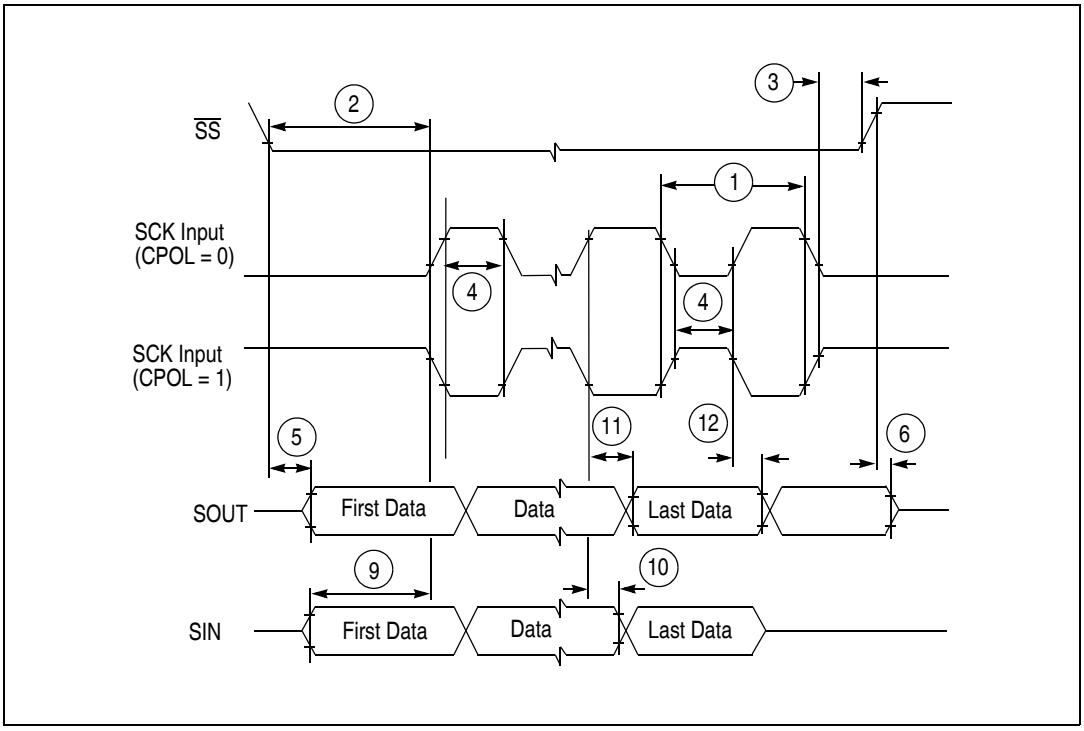


Figure 30. DSPI modified transfer format timing (slave, CPHA = 0)

3.17.9 eQADC SSI timing

Table 47. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Value			Unit
					Min	Typ	Max	
1	f_{FCK}	CC	D	FCK Frequency [2,3]	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} – 6.5		9 * t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} – 6.5		8 * t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT} + t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SSI timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

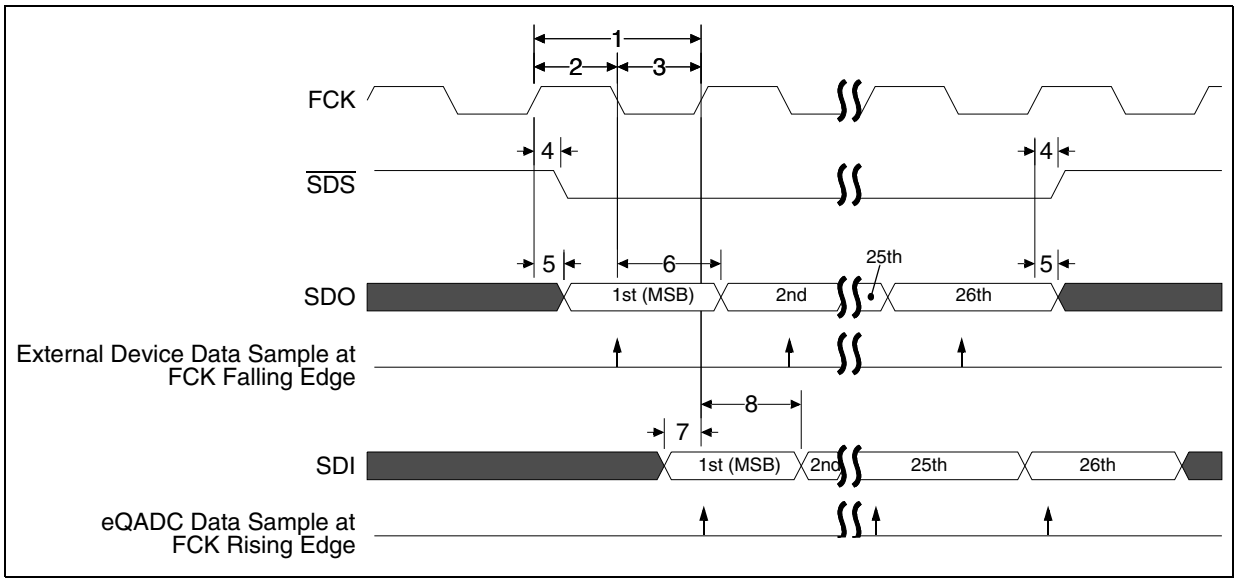


Figure 33. eQADC SSI timing

3.17.10 FlexCAN system clock source

Table 48. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	f_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

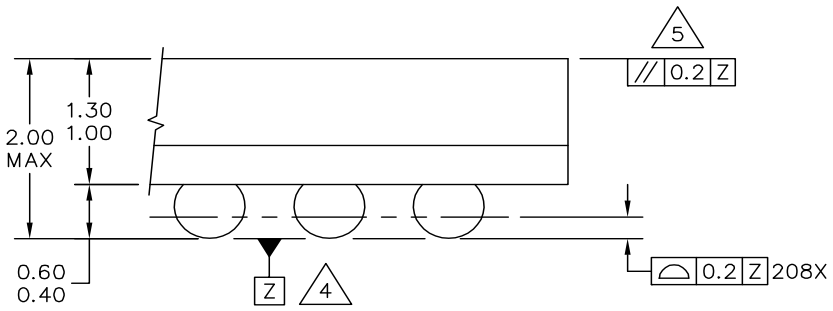
Table 49. FlexCAN engine system clock divider

System frequency	Required SIU_SYSDIV[CAN_SRC] value
$\leq f_{CAN\_TH}$	0[1,2]
$> f_{CAN\_TH}$	1[2,3]

1 Divides system clock source for FlexCAN engine by 1

2 System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1

3 Divides system clock source for FlexCAN engine by 2



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2

Figure 38. 208 MAPBGA package mechanical drawing (part 2)

Table 51. Revision history (continued)

Date	Revision	Substantive changes
26 Mar 2012	2 (cont'd)	Merged "DSPI timing (V_{DDEH} = 3.0 to 3.6 V)" and "DSPI timing (V_{DDEH} = 4.5 to 5.5V)" tables into Table 46 (DSPI timing) and changed all parameter classification to D Table 47 (eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)) changed all parameter classification to D
04 May 2012	3	Minor editorial changes and improvements throughout. In Section 2.4, Signal summary, Table 3 (MPC5642A signal properties), updated the following properties for the Nexus pins: • Added a footnote to the "Nexus" title for this pin group. • Added a footnote to the "Name" entry for $\overline{\text{EVTO}}$. • Updated the "Status During reset" entry for $\overline{\text{EVTO}}$. In Section 3.2, Maximum ratings, Table 8 (Absolute maximum ratings), removed the "TBD - To be defined" footnote. In Section 3.6, Power management control (PMC) and power on reset (POR) electrical specifications, removed the "Voltage regulator controller (VRC) electrical specifications" subsection. In Section 3.8, DC electrical specifications, Table 20 (DC electrical specifications), removed the "TBD - To be defined" footnote. In Section 3.9, I/O pad current specifications, Table 21 (I/O pad average I_{DDE} specifications): • Updated values and replaced TBDs with numerical data. • Removed the "TBD - To be defined" footnote. In Section 3.9.1, I/O pad V_{RC33} current specifications, Table 22 (I/O pad V_{RC33} average I_{DDE} specifications): • Updated values and replaced TBDs with numerical data. • Removed the "TBD - To be defined" footnote. In Section 3.14, Platform flash controller electrical characteristics, Table 31 (APC, RWSC, WWSC settings vs. frequency of operation), removed the "TBD - To be defined" footnote. In Section 5, Ordering information, Table 50 (Orderable part number summary): • Changed all part numbers from "MPC5642AF0..." to "SPC5642AF2...". • Changed "MPC5642AF0MMG1" to "SC667201MMG1". • Changed "MPC5642AF0MMG2" to "SC667201MMG2". • Changed "MPC5642AF0MMG3" to "SC667201MMG3". In Table 51 (Revision history), removed several erroneous items from the Revision 2 entry.
29 Jun 2012	3.1	No content changes, technical or editorial, were made in this revision. Removed the "preliminary" footers throughout. Changed "Data Sheet: Advance Information" to "Data Sheet: Technical Data" on page 1. Removed the "product under development" disclaimer on page 1.