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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5642af2mlu3

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Document Number: MPC5642A_AD
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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5642A series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This microcontroller is a 32-bit system-on-chip (SoC) device intended for use in mid-range engine control and automotive transmission control applications.

It is compatible with devices in Freescale's MPC5600 family and offers performance and capabilities beyond the MPC5632M devices.

The microcontroller's e200z4 host processor core is built on the Power Architecture® technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The device has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by a 128 KB on-chip SRAM and a 2 MB internal flash memory.

For development, the device includes a calibration bus that is accessible only when using the Freescale VertiCal Calibration System.

1.3 Device feature summary

Table 1 summarizes the MPC5642A features and compares them to those of the MPC5644A.

Table 1. MPC5642A device feature summary

Feature		MPC5642A	MPC5644A
Process		90 nm	
Core		e200z4	
	SIMD	Yes	
	VLE	Yes	
	Cache	8 KB instruction	
	Non-Maskable Interrupt (NMI)	NMI and Critical Interrupt	
	MMU	24-entry	
	MPU	16-entry	
	Crossbar switch	4 × 4	5 × 4
	Core performance	0–150 MHz	
Windowing software watchdog		Yes	
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit

Table 1. MPC5642A device feature summary (continued)

Feature	MPC5642A	MPC5644A
CRC	Yes	
FMPLL	Yes	
VRC	Yes	
Supplies	5 V, 3.3 V[2]	
Low-power modes	Stop mode Slow mode	
Packages	176 LQFP[3] 208 MAPBGA[3,4] 324 TEPBGA[5] 496-pin CSP[6]	176 LQFP[3] 208 MAPBGA[3,4] 324 TEPBGA[5] 496-pin CSP[6]

1 197 interrupt vectors are reserved.
2 5 V single supply only for 176 LQFP
3 Pinout compatible with Freescale's MPC5634M devices
4 Pinout compatible with Freescale's MPC5534
5 Ballmap upwardly compatible with the standardized package ballmap used for various Freescale MPC563xM family members
6 For Freescale VertiCal Calibration System only

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5642A series.

  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

VSS	VSS	VSS					VRC33	NC	NC	VDDEH6AB	M
VSS	VSS	VSS					NC	SCI_A_TX	VSS	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							NC	NC	NC	RESET	R
							VSS	BOOTCFG0	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG1	EXTAL	U
							SCI_C_RX	CAN_C_RX	PLLREF	XTAL	V
ETPUA1	EMIOS1	VDDEH4AB	EMIOS8	EMIOS15	EMIOS16	EMIOS23	SCI_C_TX	VDD	CAN_B_RX	VDDPLL	W
ETPUA0	EMIOS2	EMIOS5	EMIOS9	EMIOS14	EMIOS17	EMIOS22	CAN_A_RX	VSS	VDD	CAN_B_TX	Y
EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS18	EMIOS21	VDDEH4AB	WKPCFG	VSS	VDD	AA
TCRCLKA	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS19	EMIOS20	CAN_A_TX	SCI_B_RX	SCI_B_TX	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin TEPBGA package ballmap (southeast, viewed from above)

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
NEXUS[13]											
$\overline{\text{EVTI}}$	Nexus event in	P	01	231	I	VDDEH7 / MultiV	— / Up	$\overline{\text{EVTI}}$ / Up	116	E15	H20
$\overline{\text{EVTO}}$[14]	Nexus event out	P	01	227	O	VDDEH7 / MultiV	ABR/Up	$\overline{\text{EVTO}}$ / —	120	D15	G20
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 / Fast	—	MCKO / —	14	F15	F1
MDO[0]	Nexus message data out	P	01	220	O	VRC33 / Fast	—	MDO[0] / —	17	A14	F3
MDO[1]	Nexus message data out	P	01	221	O	VRC33 / Fast	—	MDO[1] / —	18	B14	G2
MDO[2]	Nexus message data out	P	01	222	O	VRC33 / Fast	—	MDO[2] / —	19	A13	G3
MDO[3]	Nexus message data out	P	01	223	O	VRC33 / Fast	—	MDO[3] / —	20	B13	G4
MDO[4] ETPUA2_O GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	75	O O I/O	VDDEH7 / MultiV	—	— / —	126	P10	B19
MDO[5] ETPUA4_O GPIO[76]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	76	O O I/O	VDDEH7 / MultiV	—	— / —	129	T10	B20
MDO[6] ETPUA13_O GPIO[77]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	77	O O I/O	VDDEH7 / MultiV	—	— / —	135	T11	C18
MDO[7] ETPUA19_O GPIO[78]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	78	O O I/O	VDDEH7 / MultiV	—	— / —	136	N11	B18
MDO[8] ETPUA21_O GPIO[79]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	79	O O I/O	VDDEH7 / MultiV	—	— / —	137	P11	A18
MDO[9] ETPUA25_O PIO[80]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	80	O O I/O	VDDEH7 / MultiV	—	— / —	139	T7	D18
MDO[10] ETPUA27_O GPIO[81]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	81	O O I/O	VDDEH7 / MultiV	—	— / —	134	R10	A19
MDO[11] ETPUA29_O GPIO[82]	Nexus message data out eTPU A channel (output only) GPIO[82]	P A1 G	01 10 00	82	O O I/O	VDDEH7 / MultiV	—	— / —	124	P9	C19

[7] See Table 4 for details on pad types.

[8] The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is O (output), I (input), Up (weak pull up enabled), Down (weak pull down enabled), Low (output driven low), High (output driven high). A dash for the function in this column denotes that both the input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.

[9] When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.

[10] Maximum frequency is 50 kHz

[11] PCR219 controls two different pins: MCKO and GPIO[219]. Please refer to Pad Configuration Register 219 section in SIU chapter of device reference manual for details.

[12] On 176 LQFP and 208 MAPBGA packages, this pin is tied low internally.

[13] These pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of this pin once enabled.

[14] The BAM uses this pin to select if auto baud rate is on or off.

[15] Output only

[16] This signal name is used to support legacy naming.

[17] Do not use VRC33 to drive external circuits.

[18] VDDEH1A, VDDEH1B and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[19] VDDEH4, VDDEH4A, VDDEH4B and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[20] VDDEH6, VDDEH6A, VDDEH6B and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[21] VDDEH7, VDDEH7A and VDDE7B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5642A series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 7 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 7. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 15. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
5d	Idd3p3	CC	C	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[6]	—	3.090	—	V
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[7]	Lvi3p3 – 6%	Lvi3p3	Lvi3p3 + 6%	V
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[7]	Lvi3p3 – 3%	Lvi3p3	Lvi3p3 + 3%	V
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply[8]	—	2.07	—	V
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r – 35%	Por3.3V_r	Por3.3V_r + 35%	V
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f – 35%	Por3.3V_f	Por3.3V_f + 35%	V
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply	—	4.290	—	V
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset	Lvi5p0 – 6%	Lvi5p0	Lvi5p0 + 6%	V
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset	Lvi5p0 – 3%	Lvi5p0	Lvi5p0 + 3%	V
8c	—	CC	C	Trimming step LVI 5 V	—	20	—	mV
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis	—	60	—	mV
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 35%	V
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 35%	V

1 Using external ballast transistor.

2 Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.

3 LVI for falling supply is calculated as LVI rising – LVI hysteresis.

4 Lvi1p2 tracks DC target variation of internal V_{DD} regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum V_{DD} DC target respectively.

5 With internal load up to Idd3p3

6 The Lvi3p3 specs are also valid for the V_{DDEH} LVI

7 Lvi3p3 tracks DC target variation of internal V_{DD33} regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum V_{DD33} DC target respectively.

[8] The 3.3V POR specs are also valid for the V_{DDEH} POR

3.6.1 Regulator example

In designs where the MPC5642A microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

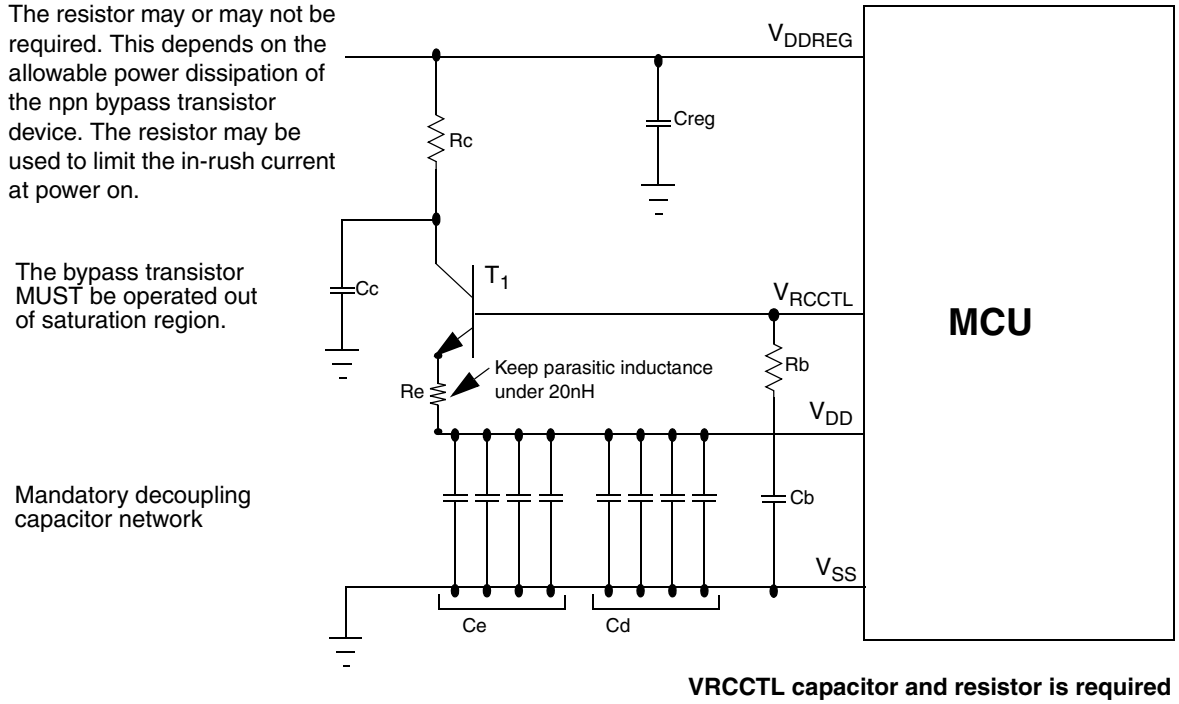

Figure 8. Core voltage regulator controller external components preferred configuration

Table 16. MPC5642A External network specification

External Network Parameter	Min	Typ	Max	Comment
T1	—	—	—	NJD2873 or BCP68 only
Cb	1.1 µF	2.2µF	2.97µF	X7R,-50%/+35%
Ce	3*2.35µF+5µF	3*4.7µF+10µF	3*6.35µF+13.5µF	X7R, -50%/+35%
Equivalent ESR of Ce capacitors	5mΩ	—	50mΩ	—
Cd	4*50nF	4*100nF	4*135nF	X7R, -50%/+35%
Rb	9Ω	10Ω	11Ω	+/-10%

Table 20. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$I_{DD}+I_{DDPLL}$	CC	P	Operating current 1.2 V supplies	V_{DD} @1.32 V @ 80 MHz	—	—	300	mA
		P		V_{DD} @ 1.32 V @ 120 MHz	—	—	360	mA
		P		V_{DD} @ 1.32 V @ 150 MHz	—	—	400	mA
I_{DDSTBY}	CC	T	Operating current 0.95-1.2 V	V_{STBY} at 55 °C	—	35	100	µA
		T	Operating current 2–5.5 V	V_{STBY} at 55 °C	—	45	110	µA
$I_{DDSTBY27}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 27 °C	—	25	90	µA
		P	Operating current 2-5.5 V	V_{STBY} 27 °C	—	35	100	µA
$I_{DDSTBY150}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 150 °C	—	790	2000	µA
		P	Operating current 2–5.5 V	V_{STBY} at 150 °C	—	760	2000	µA
I_{DDPLL}	CC	P	Operating current 1.2 V supplies	V_{DDPLL}, 80 MHz, V_{DD}=1.2 V	—	—	15	mA
I_{DDSLOW} I_{DDSTOP}	CC	C	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[12]	—	—	191	mA
		C		Stop mode[13]	—	—	190	
I_{DD33}	CC	P	Operating current 3.3 V supplies	V_{RC33}[2]	—	—	60	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies	V_{DDA}	—	—	30.0	mA
		P		Analog reference supply current (transient)	—	—	1.0	
		P		V_{DDREG}	—	—	70[14]	
I_{DDH1} I_{DDH4} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	P	Operating current V_{DDE}[15] supplies	V_{DDEH1}	—	—	See note [15]	mA
		P		V_{DDEH4}	—	—		
		P		V_{DDEH6}	—	—		
		P		V_{DDEH7}	—	—		
		P		V_{DDE7}	—	—		
		P		V_{DDEH9}	—	—		
		P		V_{DDE12}	—	—		

Table 20. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{PUPD100K}$	SR	C	Weak pull-up/down resistance[21], 100 kΩ option	—	65	—	140	kΩ
R_{PUPD5K}	SR	C	Weak pull-up/down resistance[21], 5 kΩ option	5 V ± 10% supply	1.4	—	5.2	kΩ
		C		3.3 V ± 10% supply	1.7	—	7.7	
R_{PUPD5K}	SR	C	Weak Pull-Up/Down Resistance[21], 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
$R_{PUPDMTCH}$	CC	C	Pull-up/Down Resistance matching ratios (100K/200K)	Pull-up and pull-down resistances both enabled and settings are equal.	–2.5	—	2.5	%
T_A (T_L to T_H)	SR	P	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	D	Slew rate on power supply pins	—	—	—	25	V/ms

1 These specifications are design targets and subject to change per device characterization.

2 These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).

3 ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no undesirable behavior, but the accuracy will be degraded.

4 The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.

5 V_{FLASH} is available in the calibration package only.

6 Regulator is functional, with derated performance, with supply voltage down to 4.0 V

7 Multi-voltage power supply cannot be below 4.5 V when in low-swing mode

8 The slew rate (SRC) setting must be 0b11 when in low-swing mode.

9 While in low-swing mode there are no restrictions in transitioning to high-swing mode.

10 Pin in low-swing mode can accept a 5 V input

11 All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where otherwise noted

12 Bypass mode, system clock @ 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels @ 1 kHz, all other modules stopped.

13 Bypass mode, system clock @ 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped

14 If 1.2V and 3.3V internal regulators are on,then iddreg=70mA

If supply is external that is 3.3V internal regulator is off, then iddreg=15mA

15 Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 21 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

16 Absolute value of current, measured at V_{IL} and V_{IH}

17 Weak pull-up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to all digital pad types.

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 22 based on the voltage, frequency, and load on all fast pins. The input pin V_{RC33} current can be calculated from Table 22 based on the voltage, frequency, and load on all medium pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 22.

Table 22. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad type	Symbol		C	Period (ns)	Load[2] (pF)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV[4] (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	33.7

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3 Average current is for pad configured as output only

4 In low swing mode, multi-voltage pads must operate in highest slew rate setting, ipp_sre0 = 1, ipp_sre1 = 1.

3.14 Platform flash controller electrical characteristics

Table 31. APC, RWSC, WWSC settings vs. frequency of operation[1]

Max. Flash Operating Frequency (MHz)[2]	APC[3]	RWSC[3]	WWSC
20 MHz	0b000	0b000	0b01
61 MHz	0b001	0b001	0b01
90 MHz	0b010	0b010	0b01
123 MHz	0b011	0b011	0b01
153 MHz	0b100	0b100	0b01

1 APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.

2 Max frequencies including 2% PLL FM.

3 APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 32. Flash program and erase specifications[1]

#	Symbol		C	Parameter	Value				Unit
					Min	Typ	Initial max[2]	Max[3]	
1	$T_{dwprogram}$	CC	C	Double Word (64 bits) Program Time	—	30	—	500	µs
2	$T_{pprogram}$	CC	C	Page Program Time[4]	—	40	160	500	µs
3	$T_{16kpperase}$	CC	C	16 KB Block Pre-program and Erase Time	—	250	1,000	5,000	ms
5	$T_{64kpperase}$	CC	C	64 KB Block Pre-program and Erase Time	—	450	1,800	5,000	ms
6	$T_{128kpperase}$	CC	C	128 KB Block Pre-program and Erase Time	—	800	2,600	7,500	ms
7	$T_{256kpperase}$	CC	C	256 KB Block Pre-program and Erase Time	—	1,400	5,200	15,000	ms
8	T_{psrt}	SR	—	Program suspend request rate[5]	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate [6]	10				ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Page size is 128 bits (4 words)

5 Time between program suspend resume and the next program suspend request.

6 Time between erase suspend resume and the next erase suspend request.

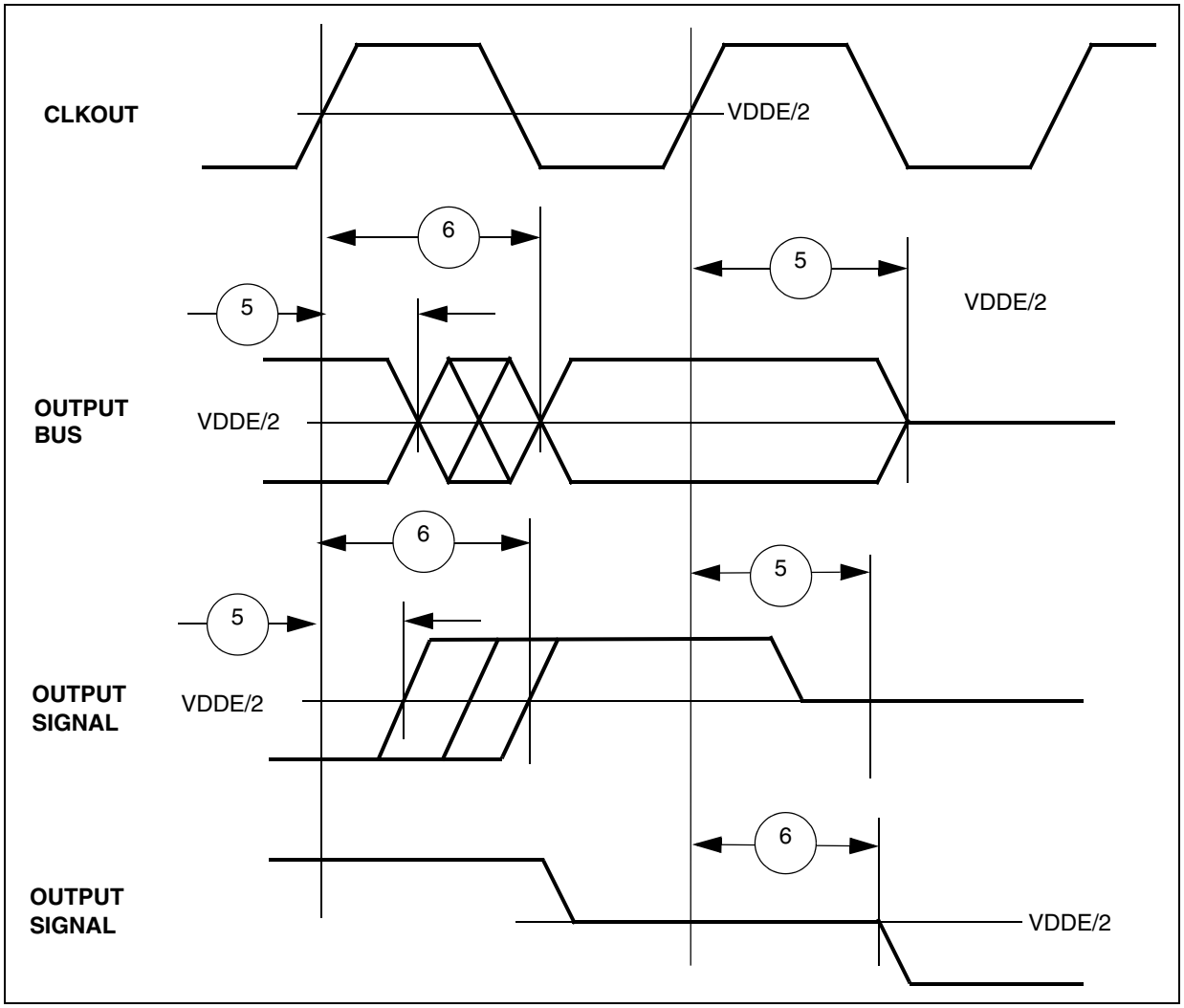

Figure 20. Synchronous output timing

3.17.5 External interrupt timing (IRQ pin)

Table 42. External interrupt timing[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{IPWL}	IRQ Pulse Width Low	3	—	t_{CYC}
2	t_{IPWH}	IRQ Pulse Width High	3	—	t_{CYC}
3	t_{ICYC}	IRQ Edge to Edge Time[2]	6	—	t_{CYC}

1 IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

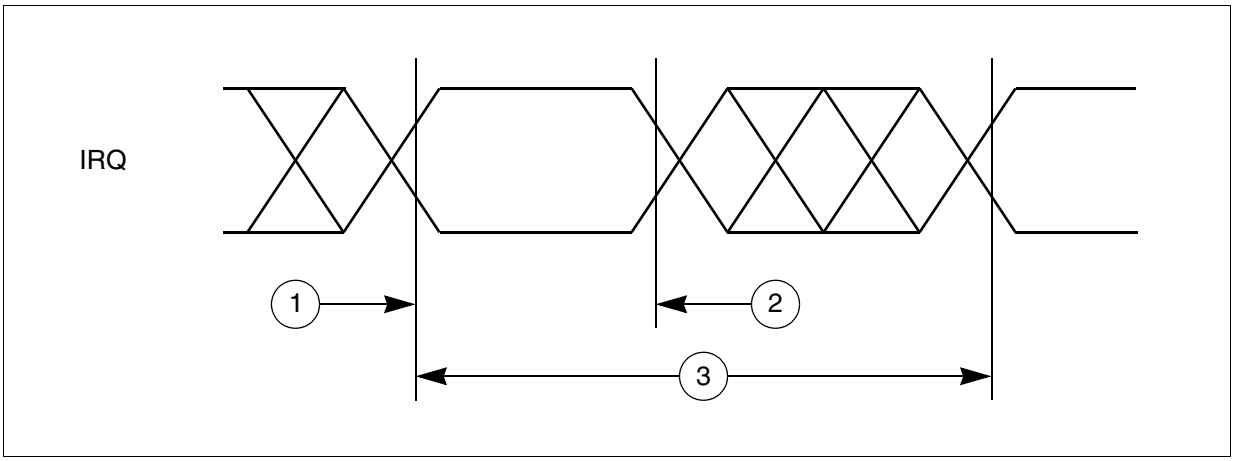

Figure 23. External interrupt timing

3.17.6 eTPU timing

Table 43. eTPU timing[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{ICPW}	eTPU Input Channel Pulse Width	4	—	t_{CYC}
2	t_{OCPW}	eTPU Output Channel Pulse Width[2]	2	—	t_{CYC}

1 eTPU timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

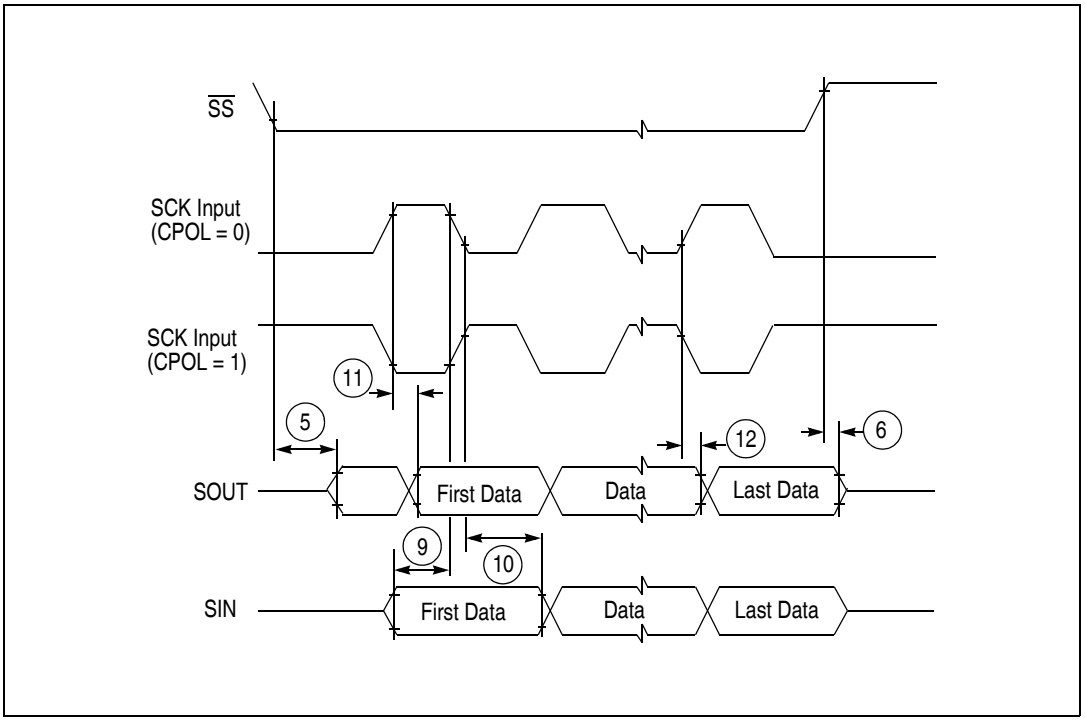

Figure 27. DSPI classic SPI timing (slave, CPHA = 1)

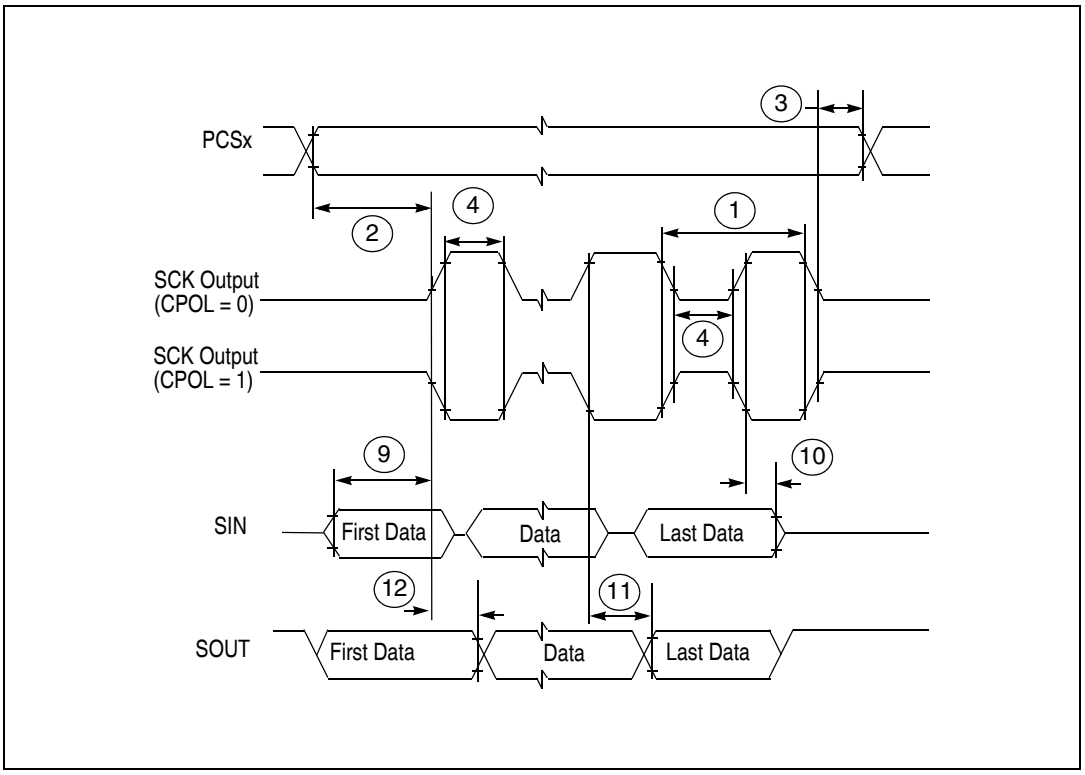

Figure 28. DSPI modified transfer format timing (master, CPHA = 0)

3.17.10 FlexCAN system clock source

Table 48. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	f_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 49. FlexCAN engine system clock divider

System frequency	Required SIU_SYSDIV[CAN_SRC] value
$\leq f_{CAN\_TH}$	0[1,2]
$> f_{CAN\_TH}$	1[2,3]

1 Divides system clock source for FlexCAN engine by 1

2 System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1

3 Divides system clock source for FlexCAN engine by 2

4 Packages

4.1 Package mechanical data

4.1.1 176 LQFP