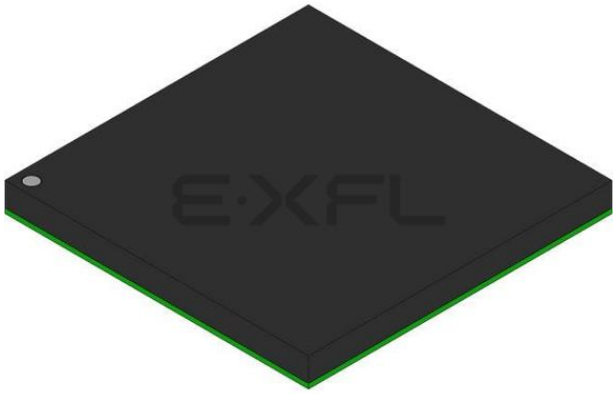

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5642af2mvz1

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Table 2. MPC5642A series block summary

Block	Function
Boot assist module (BAM)	Block of read-only memory containing executable code that searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM
Calibration bus interface	Transfers data across the crossbar switch to/from peripherals attached to the calibration system connector
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Crossbar switch (XBAR)	Internal busmaster
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
e200z4 core	Executes programs and interrupt handlers
Enhanced direct memory access (eDMA)	Performs complex data movements with minimal intervention from the core.
Enhanced modular input-output system (eMIOS)	Provides the functionality to generate or measure events
Enhanced queued analog-to-digital converter (eQADC)	Provides accurate and fast conversions for a wide range of applications
Enhanced serial communication interface (eSCI)	Provides asynchronous serial communication capability with peripheral devices and other microcontroller units
Enhanced time processor unit (eTPU2)	Second-generation co-processor processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
Error Correction Status Module (ECSM)	The Error Correction Status Module supports a number of miscellaneous control functions for the platform, and includes registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
Flash memory	Provides storage for program code, constants, and variables
FlexRay	Provides high-speed distributed control for advanced automotive applications
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
Memory protection unit (MPU)	Provides hardware access control for all memory references generated
Nexus port controller (NPC)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2010 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Reaction Module (REACM)	Works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

Table 2. MPC5642A series block summary (continued)

Block	Function
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer
System watchdog timer (SWT)	Provides protection from runaway code
Temperature sensor	Provides the temperature of the device as an analog value

2.2 208 MAP BGA ballmap

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS[3]	DSPI_B_SIN	DSPI_B_ PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_ PCS[4]	DSPI_B_ PCS[2]	DSPI_B_ PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_ SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ ETPUA29_O	MDO4_ ETPUA2_O	MDO8_ ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P
R	NC	VSS	VDD	GPIO[206]	EMIOS4	EMIOS3	EMIOS9	EMIOS11	EMIOS14	MDO10_ ETPUA27_O	EMIOS23	CAN_A_RX	CAN_B_RX	VDD	VSS	VDDPLL	R
T	VSS	VDD	NC	EMIOS0	EMIOS1	GPIO[219]	MDO9_ ETPUA25_O	EMIOS13	EMIOS15	MDO5_ ETPUA4_O	MDO6_ ETPUA13_O	CAN_B_TX	VDDE12	ENGCLK	VDD	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. 208-pin MAPBGA package ballmap (viewed from above)

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
DSPI_A_PCS[5][16] DSPI_B_PCS[3] GPIO[101]	— DSPI B peripheral chip select GPIO	— A1 G	— 10 00	101	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	A16
DSPI_B_SCK DSPI_C_PCS[1] GPIO[102]	SPI clock pin for DSPI module DSPI B peripheral chip select GPIO	P A1 G	01 10 00	102	I/O O I/O	VDDEH6 / Medium	— / Up	— / Up	106	J16	K21
DSPI_B_SIN DSPI_C_PCS[2] GPIO[103]	DSPI B data input DSPI C peripheral chip select GPIO	P A1 G	01 10 00	103	I O I/O	VDDEH6 / Medium	— / Up	— / Up	112	G15	H22
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 / Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 / Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	109	H16	J22
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 / Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 / Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0 DAN0+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[0] / —	172	B5	C6
AN1 DAN0–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[1] / —	171	A6	C7
AN2 DAN1+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[2] / —	170	D6	D7

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
AN3 DAN1–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[3] / —	169	C7	D8
AN4 DAN2+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[4] / —	168	B6	B7
AN5 DAN2–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[5] / —	167	A7	B8
AN6 DAN3+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[6] / —	166	D7	C8
AN7 DAN3–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[7] / —	165	C8	C9
AN8 ANW	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[8] / —	9	B3	E1
AN9 ANX	Single-ended Analog Input External Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[9] / —	5	A2	C2
AN10 ANY	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[10] / —	—	—	D1
AN11 ANZ	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[11] / —	4	A3	C1
AN12 - SDS MA0 ETPUA19_O $\overline{SDS}$	Single-ended Analog Input MUX Address 0 eTPU A channel (output only) eQADC Serial Data Select	P A1 A2 G	001 010 100 000	215	I O O I/O	VDDEH7 / Medium	I / —	AN[12] / —	148	A12	C13
AN13 - SDO MA1 ETPUA21_O SDO	Single-ended Analog Input MUX Address 1 eTPU A channel (output only) eQADC Serial Data Out	P A1 A2 G	001 010 100 000	216	I O O O	VDDEH7 / Medium	I / —	AN[13] / —	147	B12	B13
AN14 - SDI MA2 ETPUA27_O SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7 / Medium	I / —	AN[14] / —	146	C12	A13
AN15 - FCK FCK ETPUA29_O	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7 / Medium	I / —	AN[15] / —	145	C13	A14
AN16	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[16] / —	3	C6	A3
AN17	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[17] / —	2	C4	A4

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
AN37	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[37] / —	175	E3	A5
AN38	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[38] / —	—	—	D3
AN39	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[39] / —	8	D2	D2
VRH	Voltage Reference High	P	—	—	I	VDDA / —	I / —	—	163	A8	A10
VRL	Voltage Reference Low	P	—	—	I	VDDA / —	I / —	—	162	A9	A11
REFBYBC	Reference Bypass Capacitor Input	P	—	—	I	VDDA / Analog	I / —	—	164	B7	B10
eTPU2											
TCRCLKA IRQ[7] GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A1 G	01 10 00	113	I I I/O	VDDEH4 / Slow	— / Up	— / Up	—	L4	AB12
ETPUA0 ETPUA12_O ETPUA19_O GPIO[114]	eTPU A channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	114	I/O O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	61	N3	Y12
ETPUA1 ETPUA13_O GPIO[115]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	115	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	60	M3	W12
ETPUA2 ETPUA14_O GPIO[116]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	116	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	59	P2	AA11
ETPUA3 ETPUA15_O GPIO[117]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	117	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	GPIO / WKPCFG	58	P1	Y11
ETPUA4 ETPUA16_O — FR_B_TX GPIO[118]	eTPU A channel eTPU A channel (output only) — FlexRay transmit data channel B GPIO	P A1 A2 A3 G	0001 0010 — 1000 0000	118	I/O O — O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	56	N2	W11
ETPUA5 ETPUA17_O DSPI_B_SCK_LVDS– FR_B_TX_EN GPIO[119]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI clock FlexRay tx data enable for ch. B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	119	I/O O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	54	M4	AB11

Table 4. Pad types

Pad Type	Name	I/O Voltage Range
Slow	pad_ssr_hv	3.0V - 5.5 V
Medium	pad_msr_hv	3.0 V - 5.5 V
Fast	pad_fc	3.0 V - 3.6 V
MultiV[1,2]	pad_multv_hv	3.0 V - 5.5 V (high swing mode) 3.0 V - 3.6 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.5 V
LVDS	pad_lo_lv	—

1 Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.

2 VDDEH7 supply cannot be below 4.5 V when in low-swing mode.

2.5 Signal details

Table 5. Signal details

Signal	Module or function	Description
CLKOUT	Clock Generation	MPC5642A clock output for the calibration bus interface
ENGCLK	Clock Generation	Clock for external ASIC devices
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset
PLLREF	Clock Generation Reset/Configuration	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF = 0 selects external reference mode. On the 324 TEPBGA package, PLLREF is bonded to the ball used for PLLCFG[0] for compatibility with MPC55xx devices. For the 176-pin QFP and 208-ball BGA packages: 0: External reference clock is selected 1: XTAL oscillator mode is selected For the 324-ball BGA package: If RSTCFG is 0: 0: External reference clock is selected 1: XTAL oscillator mode is selected If RSTCFG is 1, XTAL oscillator mode is selected.
XTAL	Clock Generation	Crystal oscillator input
DSPI_B_SCK_LVDS– DSPI_B_SCK_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_B_SOUT_LVDS– DSPI_B_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission

Table 5. Signal details (continued)

Signal	Module or function	Description
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base
CAN_A_TX CAN_B_TX CAN_C_TX	FlexCAN_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_B_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
FR_A_RX FR_B_RX	FlexRay	FlexRay receive (Channels A, B)
FR_A_TX_EN FR_B_TX_EN	FlexRay	FlexRay transmit enable (Channels A, B)
FR_A_TX FR_B_TX	FlexRay	FlexRay transmit (Channels A, B)
JCOMP	JTAG	Enables the JTAG TAP controller
TCK	JTAG	Clock input for the on-chip test logic
TDI	JTAG	Serial test instruction and data input for the on-chip test logic
TDO	JTAG	Serial test data output for the on-chip test logic
TMS	JTAG	Controls test mode operations for the on-chip test logic
$\overline{\text{EVTI}}$	Nexus	$\overline{\text{EVTI}}$ is an input that is read on the negation of $\overline{\text{RESET}}$ to enable or disable the Nexus Debug port. After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program synchronization messages or generate a breakpoint.
$\overline{\text{EVTO}}$	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and $\overline{\text{MSEO}}$ signals.
MDO[0:11]	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
$\overline{\text{MSEO}}$[0:1]	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
RDY	Nexus	Nexus Ready Output (RDY)—Indicates to the development tools that data is ready to be read from or written to the Nexus read/write access registers.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 324-pin TEPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Single-layer board – 1s	29	°C/W
	CC	D		Four-layer board – 2s2p	19	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient[2]	at 200 ft./min., single-layer board – 1s	23	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	16	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]		10	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case[4]		7	°C/W
Ψ_{JT}	CC	D	Junction-to-package top, natural convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 22 based on the voltage, frequency, and load on all fast pins. The input pin V_{RC33} current can be calculated from Table 22 based on the voltage, frequency, and load on all medium pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 22.

Table 22. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad type	Symbol		C	Period (ns)	Load[2] (pF)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV[4] (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	33.7

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3 Average current is for pad configured as output only

4 In low swing mode, multi-voltage pads must operate in highest slew rate setting, ipp_sre0 = 1, ipp_sre1 = 1.

Table 29. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)[5]	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[5]	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1 Applies only to differential channels.

2 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

3 At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4 Guaranteed 10-bit mono tonicity.

5 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 30. Cutoff frequency for additional SRAM wait state

1	SWSC Value
98	0
153	1

1 Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

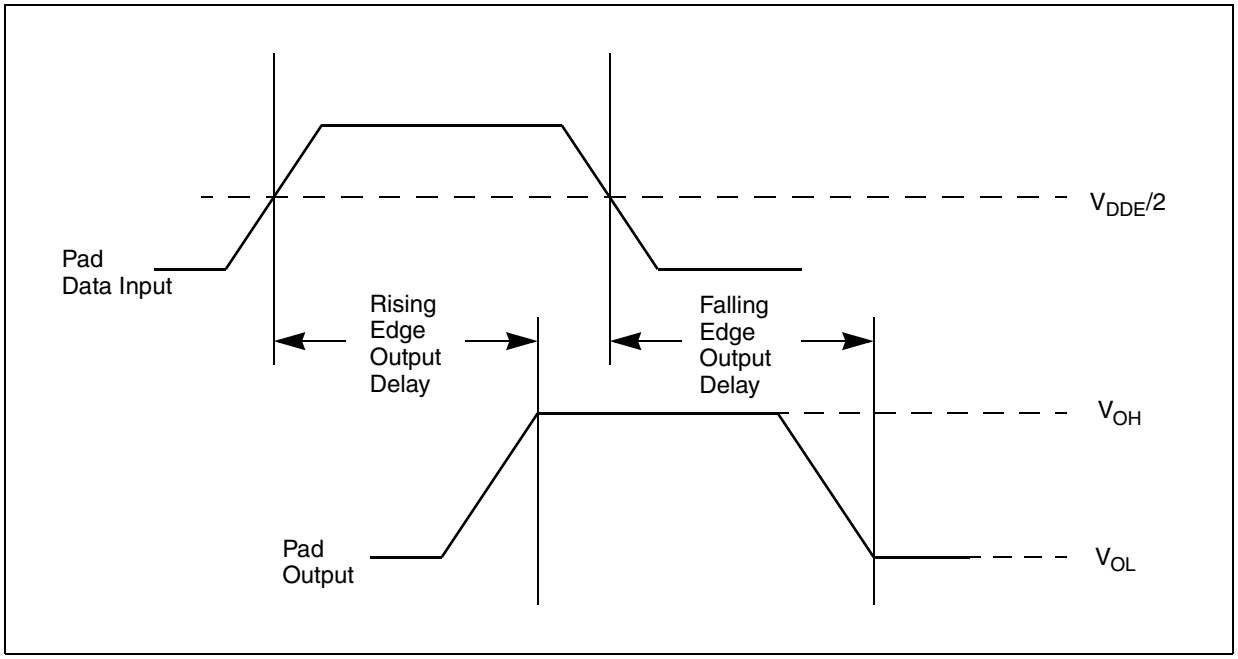


Figure 10. Pad output delay—Slew rate controlled fast, medium, and slow pads

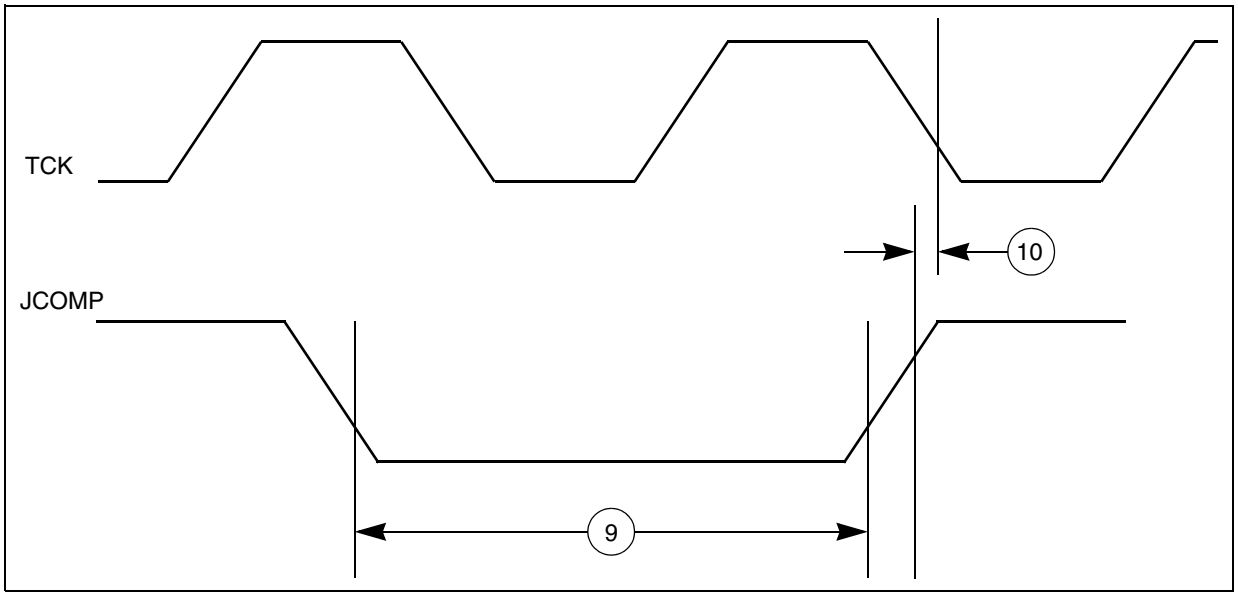


Figure 14. JTAG JCOMP timing

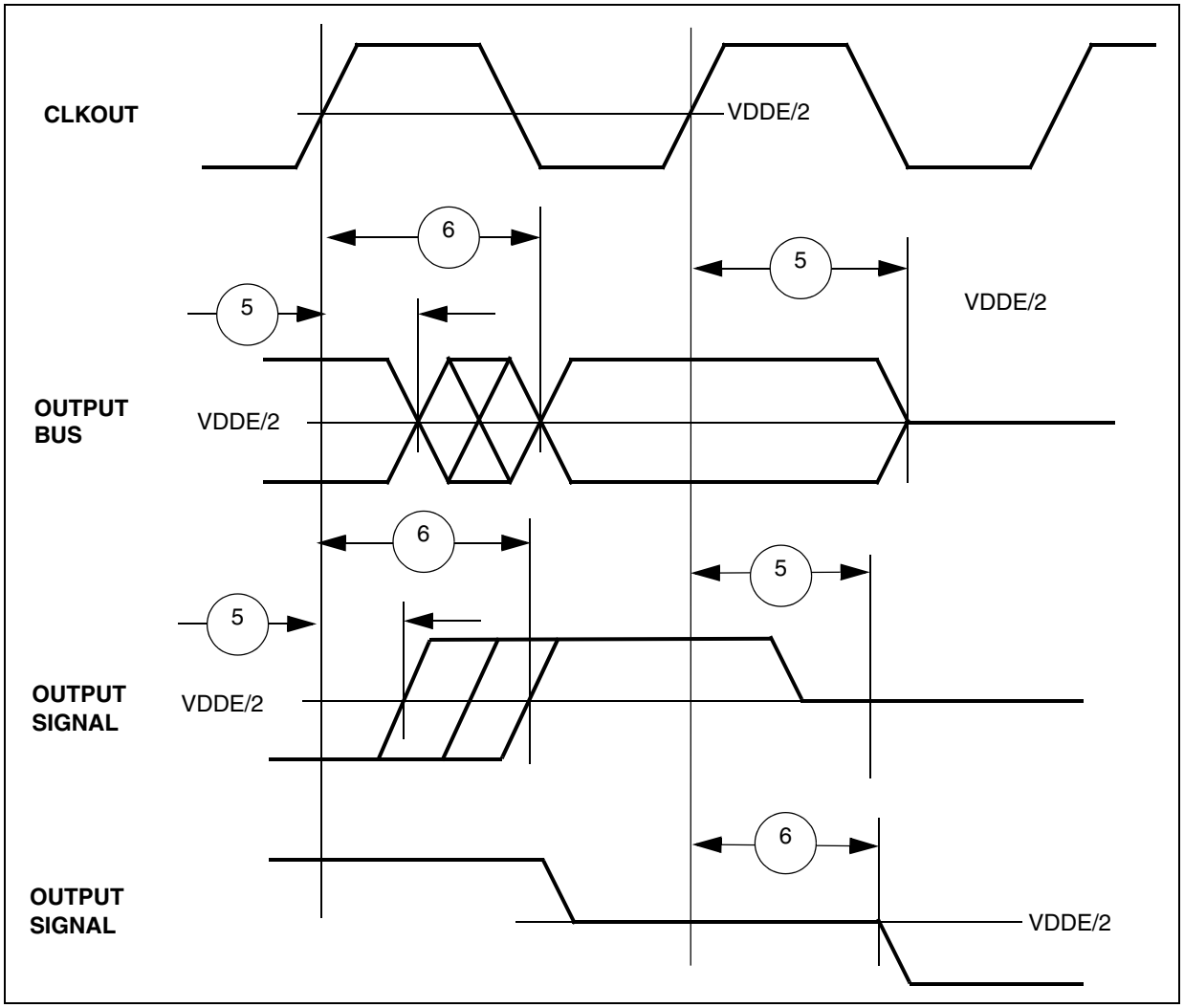


Figure 20. Synchronous output timing

Table 46. DSPI timing[1,2] (continued)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
9	t_{SUI}	CC	Data Setup Time for Inputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	20	—	ns
			D		V_{DDEH}=3–3.6 V	22	—	
			D	Slave		2	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		8	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	20	—	
			D		V_{DDEH}=3–3.6 V	22	—	
10	t_{HI}	CC	Data Hold Time for Inputs					
			D	Master (MTFE = 0)		–4	—	ns
			D	Slave		7	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		21	—	
			D	Master (MTFE = 1, CPHA = 1)		–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	—	5	ns
			D		V_{DDEH}=3–3.6 V	—	6.3	
			D	Slave	V_{DDEH}=4.75–5.25 V	—	25	
			D		V_{DDEH}=3–3.6 V	—	25.7	
			D	Master (MTFE = 1, CPHA = 0)		—	21	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	—	5	
			D		V_{DDEH}=3–3.6 V	—	6.3	
12	t_{HO}	CC	Data Hold Time for Outputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	–5	—	ns
			D		V_{DDEH}=3–3.6 V	–6.3	—	
			D	Slave		5.5	—	
			D	Master (MTFE = 1, CPHA = 0)		3	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	–5	—	
			D		V_{DDEH}=3–3.6 V	–6.3	—	

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type pad_msr. DSPI signals using pad type of pad_ssr have an additional delay based on the slew rate. DSPI timing is specified at V_{DDEH} = 3.0 to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b11.

2 Data is verified at f_{SYS} = 102 MHz and 153 MHz (100 MHz and 150 MHz + 2% frequency modulation).

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5642A devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.

6 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

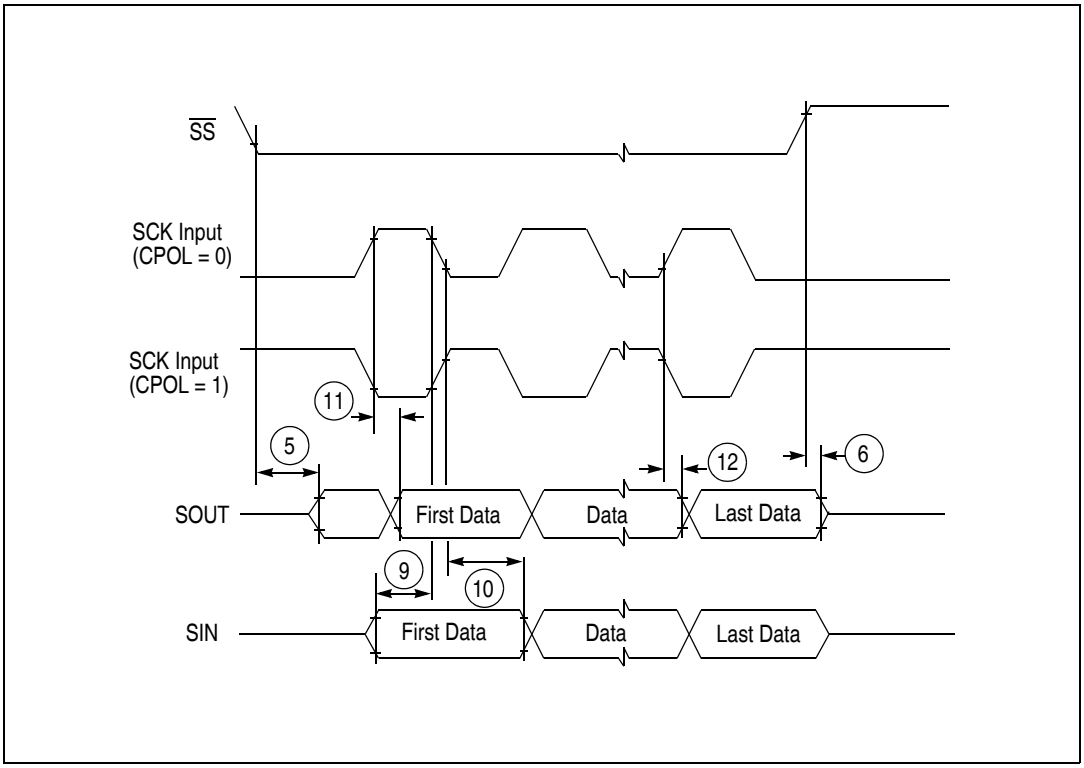


Figure 31. DSPI modified transfer format timing (slave, CPHA = 1)

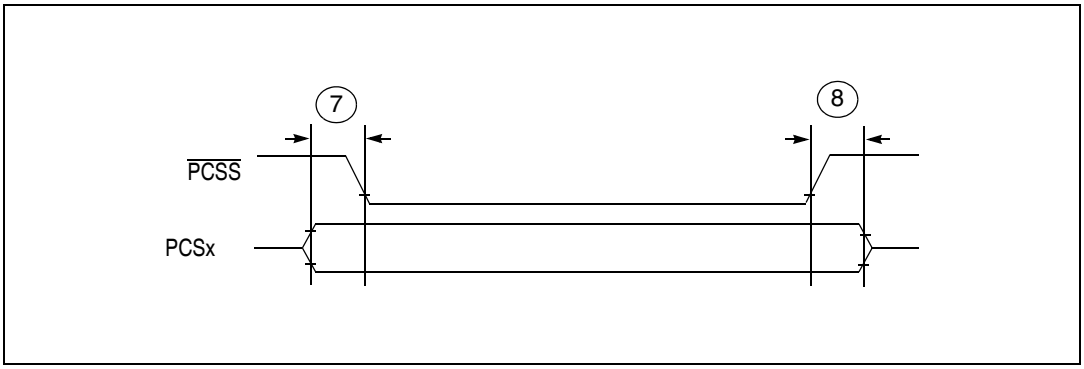


Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4.1.3 324 TEPBGA

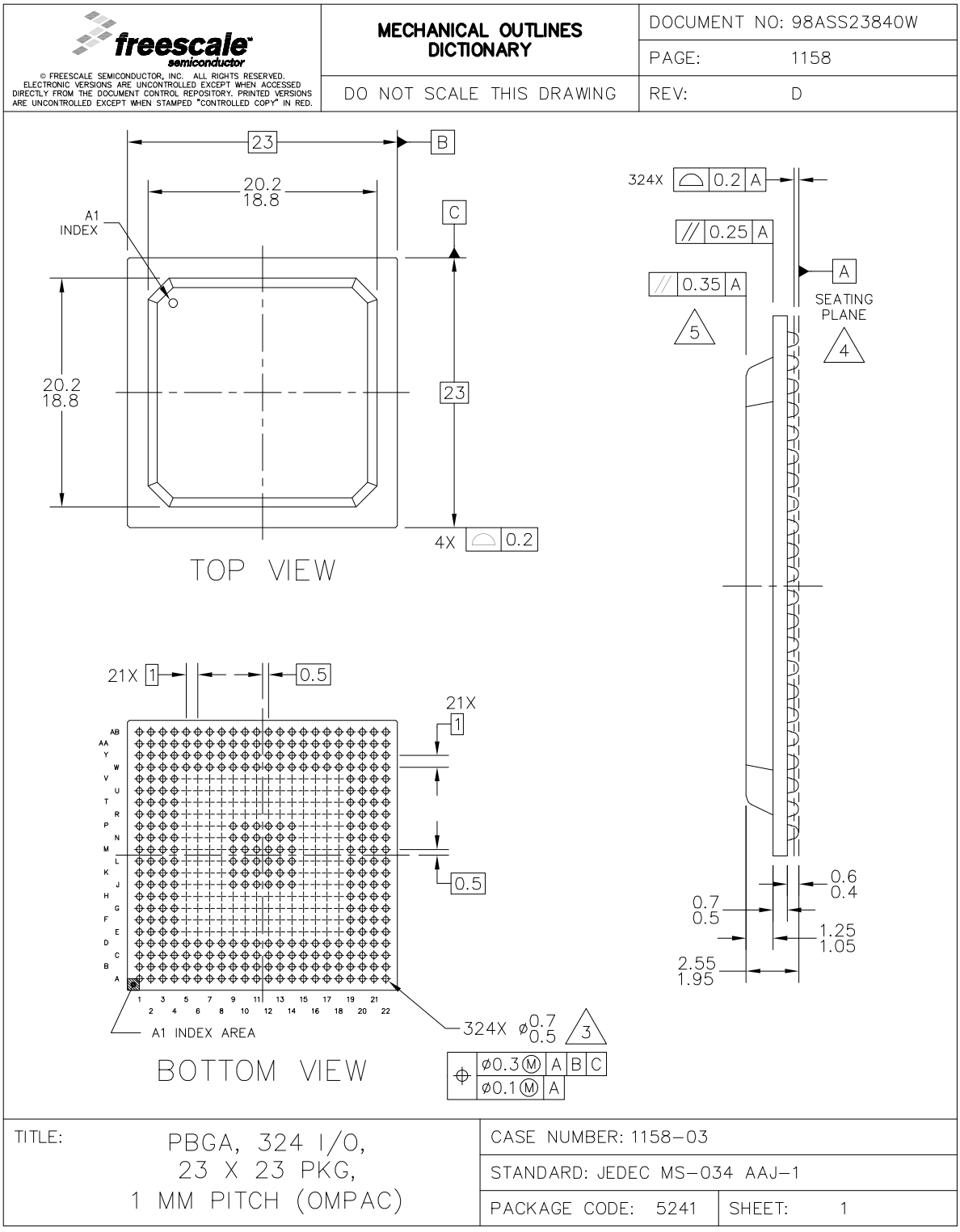


Figure 39. 324 BGA package mechanical drawing (part 1)

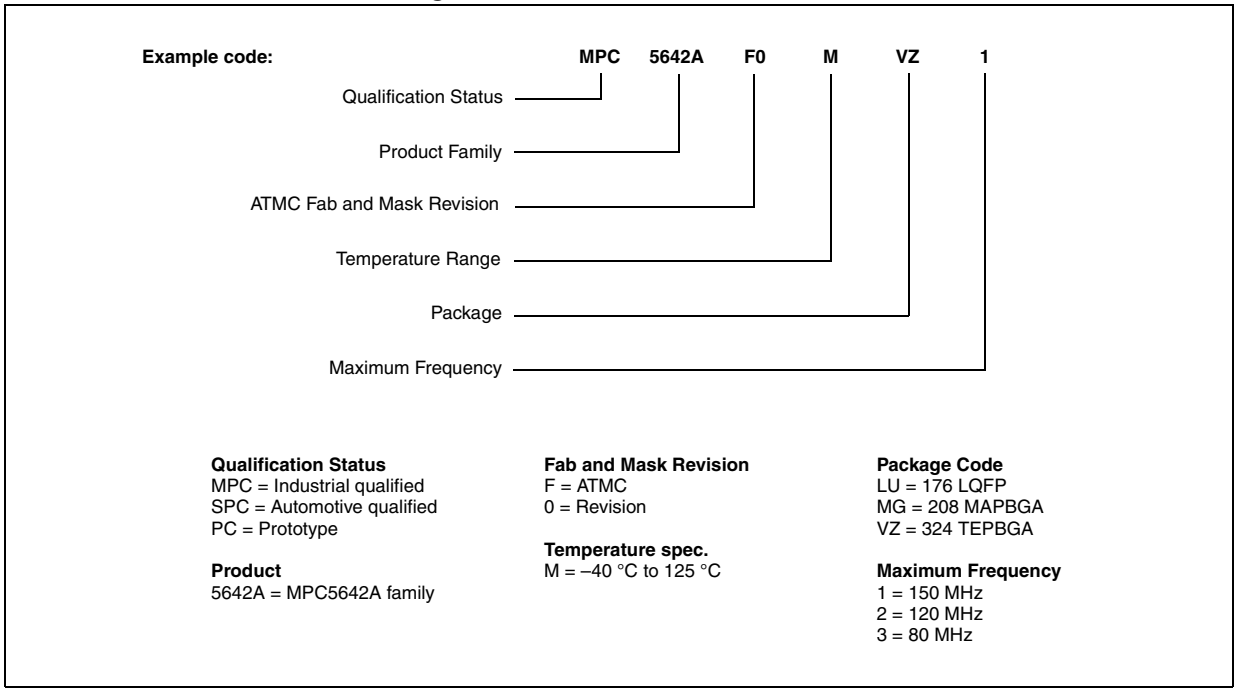
5 Ordering information

Table 50 shows the orderable part numbers for the MPC5642A series.

Table 50. Orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
SPC5642AF2MLU1	2 MB/128 KB	176 LQFP (Pb free)	150
SC667201MMG1	2 MB/128 KB	208 MAPBGA (Pb free)	
SPC5642AF2MVZ1	2 MB/128 KB	324 TEPBGA	
SPC5642AF2MLU2	2 MB/128 KB	176 LQFP (Pb free)	120
SC667201MMG2	2 MB/128 KB	208 MAPBGA (Pb free)	
SPC5642AF2MVZ2	2 MB/128 KB	324 TEPBGA	
SPC5642AF2MLU3	2 MB/128 KB	176 LQFP (Pb free)	80
SC667201MMG3	2 MB/128 KB	208 MAPBGA (Pb free)	
SPC5642AF2MVZ3	2 MB/128 KB	324 TEPBGA	

Figure 41. Product code structure



6 Document revision history

Table 51 summarizes customer facing revisions to this document.

Table 51. Revision history

Date	Revision	Substantive changes
05 Oct 2010	1	Initial release
26 Mar 2012	2	Figure 1 (MPC5642A series block diagram), added ECSM block and its definition in the elegend. Table 2 (MPC5642A series block summary), added the following blocks: REACN, SIU, ECSM, FMPLL, PIT and SWT. Updated Table 8 (Absolute maximum ratings) In 3, Electrical characteristics, deleted the “Recommended operating conditions” subsection. Table 14 (PMC operating conditions and external regulators supply voltage), removed minimum value of V_{DDREG} and its footnote. Updated Table 15 (PMC electrical characteristics) Updated Section 3.6.1, Regulator example Updated Table 20 (DC electrical specifications) Figure 8 (Core voltage regulator controller external components preferred configuration), added “T1” label to indicate the transistor. Table 20 (DC electrical specifications), changed maximum value of V_{IL_LS} to 0.9, was 1.1 Table 21 (I/O pad average I_{DDE} specifications), in the V_{DDE} column changed all 5.5 to 5.25 Table 24 (DSPI LVDS pad specification): Renamed V_{OC}, was V_{OD} Updated minimum and maximum value of V_{OC} deleted all footnote Table 26 (Temperature sensor electrical characteristics), updated minimum and maximum value of accuracy Updated Section 3.12, eQADC electrical characteristics Added Section 3.13, Configuring SRAM wait states Updated Table 31 (APC, RWSC, WWSC settings vs. frequency of operation) Updated Table 32 (Flash program and erase specifications) Table 31 (APC, RWSC, WWSC settings vs. frequency of operation), changed all values in the WWSC column to 0b01. Updated Table 32 (Flash program and erase specifications) Table 33 (Flash EEPROM module life): updated temperature value in the Retention description (was 150 °C, is 85 °C) added values for Retention Table 34 (Pad AC specifications (V_{DDE} = 4.75 V)): changed maximum value of Medium to 12/12 changed maximum value of Slow to 20/20 Updated Table 35 (Pad AC specifications (V_{DDE} = 3.0 V)) Table 37 (JTAG pin AC electrical characteristics): changed all parameter classification to D changed minumum value of t_{TMSS}, t_{TDIS} to 10 Updated Table 38 (Nexus debug port timing) Added Table 39 (Nexus debug port operating frequency) Table 39 (Nexus debug port operating frequency), added a footnote near the value of t_{AAI} Table 44 (eMIOS timing): changed minumum value of t_{MOPW} to 1 removed the footnote of t_{MOPW}