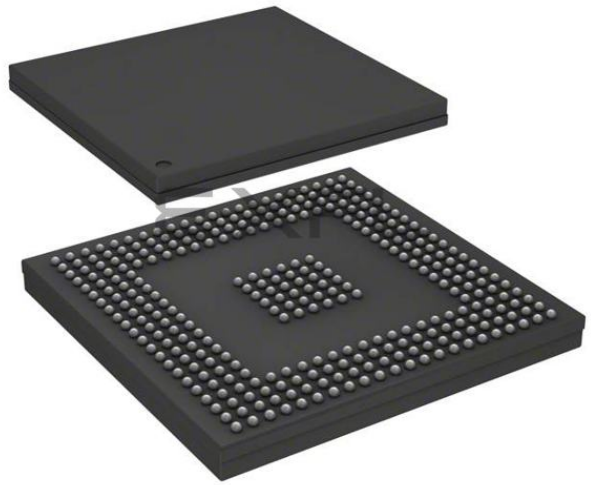

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5642af2mvz2

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5642A series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This microcontroller is a 32-bit system-on-chip (SoC) device intended for use in mid-range engine control and automotive transmission control applications.

It is compatible with devices in Freescale's MPC5600 family and offers performance and capabilities beyond the MPC5632M devices.

The microcontroller's e200z4 host processor core is built on the Power Architecture® technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The device has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by a 128 KB on-chip SRAM and a 2 MB internal flash memory.

For development, the device includes a calibration bus that is accessible only when using the Freescale VertiCal Calibration System.

1.3 Device feature summary

Table 1 summarizes the MPC5642A features and compares them to those of the MPC5644A.

Table 1. MPC5642A device feature summary

Feature		MPC5642A	MPC5644A
Process		90 nm	
Core		e200z4	
	SIMD	Yes	
	VLE	Yes	
	Cache	8 KB instruction	
	Non-Maskable Interrupt (NMI)	NMI and Critical Interrupt	
	MMU	24-entry	
	MPU	16-entry	
	Crossbar switch	4 × 4	5 × 4
	Core performance	0–150 MHz	
Windowing software watchdog		Yes	
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit

Table 2. MPC5642A series block summary (continued)

Block	Function
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer
System watchdog timer (SWT)	Provides protection from runaway code
Temperature sensor	Provides the temperature of the device as an analog value

1.5 Feature details

1.5.1 e200z4 core

MPC5642A devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability
  - Synthesizeable, MuxD scan design
  - ABIST/MBIST for arrays
  - Built-in Parallel Signature Unit

— An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
— 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The MPC5642A SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software

- 3 channels' internal timebases sharable between channels
- 1 timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)
- Each channel (0–23) supports the following functions:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
  - Output Pulse Width Modulation Buffered (OPWMB)
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (DOAC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width & Frequency Modulation Buffered (OPWFMB)
- Each channel has its own pin (not available on all package types)

1.5.12 Second generation enhanced time processing unit (eTPU2)

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

MPC5642A devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler

  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

2.2 208 MAP BGA ballmap

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS[3]	DSPI_B_SIN	DSPI_B_ PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_ PCS[4]	DSPI_B_ PCS[2]	DSPI_B_ PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_ SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ ETPUA29_O	MDO4_ ETPUA2_O	MDO8_ ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P
R	NC	VSS	VDD	GPIO[206]	EMIOS4	EMIOS3	EMIOS9	EMIOS11	EMIOS14	MDO10_ ETPUA27_O	EMIOS23	CAN_A_RX	CAN_B_RX	VDD	VSS	VDDPLL	R
T	VSS	VDD	NC	EMIOS0	EMIOS1	GPIO[219]	MDO9_ ETPUA25_O	EMIOS13	EMIOS15	MDO5_ ETPUA4_O	MDO6_ ETPUA13_O	CAN_B_TX	VDDE12	ENGCLK	VDD	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. 208-pin MAPBGA package ballmap (viewed from above)

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration data bus	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[0]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[1]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A1	01 10	343	O O	VDDE12 / Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[11] / —	—	—	—

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
NEXUS[13]											
$\overline{\text{EVTI}}$	Nexus event in	P	01	231	I	VDDEH7 / MultiV	— / Up	$\overline{\text{EVTI}}$ / Up	116	E15	H20
$\overline{\text{EVTO}}$[14]	Nexus event out	P	01	227	O	VDDEH7 / MultiV	ABR/Up	$\overline{\text{EVTO}}$ / —	120	D15	G20
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 / Fast	—	MCKO / —	14	F15	F1
MDO[0]	Nexus message data out	P	01	220	O	VRC33 / Fast	—	MDO[0] / —	17	A14	F3
MDO[1]	Nexus message data out	P	01	221	O	VRC33 / Fast	—	MDO[1] / —	18	B14	G2
MDO[2]	Nexus message data out	P	01	222	O	VRC33 / Fast	—	MDO[2] / —	19	A13	G3
MDO[3]	Nexus message data out	P	01	223	O	VRC33 / Fast	—	MDO[3] / —	20	B13	G4
MDO[4] ETPUA2_O GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	75	O O I/O	VDDEH7 / MultiV	—	— / —	126	P10	B19
MDO[5] ETPUA4_O GPIO[76]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	76	O O I/O	VDDEH7 / MultiV	—	— / —	129	T10	B20
MDO[6] ETPUA13_O GPIO[77]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	77	O O I/O	VDDEH7 / MultiV	—	— / —	135	T11	C18
MDO[7] ETPUA19_O GPIO[78]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	78	O O I/O	VDDEH7 / MultiV	—	— / —	136	N11	B18
MDO[8] ETPUA21_O GPIO[79]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	79	O O I/O	VDDEH7 / MultiV	—	— / —	137	P11	A18
MDO[9] ETPUA25_O PIO[80]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	80	O O I/O	VDDEH7 / MultiV	—	— / —	139	T7	D18
MDO[10] ETPUA27_O GPIO[81]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	81	O O I/O	VDDEH7 / MultiV	—	— / —	134	R10	A19
MDO[11] ETPUA29_O GPIO[82]	Nexus message data out eTPU A channel (output only) GPIO[82]	P A1 G	01 10 00	82	O O I/O	VDDEH7 / MultiV	—	— / —	124	P9	C19

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
AN18	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[18] / —	1	D5	B4
AN19	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[19] / —	—	—	D6
AN20	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[20] / —	—	—	C5
AN21	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[21] / —	173	B4	B6
AN22	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[22] / —	161	B8	D9
AN23	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[23] / —	160	C9	A8
AN24	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[24] / —	159	D8	B9
AN25	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[25] / —	158	B9	A9
AN26	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[26] / —	—	—	D10
AN27	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[27] / —	157	A10	C10
AN28	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[28] / —	156	B10	D11
AN29	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[29] / —	—	—	C11
AN30	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[30] / —	155	D9	B11
AN31	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[31] / —	154	D10	D12
AN32	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[32] / —	153	C10	C12
AN33	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[33] / —	152	C11	B12
AN34	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[34] / —	151	C5	A12
AN35	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[35] / —	150	D11	D13
AN36	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[36] / —	174	F4	B5

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
ETPUA17 DSPI_D_PCS[2] RCH3_A GPIO[131]	eTPU A channel DSPI D peripheral chip select Reaction channel 3A GPIO	P A1 A2 G	001 010 100 000	131	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	38	H3	Y1
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	37	H4	W3
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	36	J2	W2
ETPUA20 IRQ[8] RCH0_B FR_A_TX GPIO[134]	eTPU A channel External interrupt request Reaction channel 0B FlexRay transmit data channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	134	I/O I O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	35	J1	W1
ETPUA21 IRQ[9] RCH0_C FR_A_RX GPIO[135]	eTPU A channel External interrupt request Reaction channel 0C FlexRay receive channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	135	I/O I O I I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	34	G4	N4
ETPUA22 IRQ[10] ETPUA17_O GPIO[136]	eTPU A channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	136	I/O I O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	32	H2	N3
ETPUA23 IRQ[11] ETPUA21_O FR_A_TX_EN GPIO[137]	eTPU A channel External interrupt request eTPU A channel (output only) FlexRay ch. A transmit enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	137	I/O I O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	30	H1	M1
ETPUA24 IRQ[12] DSPI_C_SCK_LVDS– GPIO[138]	eTPU A channel External interrupt request LVDS negative DSPI clock GPIO	P A1 A2 G	001 010 100 000	138	I/O I O I/O	VDDEH1 / Slow + LVDS	— / WKPCFG	— / WKPCFG	28	G1	M2
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 / Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	M3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS– GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 / Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	L2

3.3 Thermal characteristics

Table 9. Thermal characteristics for 176-pin LQFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Single-layer board – 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Four-layer board – 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient[2]	at 200 ft./min., single-layer board – 1s	30	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top, natural convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 10. Thermal characteristics for 208-pin MAPBGA[1],

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Single layer board – 1s[3]	39	°C/W
	CC	D		Four layer board – 2s2p[4]	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient[2]	at 200 ft./min., single-layer board – 1s[4]	31	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four-layer board – 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal

4 Per JEDEC JESD51-6 with the board horizontal

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

Table 20. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IL_LS}	SR	P	Multi-voltage I/O pad input low voltage in Low-swing-mode[7,8,9,10]	Hysteresis enabled	V_{SS} – 0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.9	
V_{IL_HS}	SR	P	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS} – 0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.4 V_{DDEH}	
V_{IH_S}	SR	P	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{IH_F}	SR	P	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE} + 0.3	
V_{IH_LS}	SR	P	Multi-voltage pad I/O input high voltage in low-swing-mode[7,8,9,10]	Hysteresis enabled	2.5	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDE} + 0.3	
V_{IH_HS}	SR	P	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage[11]	—	—	—	0.2 * V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage[11]	—	—	—	0.2 * V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[7,8,9,10,11]	—	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode[11]	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium I/O output high voltage[11]	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage[11]	—	0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[7,8,9,10,11]	—	2.3	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[11]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	P	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	P	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-swing-mode multi-voltage I/O input hysteresis	Hysteresis enabled	0.25	—	—	v

[18] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.

[19] Applies to CLKOUT, external bus pins, and Nexus pins

[20] Applies to the FCK, SDI, SDO, and SDS pins

[21] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 21 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 21.

Table 21. I/O pad average I_{DDE} specifications[1]

Pad type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.25	11	9	—
		CC	D	30	50	5.25	01	6.1	—
		CC	D	117	50	5.25	00	2.3	—
		CC	D	212	200	5.25	00	5.8	—
MultiV (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.25	11	3.4	—

[1] Numbers from simulations at best case process, 150 °C

[2] All loads are lumped.

[3] Average current is for pad configured as output only

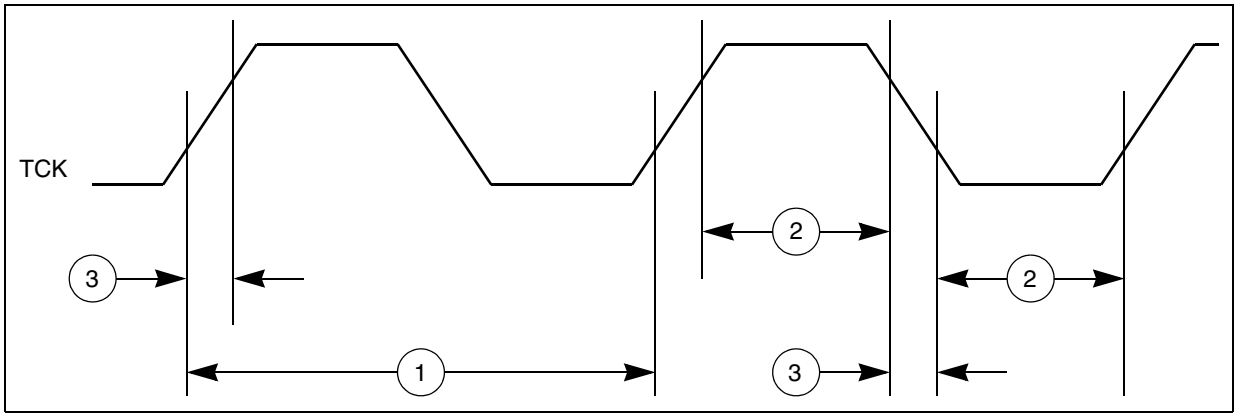

Figure 12. JTAG test clock input timing

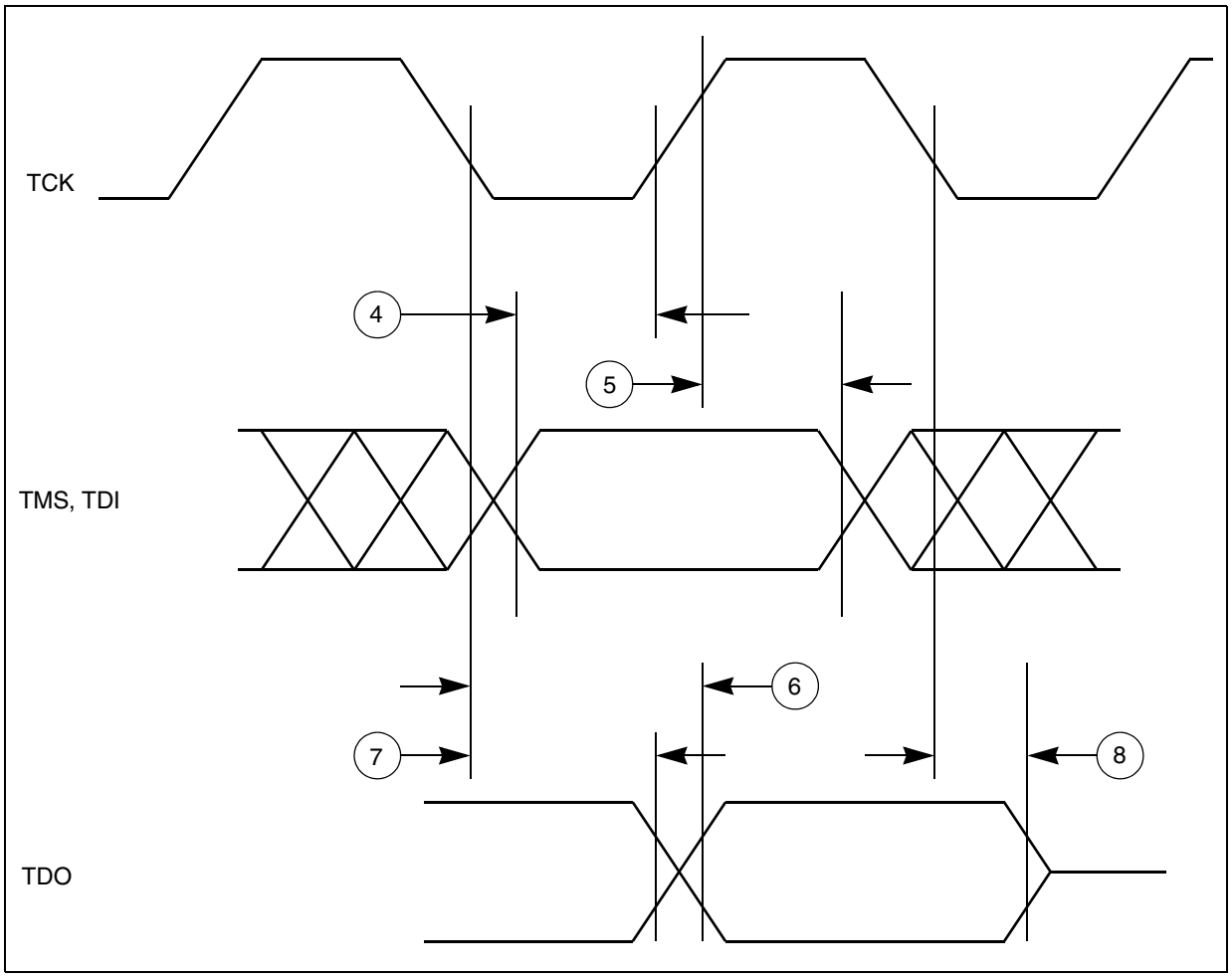

Figure 13. JTAG test access port timing

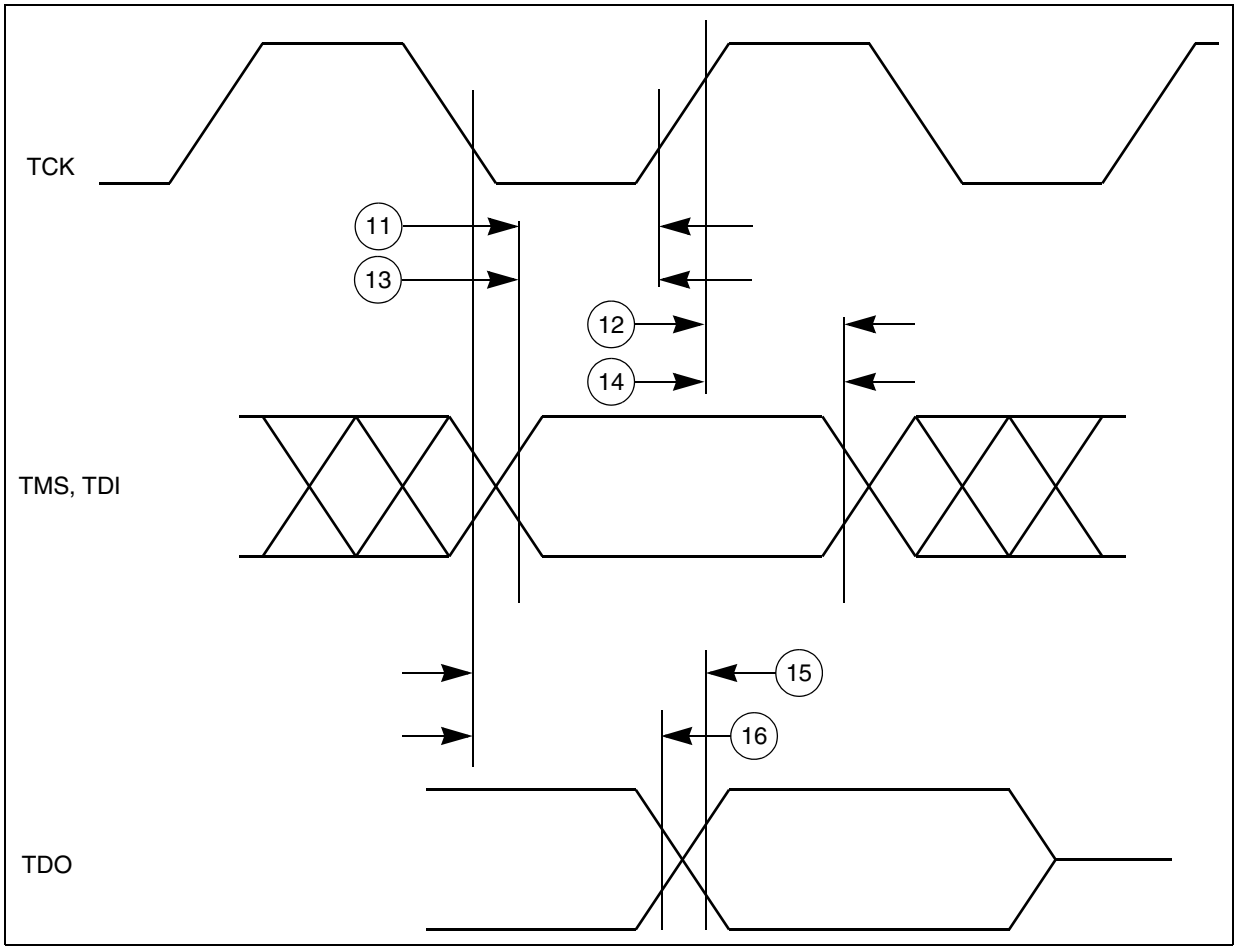

Figure 18. Nexus TDI, TMS, TDO timing

Table 39. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
176 LQFP 208 BGA 324 BGA	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
496 CSP	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
		Route to CAL_MDO[7]	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz[3]

1 NPC_PCR[FPM] = 0

2 NPC_PCR[NEXCFG] = 0

3 The Nexus AUX port runs up to 40 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 40 MHz.

4 NPC_PCR[FPM] = 1

5 Set the NPC_PCR[MCKO_DIV] to divide by two if the system frequency is between 40 MHz and 80 MHz inclusive. Set the NPC_PCR[MCKO_DIV] to divide by four if the system frequency is greater than 80 MHz.

6 Pad restrictions limit the Maximum Operation Frequency in these configurations

7 NPC_PCR[NEXCFG] = 1

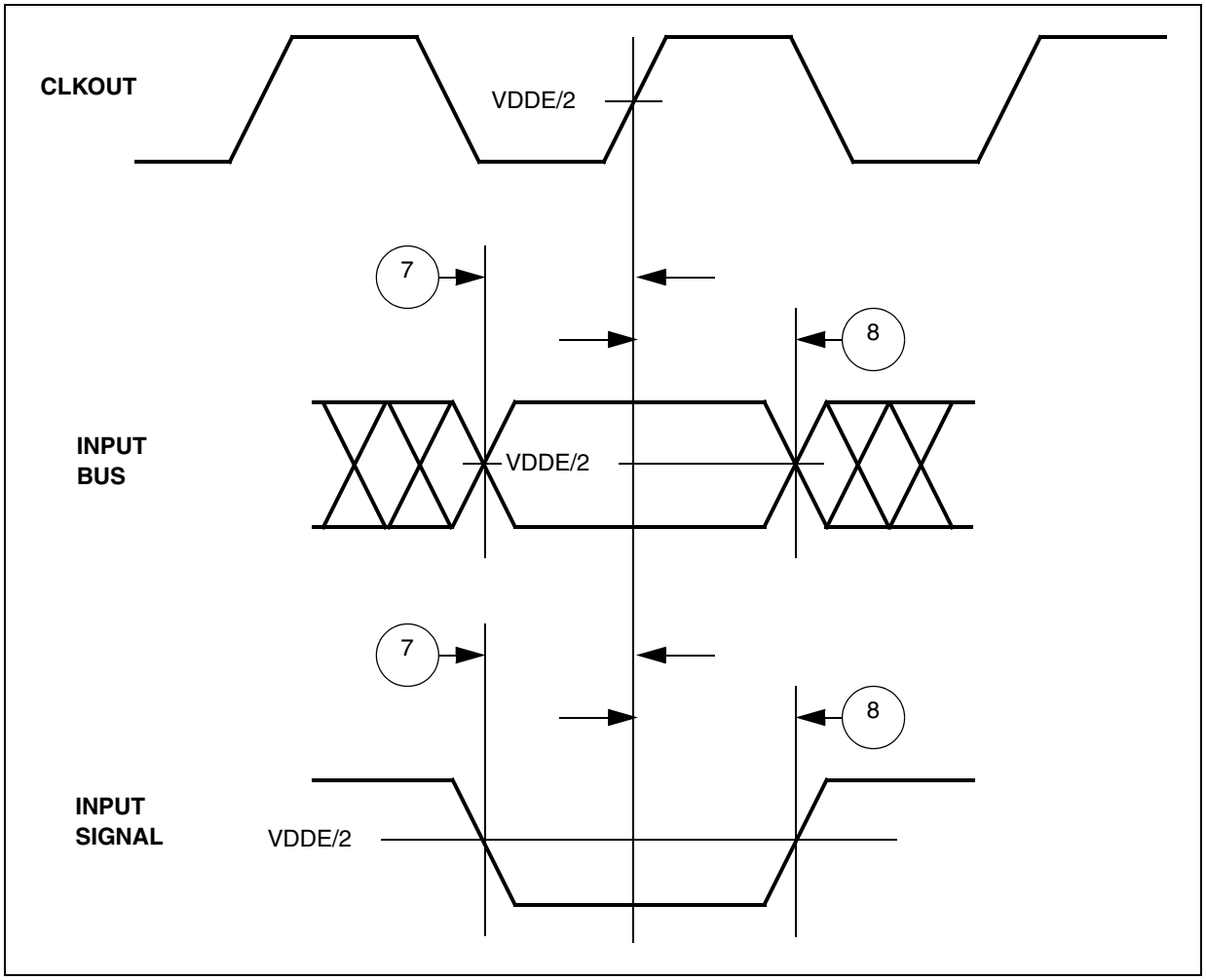

Figure 21. Synchronous input timing

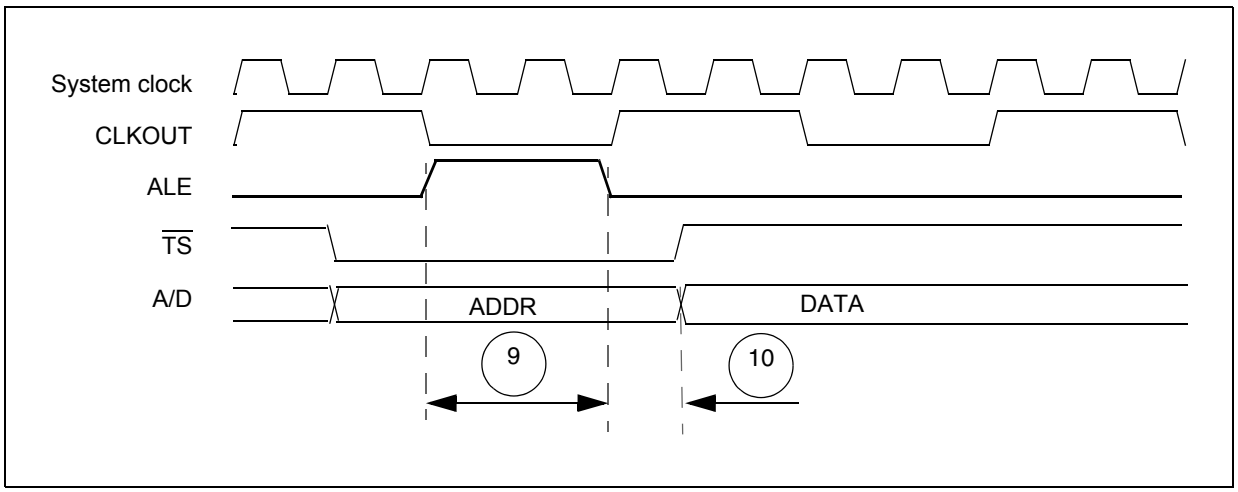

Figure 22. ALE signal timing

Figure 34. 176 LQFP package mechanical drawing (part 1)

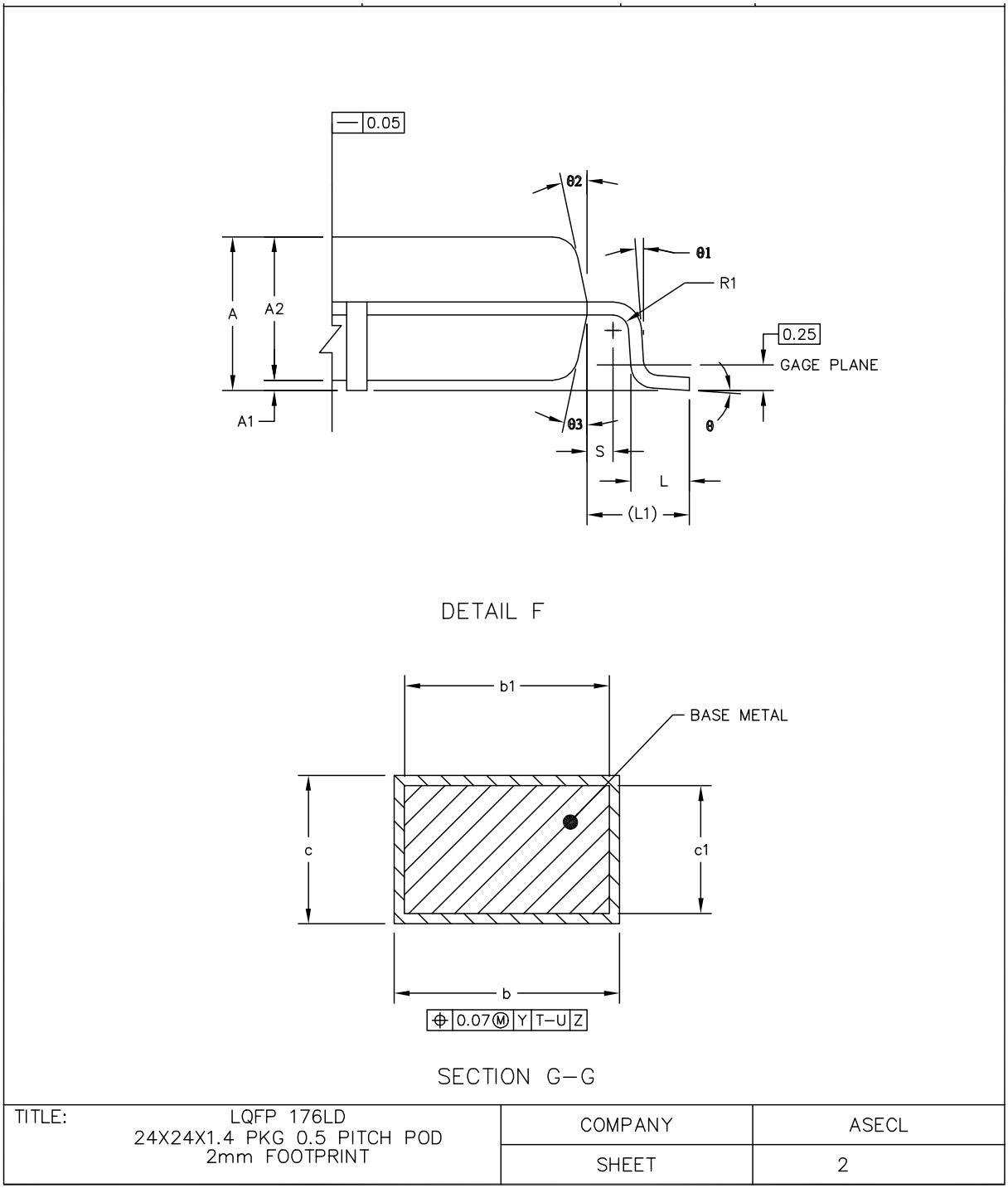

Figure 35. 176 LQFP package mechanical drawing (part 2)

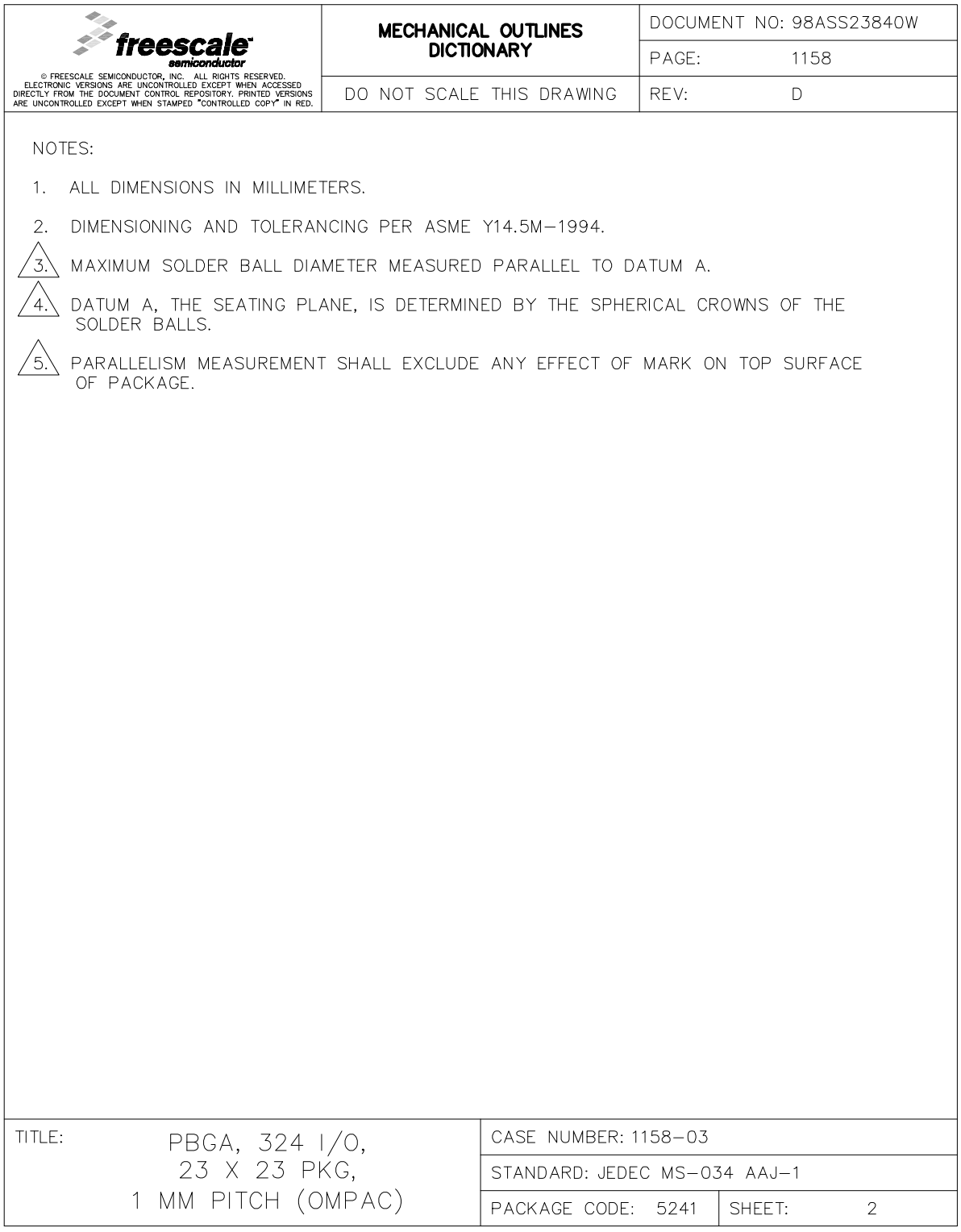

Figure 40. 324 BGA package mechanical drawing (part 2)