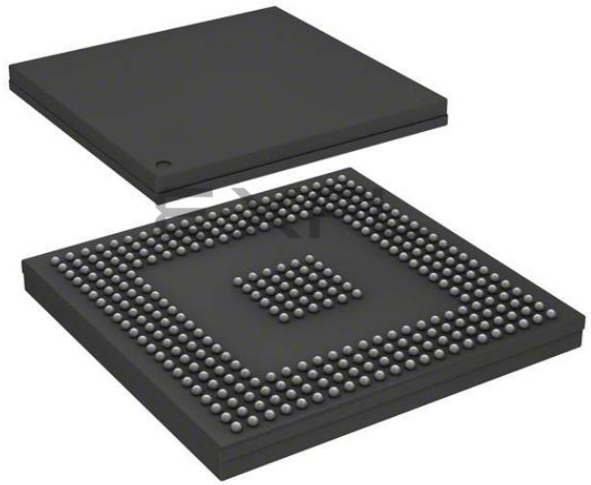


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5642af2mvz2r

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: MPC5642A_AD
Rev. 1
12/2014

Table 2. MPC5642A series block summary (continued)

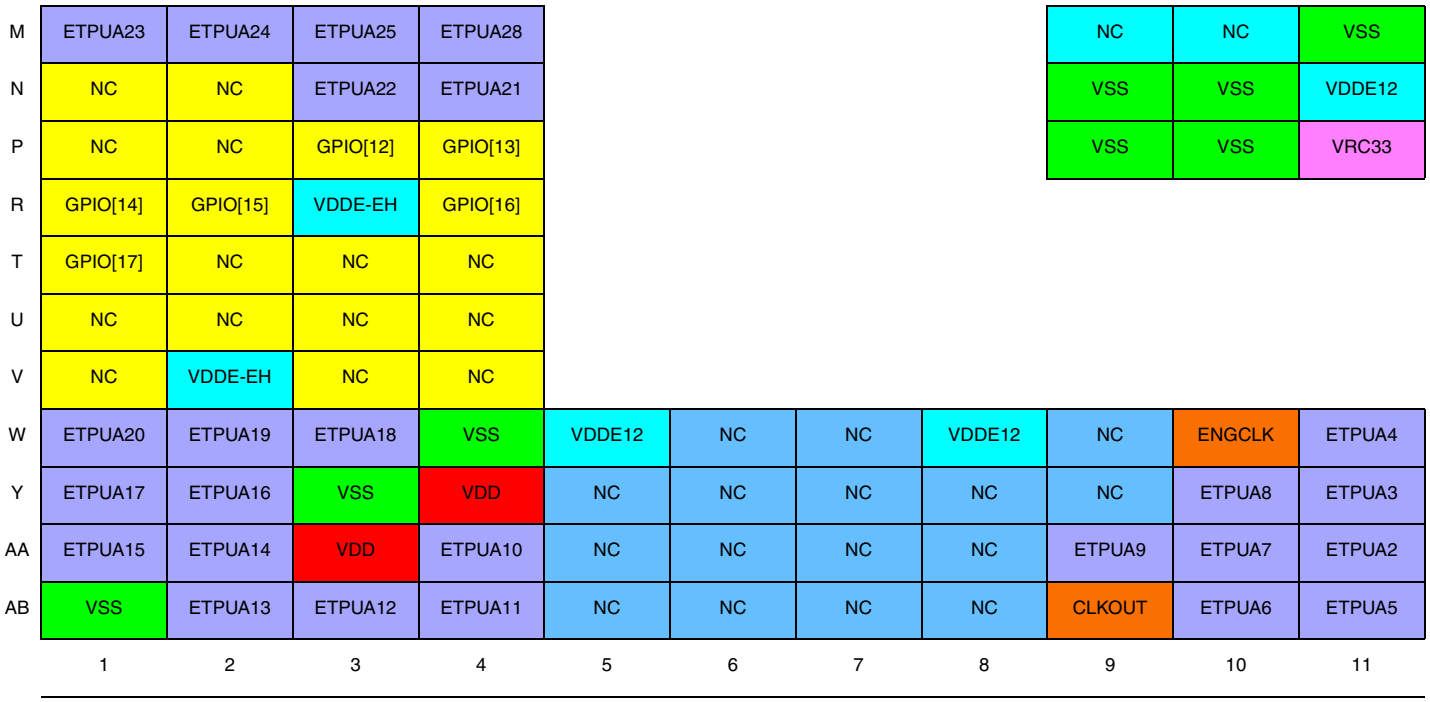
Block	Function
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer
System watchdog timer (SWT)	Provides protection from runaway code
Temperature sensor	Provides the temperature of the device as an analog value

1.5 Feature details

1.5.1 e200z4 core

MPC5642A devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability
  - Synthesizeable, MuxD scan design
  - ABIST/MBIST for arrays
  - Built-in Parallel Signature Unit



	1	2	3	4	5	6	7	8	9	10	11
M	ETPUA23	ETPUA24	ETPUA25	ETPUA28					NC	NC	VSS
N	NC	NC	ETPUA22	ETPUA21					VSS	VSS	VDDE12
P	NC	NC	GPIO[12]	GPIO[13]					VSS	VSS	VRC33
R	GPIO[14]	GPIO[15]	VDDE-EH	GPIO[16]							
T	GPIO[17]	NC	NC	NC							
U	NC	NC	NC	NC							
V	NC	VDDE-EH	NC	NC							
W	ETPUA20	ETPUA19	ETPUA18	VSS	VDDE12	NC	NC	VDDE12	NC	ENGCLK	ETPUA4
Y	ETPUA17	ETPUA16	VSS	VDD	NC	NC	NC	NC	NC	ETPUA8	ETPUA3
AA	ETPUA15	ETPUA14	VDD	ETPUA10	NC	NC	NC	NC	ETPUA9	ETPUA7	ETPUA2
AB	VSS	ETPUA13	ETPUA12	ETPUA11	NC	NC	NC	NC	CLKOUT	ETPUA6	ETPUA5

Figure 5. 324-pin TEPBGA package ballmap (southwest, viewed from above)

VSS	VSS	VSS					VRC33	NC	NC	VDDEH6AB	M
VSS	VSS	VSS					NC	SCI_A_TX	VSS	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							NC	NC	NC	RESET	R
							VSS	BOOTCFG0	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG1	EXTAL	U
							SCI_C_RX	CAN_C_RX	PLLREF	XTAL	V
ETPUA1	EMIOS1	VDDEH4AB	EMIOS8	EMIOS15	EMIOS16	EMIOS23	SCI_C_TX	VDD	CAN_B_RX	VDDPLL	W
ETPUA0	EMIOS2	EMIOS5	EMIOS9	EMIOS14	EMIOS17	EMIOS22	CAN_A_RX	VSS	VDD	CAN_B_TX	Y
EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS18	EMIOS21	VDDEH4AB	WKPCFG	VSS	VDD	AA
TCRCLKA	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS19	EMIOS20	CAN_A_TX	SCI_B_RX	SCI_B_TX	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin TEPBGA package ballmap (southeast, viewed from above)

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
BOOTCFG[0] IRQ[2] GPIO[211]	Boot Config. Input External Interrupt Request GPIO	P A1 G	01 10 00	211	I I I/O	VDDEH6 / Slow	— / Down	BOOTCFG[0] / Down	—	—	T20
BOOTCFG[1] IRQ[3] ETRIG3 GPIO[212]	Boot Config. Input External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	212	I I I I/O	VDDEH6 / Slow	— / Down	BOOTCFG[1] / Down	85	M15	U21
WKPCFG $\overline{\text{NMI}}$ DSPI_B_SOUT GPIO[213]	Weak Pull Config. Input Non-Maskable Interrupt DSPI B data output GPIO	P A1 A2 G	001 010 100 000	213	I I O I/O	VDDEH6 / Medium	— / Up	WKPCFG / Up	86	L15	AA20
Calibration Bus											
CAL_CS0	Calibration chip select	P	01	336	O	VDDE12 / Fast		— / —	—	—	—
CAL_CS2 CAL_ADDR[10] CAL_WE[2]/BE[2]	Calibration chip select Calibration address bus Calibration write/byte enable	P A1 A2	001 010 100	338	O I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_CS3 CAL_ADDR[11] CAL_$\overline{\text{WE}}$[3]/$\overline{\text{BE}}$[3]	Calibration chip select Calibration address bus Calibration write/byte enable	P A1 A2	001 010 100	339	O I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[12] CAL_$\overline{\text{WE}}$[2]/$\overline{\text{BE}}$[2]	Calibration address bus Calibration write/byte enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[13] CAL_$\overline{\text{WE}}$[3]/$\overline{\text{BE}}$[3]	Calibration address bus Calibration write/byte enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[14] CAL_DATA[31]	Calibration address bus Calibration data bus	P A1	01 10	340	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[15] CAL_ALE	Calibration address bus Calibration address latch enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[16] CAL_DATA[16]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[17] CAL_DATA[17]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[18] CAL_DATA[18]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[19] CAL_DATA[19]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[20] CAL_DATA[20]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[21] CAL_DATA[21]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration data bus	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[0]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[1]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A1	01 10	343	O O	VDDE12 / Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[11] / —	—	—	—

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
SCI_A_TX EMIOS13[15] GPIO[89]	eSCI A transmit eMIOS channel GPIO	P A1 G	01 10 00	89	O O I/O	VDDEH6 / Medium	— / Up	— / Up	100	J14	N20
SCI_A_RX EMIOS15[15] GPIO[90]	eSCI A receive eMIOS channel GPIO	P A1 G	01 10 00	90	I O I/O	VDDEH6 / Medium	— / Up	— / Up	99	K14	P20
SCI_B_TX DSPI_D_PCS[1] GPIO[91]	eSCI B transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	91	O O I/O	VDDEH6 / Medium	— / Up	— / Up	87	L13	AB21
SCI_B_RX DSPI_D_PCS[5] GPIO[92]	eSCI B receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	92	I O I/O	VDDEH6 / Medium	— / Up	— / Up	84	M13	AB20
SCI_C_TX GPIO[244]	eSCI C transmit GPIO	P G	01 00	244	O I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	W19
SCI_C_RX GPIO[245]	eSCI C receive GPIO	P G	01 00	245	I I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	V19
DSPI											
DSPI_A_SCK[16] DSPI_C_PCS[1] GPIO[93]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	93	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	C17
DSPI_A_SIN[16] DSPI_C_PCS[2] GPIO[94]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	94	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	B17
DSPI_A_SOUT[16] DSPI_C_PCS[5] GPIO[95]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	95	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	A17
DSPI_A_PCS[0][16] DSPI_D_PCS[2] GPIO[96]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	96	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	D16
DSPI_A_PCS[1][16] DSPI_B_PCS[2] GPIO[97]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	97	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	C16
DSPI_A_PCS[2][16] DSPI_D_SCK GPIO[98]	— SPI clock pin for DSPI module GPIO	— A1 G	— 10 00	98	— I/O I/O	VDDEH7 / Medium	— / Up	— / Up	141	J15	C15
DSPI_A_PCS[3][16] DSPI_D_SIN GPIO[99]	— DSPI D data input GPIO	— A1 G	— 10 00	99	— I I/O	VDDEH7 / Medium	— / Up	— / Up	142	H13	B15
DSPI_A_PCS[4][16] DSPI_D_SOUT GPIO[100]	— DSPI D data output GPIO	— A1 G	— 10 00	100	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	B16

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
AN18	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[18] / —	1	D5	B4
AN19	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[19] / —	—	—	D6
AN20	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[20] / —	—	—	C5
AN21	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[21] / —	173	B4	B6
AN22	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[22] / —	161	B8	D9
AN23	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[23] / —	160	C9	A8
AN24	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[24] / —	159	D8	B9
AN25	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[25] / —	158	B9	A9
AN26	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[26] / —	—	—	D10
AN27	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[27] / —	157	A10	C10
AN28	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[28] / —	156	B10	D11
AN29	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[29] / —	—	—	C11
AN30	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[30] / —	155	D9	B11
AN31	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[31] / —	154	D10	D12
AN32	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[32] / —	153	C10	C12
AN33	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[33] / —	152	C11	B12
AN34	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[34] / —	151	C5	A12
AN35	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[35] / —	150	D11	D13
AN36	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[36] / —	174	F4	B5

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AB18
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AA18
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	—	—	Y18
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	80	R11	W18
EMIOS14[15] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	A15
EMIOS15[15] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	D14
Clock Synthesizer											
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 / Analog	—	—	93	P16	V22
EXTAL	Crystal oscillator input	P	01	—	I	VDDEH6 / Analog	—	—	92	N16	U22
CLKOUT	System clock output	P	01	229	O	VDDE12 / Fast	—	CLKOUT	—	—	AB9
ENGCLK	Engineering clock output	P	01	214	O	VDDE12 / Fast	—	ENGCLK	—	T14	W10
Power / Ground											
VDDREG	Voltage regulator supply	—		—	I	5 V	I / —	VDDREG	10	K16	F4
VRCCTL	Voltage regulator control output	—		—	O	—	O / —	VRCCTL	11	N14	F2
VRC33[17]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	B1, M19, P11
	Input for external 3.3 V supply	—		—	I	3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	A4, B11	E3, A6
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	A5, A11	A7, E2
VDDPLL	FMPLL supply voltage	—		—	I	1.2 V	I / —	VDDPLL	91	R16	W22
VSTBY	Power supply for standby RAM	—		—	I	0.9 V – 6 V	I / —	VSTBY	12	C1	E4

Table 6. Power/ground segmentation

Power segment	Voltage	I/O pins powered by segment
VDDE5	3.0 V – 3.6 V	DATA[0:15], CLKOUT, ENGCLK
VDDE12	3.0 V – 3.6 V	CAL_CS0, CAL_CS2, CAL_CS3, CAL_ADDR[12:30], CAL_DATA[0:15], CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V – 5.5 V	FR_A_TX, FR_A_TX_EN, FR_A_RX, FR_B_TX, FR_B_TX_EN, FR_B_RX
VDDEH1	3.3 V – 5.5 V	ETPUA[10:31]
VDDEH4	3.3 V – 5.5 V	EMIOS[0:23], TCRCLKA, ETPUA[0:9]
VDDEH6	3.3 V – 5.5 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_B_RX, SCI_C_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0:5], EXTAL, XTAL
VDDEH7	3.3 V – 5.5 V	EMIOS14, EMIOS15, GPIO[98:99], GPIO[203:204], GPIO[206], GPIO[207], GPIO[219], EVTI, EVTO, MDO[4:11], MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0:1], DSPI_A_PCS[4:5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK
VDDA	5.0 V	AN[0:11], AN[16:39], VRH, VRL, REFBYBC
VRC33	3.3 V	MCKO, MDO[0:3]
Other power segments		
VDDREG	5.0 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.9 V – 6.0 V	—
VSS	—	—

[18] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.

[19] Applies to CLKOUT, external bus pins, and Nexus pins

[20] Applies to the FCK, SDI, SDO, and SDS pins

[21] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 21 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 21.

Table 21. I/O pad average I_{DDE} specifications[1]

Pad type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.25	11	9	—
		CC	D	30	50	5.25	01	6.1	—
		CC	D	117	50	5.25	00	2.3	—
		CC	D	212	200	5.25	00	5.8	—
MultiV (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.25	11	3.4	—

[1] Numbers from simulations at best case process, 150 °C

[2] All loads are lumped.

[3] Average current is for pad configured as output only

1 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.

2 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.

4 Condition applies to two adjacent pins at injection limits.

5 Performance expected with production silicon.

6 All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; $I_{INJ}=I_{INJMAX}, I_{INJMIN}$

Table 29. eQADC differential ended conversion specifications (operating)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA1[1]	CC	–	Variable gain amplifier accuracy (gain=1)[2]				
	CC	C	INL	8 MHz ADC	–4	4	Counts[3]
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3[4]	3[4]	Counts
	CC	C		16 MHz ADC	–3[4]	3[4]	Counts
GAINVGA2[1]	CC	–	Variable gain amplifier accuracy (gain=2)[2]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4[1]	CC	–	Variable gain amplifier accuracy (gain=4)[2]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts

3.14 Platform flash controller electrical characteristics

Table 31. APC, RWSC, WWSC settings vs. frequency of operation[1]

Max. Flash Operating Frequency (MHz)[2]	APC[3]	RWSC[3]	WWSC
20 MHz	0b000	0b000	0b01
61 MHz	0b001	0b001	0b01
90 MHz	0b010	0b010	0b01
123 MHz	0b011	0b011	0b01
153 MHz	0b100	0b100	0b01

1 APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.

2 Max frequencies including 2% PLL FM.

3 APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 32. Flash program and erase specifications[1]

#	Symbol		C	Parameter	Value				Unit
					Min	Typ	Initial max[2]	Max[3]	
1	$T_{dwprogram}$	CC	C	Double Word (64 bits) Program Time	—	30	—	500	µs
2	$T_{pprogram}$	CC	C	Page Program Time[4]	—	40	160	500	µs
3	$T_{16kpperase}$	CC	C	16 KB Block Pre-program and Erase Time	—	250	1,000	5,000	ms
5	$T_{64kpperase}$	CC	C	64 KB Block Pre-program and Erase Time	—	450	1,800	5,000	ms
6	$T_{128kpperase}$	CC	C	128 KB Block Pre-program and Erase Time	—	800	2,600	7,500	ms
7	$T_{256kpperase}$	CC	C	256 KB Block Pre-program and Erase Time	—	1,400	5,200	15,000	ms
8	T_{psrt}	SR	—	Program suspend request rate[5]	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate [6]	10				ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Page size is 128 bits (4 words)

5 Time between program suspend resume and the next program suspend request.

6 Time between erase suspend resume and the next erase suspend request.

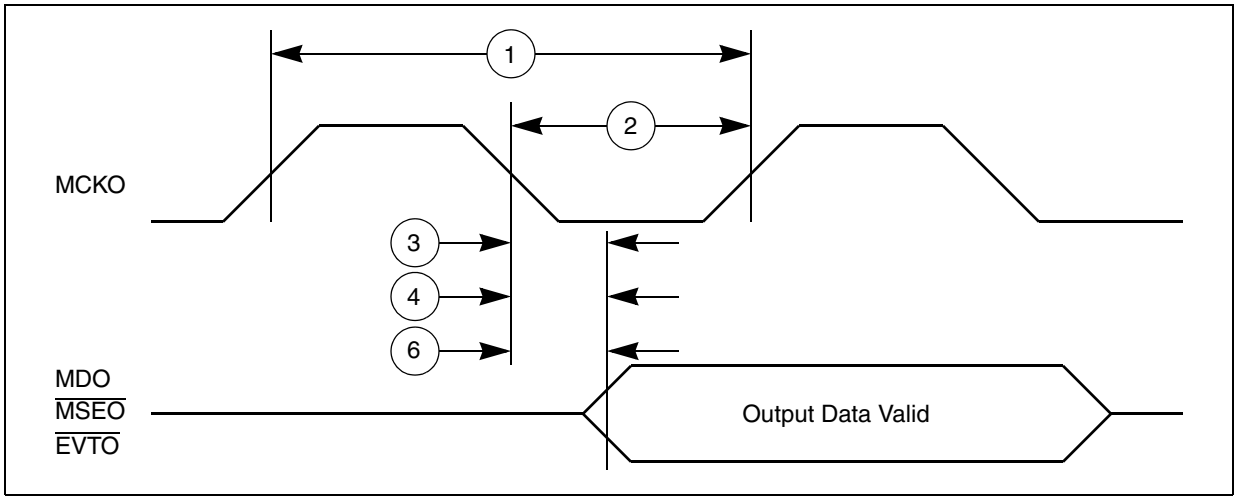


Figure 16. Nexus output timing

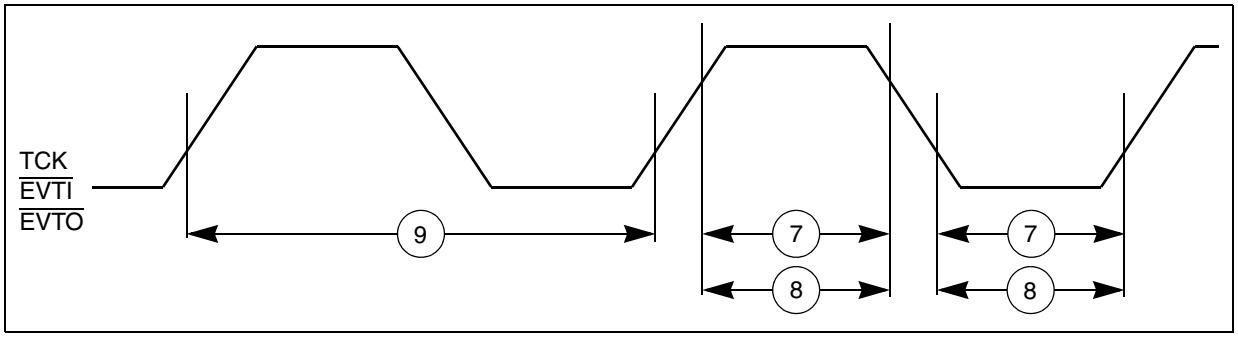


Figure 17. Nexus event trigger and test clock timings

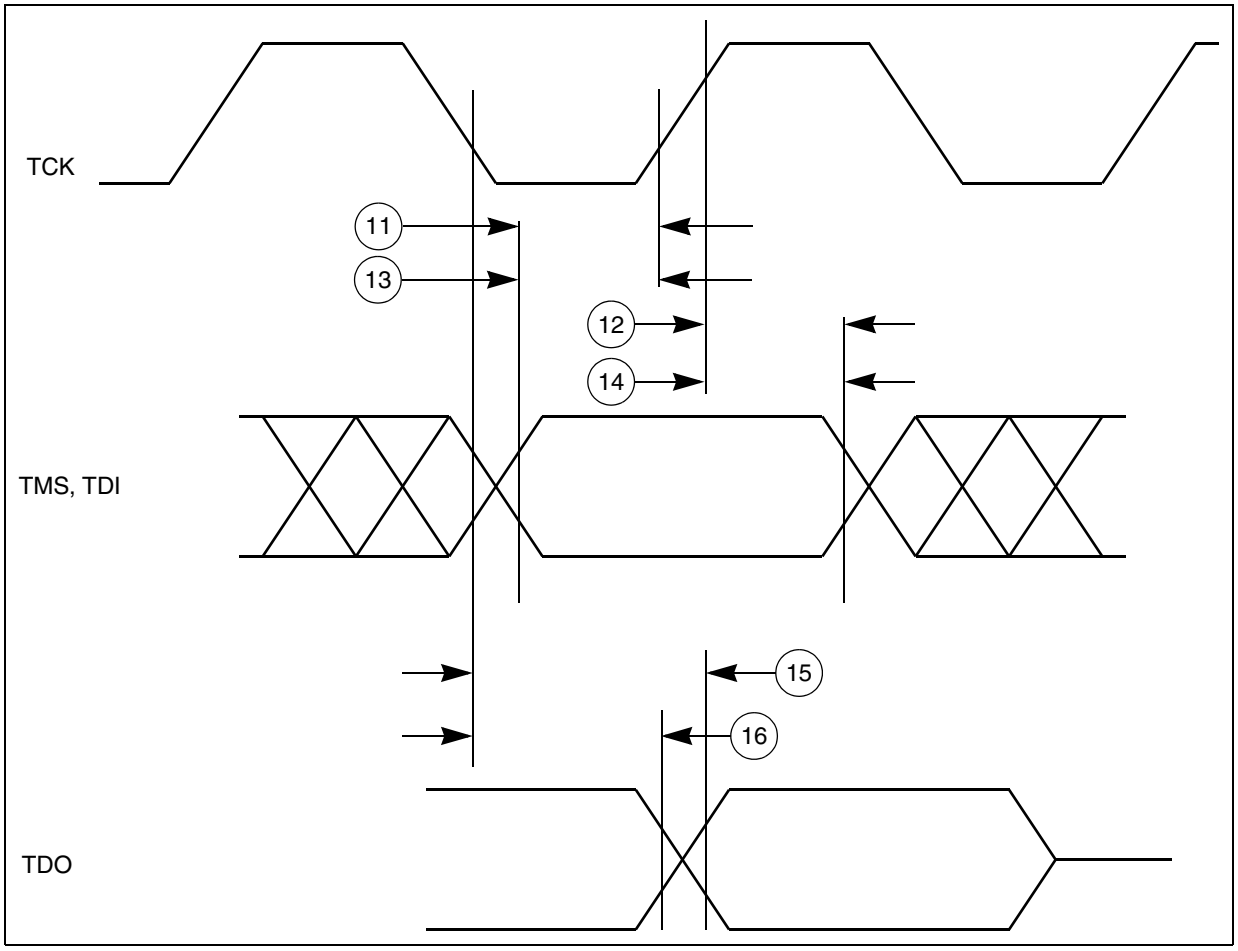


Figure 18. Nexus TDI, TMS, TDO timing

Table 39. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
176 LQFP 208 BGA 324 BGA	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
496 CSP	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
		Route to CAL_MDO[7]	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz[3]

1 NPC_PCR[FPM] = 0

2 NPC_PCR[NEXCFG] = 0

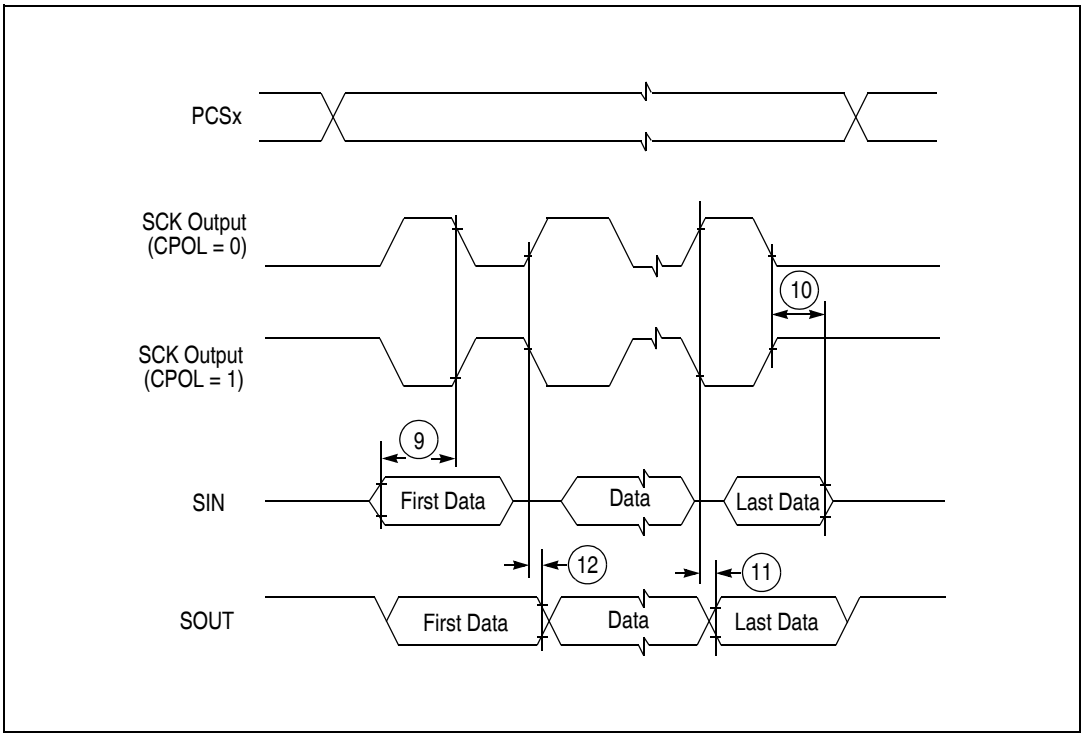


Figure 25. DSPI classic SPI timing (master, CPHA = 1)

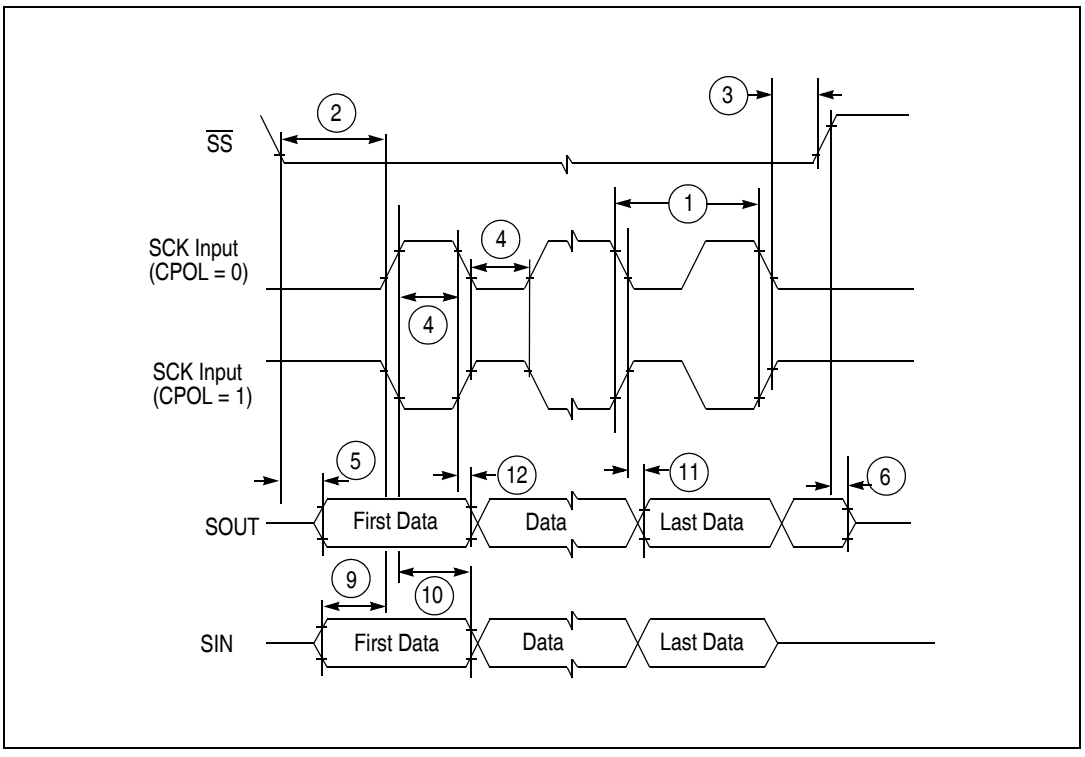


Figure 26. DSPI classic SPI timing (slave, CPHA = 0)

3.17.10 FlexCAN system clock source

Table 48. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	f_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 49. FlexCAN engine system clock divider

System frequency	Required SIU_SYSDIV[CAN_SRC] value
$\leq f_{CAN\_TH}$	0[1,2]
$> f_{CAN\_TH}$	1[2,3]

1 Divides system clock source for FlexCAN engine by 1

2 System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1

3 Divides system clock source for FlexCAN engine by 2

4.1.3 324 TEPBGA

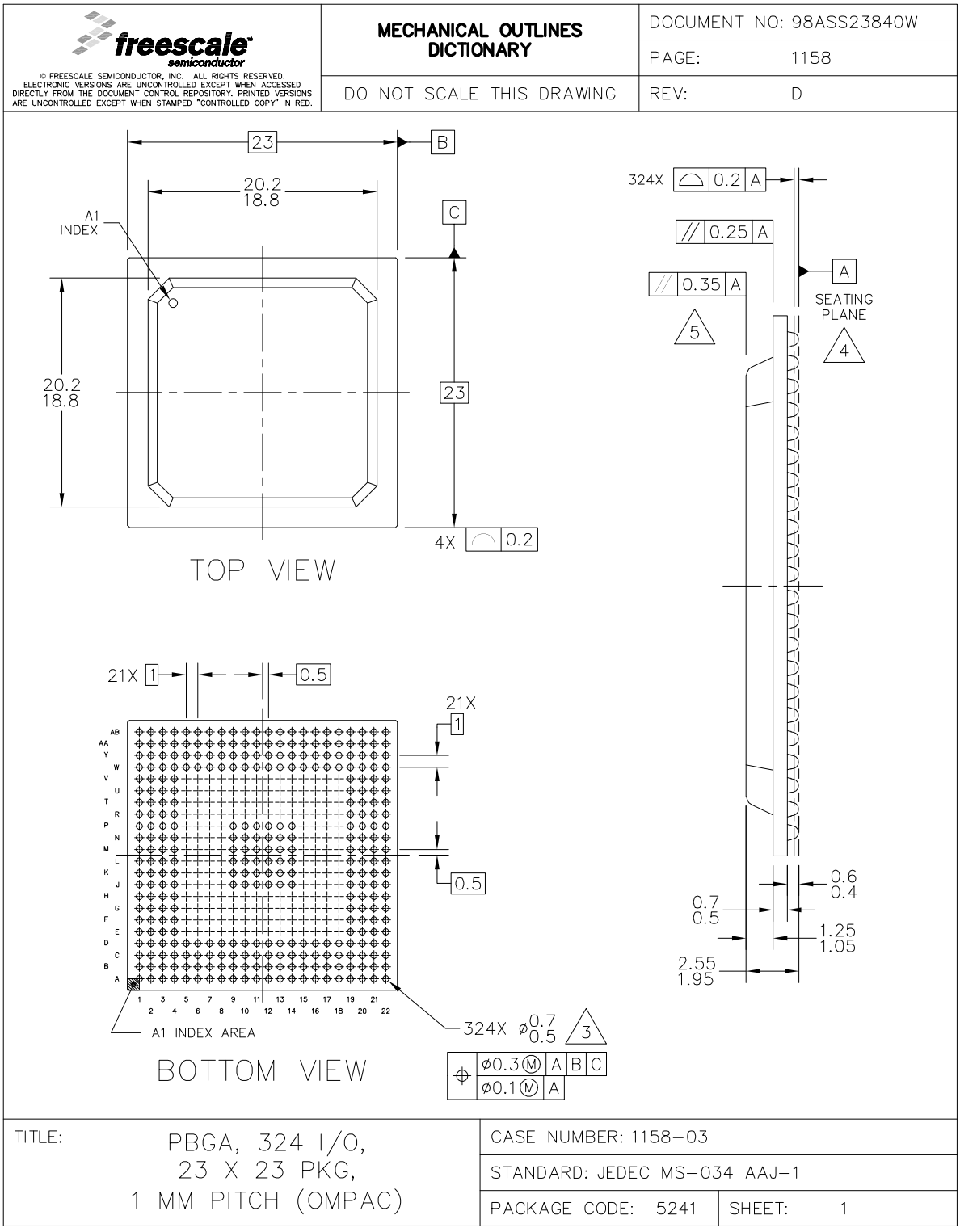


Figure 39. 324 BGA package mechanical drawing (part 1)