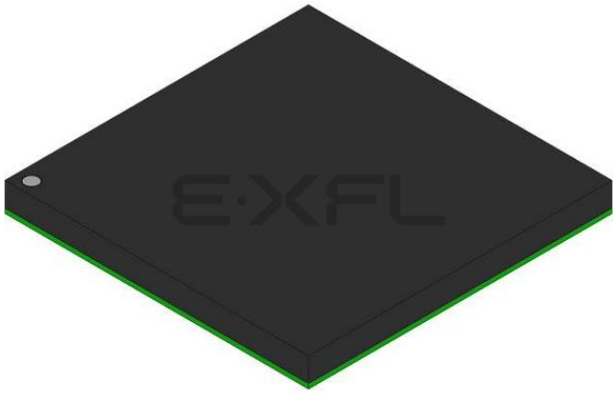

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5642af2mvz3

1 Addendum List for Revision 3.1

Table 1. MPC5642A Rev 3.1 Addendum

Location	Description
Section 3.11, “Temperature Sensor Electrical Characteristics”, Page 77	In “Temperature Sensor Electrical Characteristics” table, update the Min and Max value of “Accuracy” parameter to -20^{o}C and +20^{o}C, respectively.

2 Revision History

Table 2 provides a revision history for this datasheet addendum document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release.	12/2014

1.5.4 Interrupt controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors

  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 decimation filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface (SSI) to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports 6 queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.5.15 Deserial serial peripheral interface (DSPI)

The DSPI block provides a synchronous serial interface for communication between the MPC5642A MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the MPC5642A MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHz for SOUT and SCK pins for DSPI_B and DSPI_C
- Support for downstream Micro Second Channel (MSC) with Timed Serial Bus (TSB) configuration on DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels, and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI module can generate and check parity in a serial frame

Table 3. MPC5642A signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208	324
EMIOS6 ETPUA6_O GPIO[185]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	185	I/O O I/O	VDDEH4 / Slow	— / Down	— / Down	68	P7	AA14
EMIOS7 ETPUA7_O GPIO[186]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	186	I/O O I/O	VDDEH4 / Slow	— / Down	— / Down	69	—	AB14
EMIOS8 ETPUA8_O SCI_B_TX GPIO[187]	eMIOS channel eTPU A channel (output only) eSCI B transmit GPIO	P A1 A2 G	001 010 100 000	187	I/O O O I/O	VDDEH4 / Slow	— / Up	— / Up	70	P8	W15
EMIOS9 ETPUA9_O SCI_B_RX GPIO[188]	eMIOS channel eTPU A channel (output only) eSCI B receive GPIO	P A1 A2 G	001 010 100 000	188	I/O O I I/O	VDDEH4 / Slow	— / Up	— / Up	71	R7	Y15
EMIOS10 DSPI_D_PCS[3] RCH3_B GPIO[189]	eMIOS channel DSPI D peripheral chip select Reaction channel 3B GPIO	P A1 A2 G	001 010 100 000	189	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	73	N8	AA15
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	75	R8	AB15
EMIOS12 DSPI_C_SOUT ETPUA27_O GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	76	N10	AB16
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	77	T8	AA16
EMIOS14 IRQ[0] ETPUA29_O GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 / Slow	— / Down	— / Down	78	R9	Y16
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 / Slow	— / Down	— / Down	79	T9	W16
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	W17
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	Y17
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	AA17
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AB17

Table 6. Power/ground segmentation

Power segment	Voltage	I/O pins powered by segment
VDDE5	3.0 V – 3.6 V	DATA[0:15], CLKOUT, ENGCLK
VDDE12	3.0 V – 3.6 V	CAL_CS0, CAL_CS2, CAL_CS3, CAL_ADDR[12:30], CAL_DATA[0:15], CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V – 5.5 V	FR_A_TX, FR_A_TX_EN, FR_A_RX, FR_B_TX, FR_B_TX_EN, FR_B_RX
VDDEH1	3.3 V – 5.5 V	ETPUA[10:31]
VDDEH4	3.3 V – 5.5 V	EMIOS[0:23], TCRCLKA, ETPUA[0:9]
VDDEH6	3.3 V – 5.5 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_B_RX, SCI_C_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0:5], EXTAL, XTAL
VDDEH7	3.3 V – 5.5 V	EMIOS14, EMIOS15, GPIO[98:99], GPIO[203:204], GPIO[206], GPIO[207], GPIO[219], EVTI, EVTO, MDO[4:11], MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0:1], DSPI_A_PCS[4:5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK
VDDA	5.0 V	AN[0:11], AN[16:39], VRH, VRL, REFBYBC
VRC33	3.3 V	MCKO, MDO[0:3]
Other power segments		
VDDREG	5.0 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.9 V – 6.0 V	—
VSS	—	—

3.2 Maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD}	SR	1.2 V core supply voltage[2]		–0.3	1.32	V
V_{FLASH}	SR	Flash core voltage[3,4]		–0.3	3.6	V
V_{STBY}	SR	SRAM standby voltage[5]		–0.3	6.0	V
V_{DDPLL}	SR	Clock synthesizer voltage[3]		–0.3	1.32	V
V_{RC33}	SR	Voltage regulator control input voltage[4]		–0.3	3.6	V
V_{DDA}	SR	Analog supply voltage[5]	Reference to V_{SSA}	–0.3	5.5	V
V_{DDE}	SR	I/O supply voltage[4,6]		–0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage[5,7]		–0.3	5.5	V
V_{IN}	SR	DC input voltage[8]	V_{DDEH} powered I/O pads	–1.0[10]	V_{DDEH} + 0.3 V[9]	V
			V_{DDE} powered I/O pads	–1.0[14]	V_{DDE} + 0.3 V[10]	
			V_{DDA} powered I/O pads	–1.0	5.5	
V_{DDREG}	SR	Voltage regulator supply voltage		–0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	–0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		–0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage		–0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	V_{RL} to V_{SSA} differential voltage		–0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		–0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current[11]	Per pin, applies to all digital pins	–3	3	mA
I_{MAXA}	SR	Maximum DC analog input current[12]	Per pin, applies to all analog pins	—	5[13]	mA
T_J	SR	Maximum operating temperature range — die junction temperature		–40.0	150.0	°C
T_{STG}	SR	Storage temperature range		–55	150	°C
T_{SDR}	SR	Maximum solder temperature[14]		—	260	°C
MSL	SR	Moisture sensitivity level[15]		—	3	—

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V + 10%

3 The V_{FLASH} supply is connected to V_{RC33} in the package substrate. This specification applies to calibration package devices only.

4 Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V + 10%

5 Allowed 5.9 V for 10 hours cumulative time, remaining time at 5 V + 10%

Table 25. PLLMRFM electrical specifications[1]

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ILEXT}	CC	D	EXTAL input low voltage	Crystal mode[13]	—	Vxtal – 0.4	V
		T		External reference[13,14]	0	V_{RC33}/2 – 0.4	
—	CC	T	XTAL load capacitance	—	5	30	pF
—	CC	C	XTAL load capacitance[11]	4 MHz	5	30	pF
				8 MHz	5	26	
				12 MHz	5	23	
				16 MHz	5	19	
				20 MHz	5	16	
				40 MHz	5	8	
t_{lpll}	CC	P	PLL lock time[11,15]	—	—	200	µs
t_{dc}	CC	D	Duty cycle of reference	—	40	60	%
f_{LCK}	CC	D	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	D	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation depth	Center spread	±0.25	±4.0	% f_{sys}
		D		Down spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[16]	—	—	100	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed

3 All internal registers retain data at 0 Hz.

4 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

5 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

6 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

7 This value is determined by the crystal manufacturer and board design.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

9 Proper PC board layout procedures must be followed to achieve specifications.

10 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

11 This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this PLL, load capacitors should not exceed these limits.

12 Proper PC board layout procedures must be followed to achieve specifications.

13 This parameter is guaranteed by design rather than 100% tested.

Table 33. Flash EEPROM module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	D	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	CC	D	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	CC	D	Minimum data retention at 85 °C	Blocks with 0 – 1,000 P/E cycles	20	—	years
		D		Blocks with 10,000 P/E cycles	10	—	
		D		Blocks with 100,000 P/E cycles	5	—	

Table 35. Pad AC specifications (V_{DDE} = 3.0 V)[1]

Pad type		C	Output delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall edge (ns)[3,4]		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	—							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7,10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	—							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7,11] (High Swing Mode)	CC	D	—	3.7/3.1	—	10/10	30	11[8]
	CC	D	—	46/49	—	42/42	200	
	—							10[9]
	CC	D	—	32	—	15/15	50	01
	CC	D	—	72	—	46/46	200	
	CC	D	—	210	—	100/100	50	00
	CC	D	—	295	—	134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							
Fast	CC	D	—	2.5/2.5	—	1.2/1.2	10	00
	CC	D	—	2.5/2.5	—	1.2/1.2	20	01
	CC	D	—	2.5/2.5	—	1.2/1.2	30	10
	CC	D	—	2.5/2.5	—	1.2/1.2	50	11[8]
Standalone input buffer[12]	CC	D	0.5/0.5	3/3	0.4/0.4	±1.5/1.5	0.5	—

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 In high swing mode, high/low swing pad V_{OL} and V_{OH} values are the same as those of the slew controlled output pads.

6 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.

7 Output delay is shown in Figure 9 and Figure 10. Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Can be used on the tester.

9 This drive select value is not supported. If selected, it will be approximately equal to 11.

10 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.

11 Selectable high/low swing I/O pad with selectable slew in high swing mode only.

12 Also has weak pull-up/pull-down.

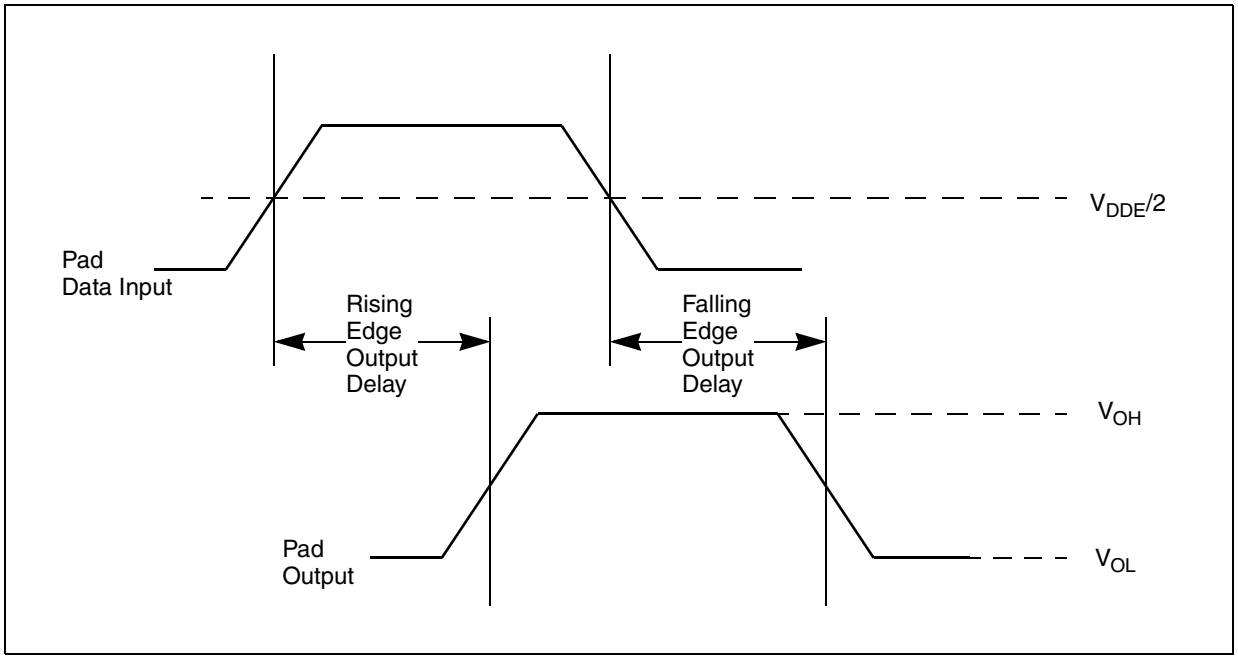

Figure 9. Pad output delay—Fast pads

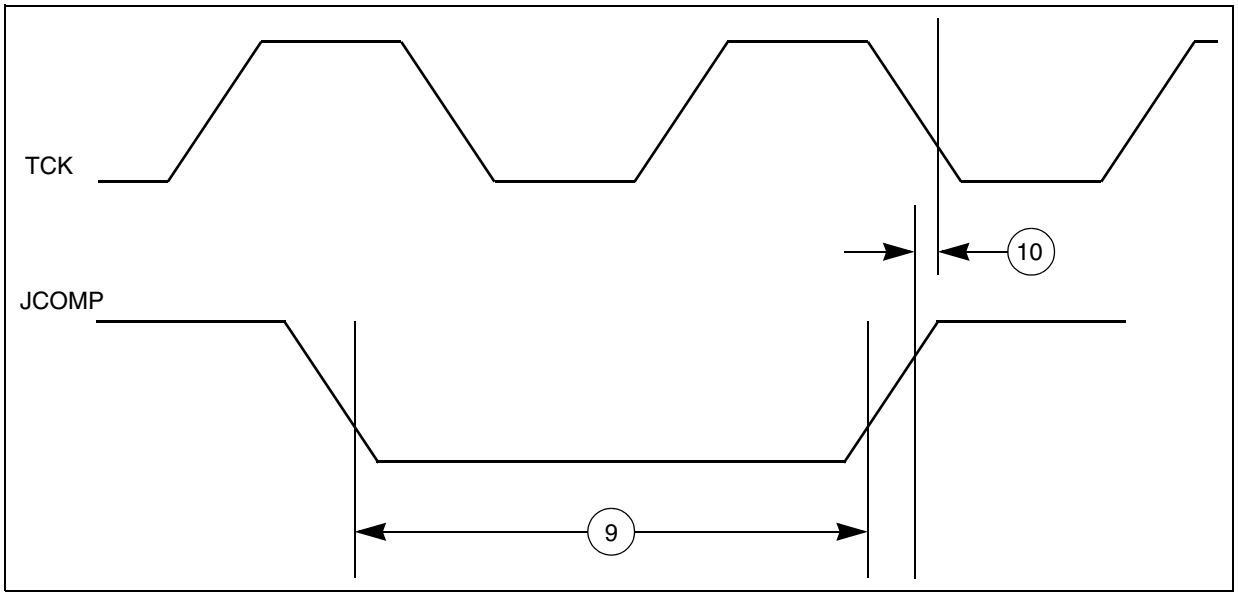

Figure 14. JTAG JCOMP timing

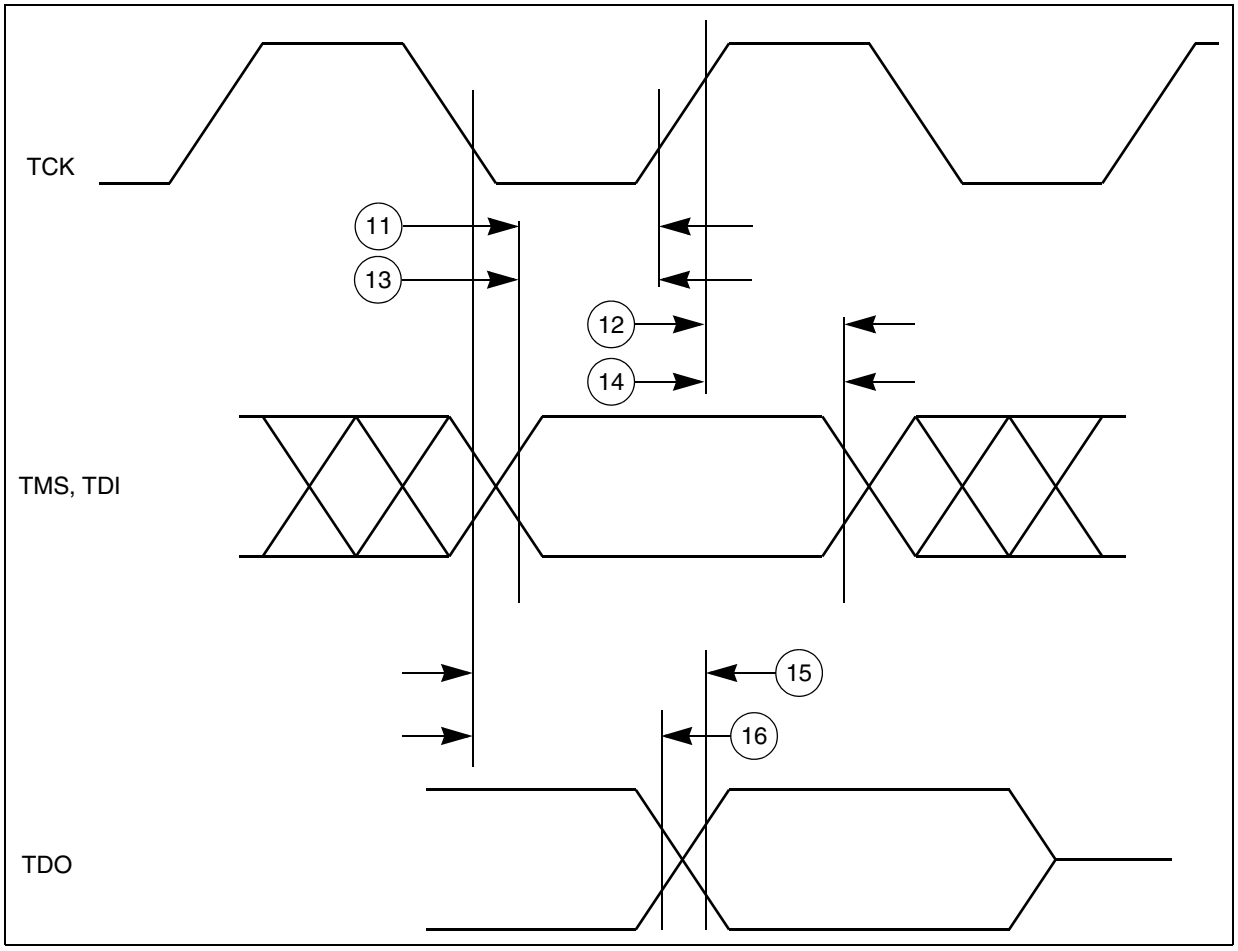

Figure 18. Nexus TDI, TMS, TDO timing

Table 39. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
176 LQFP 208 BGA 324 BGA	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
496 CSP	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
		Route to CAL_MDO[7]	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz[3]

1 NPC_PCR[FPM] = 0

2 NPC_PCR[NEXCFG] = 0

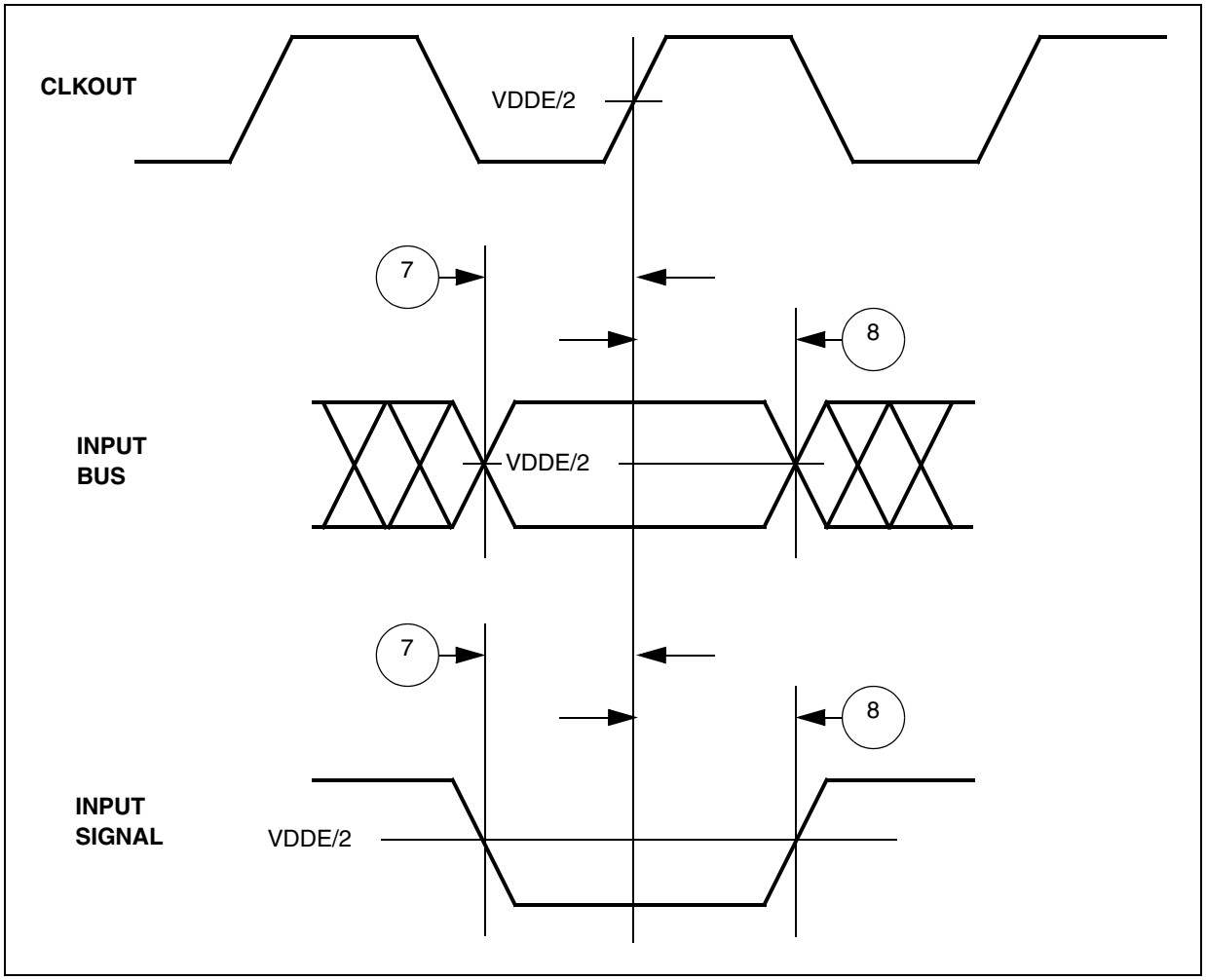

Figure 21. Synchronous input timing

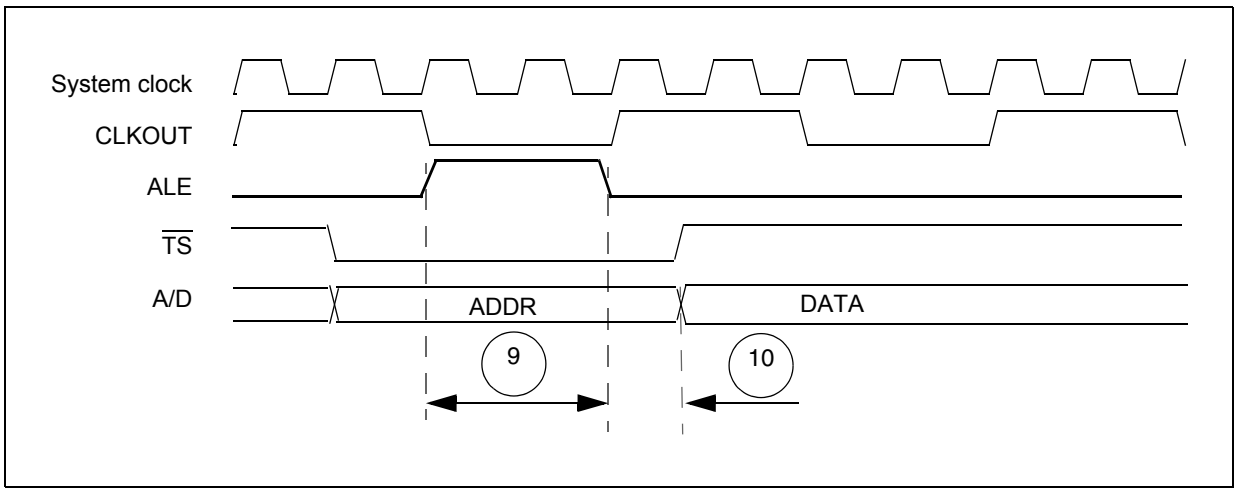

Figure 22. ALE signal timing

7 Timing met when PCSSCK = 3 (01), and CSSCK = 2 (0000)
8 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9 Timing met when ASC = 2 (0000), and PASC = 3 (01)
10 Timing met when PCSSCK = 3
11 Timing met when ASC = 3
12 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

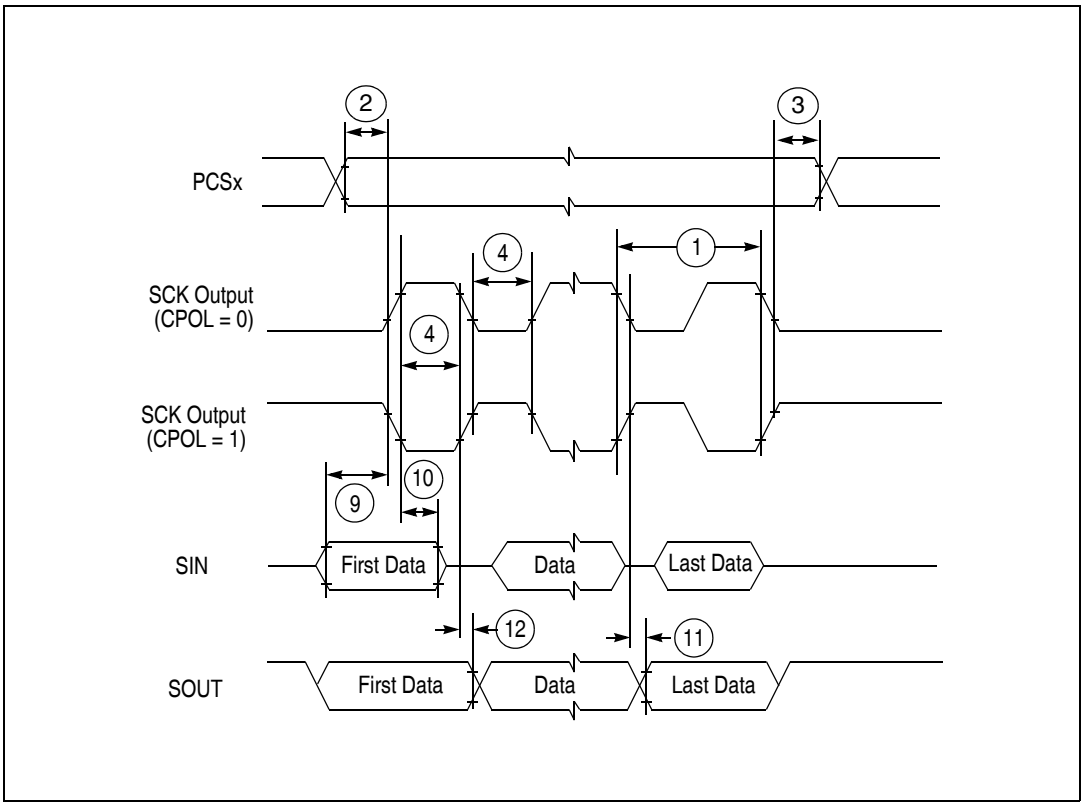

Figure 24. DSPI classic SPI timing (master, CPHA = 0)

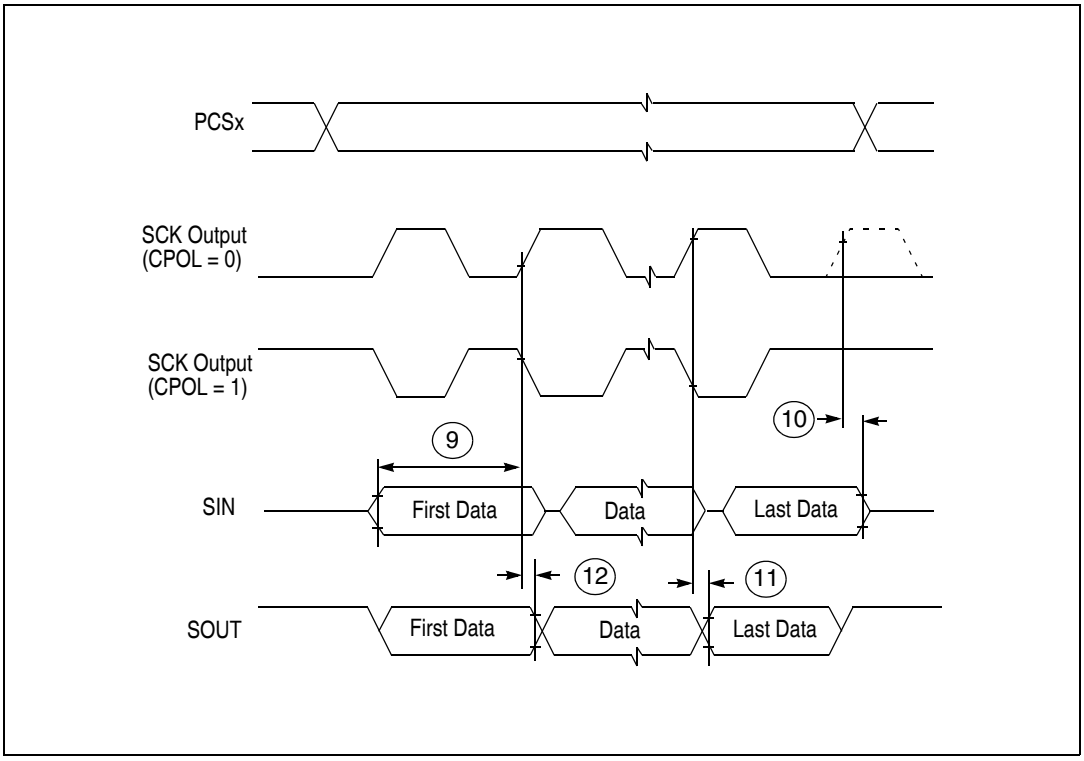

Figure 29. DSPI modified transfer format timing (master, CPHA = 1)

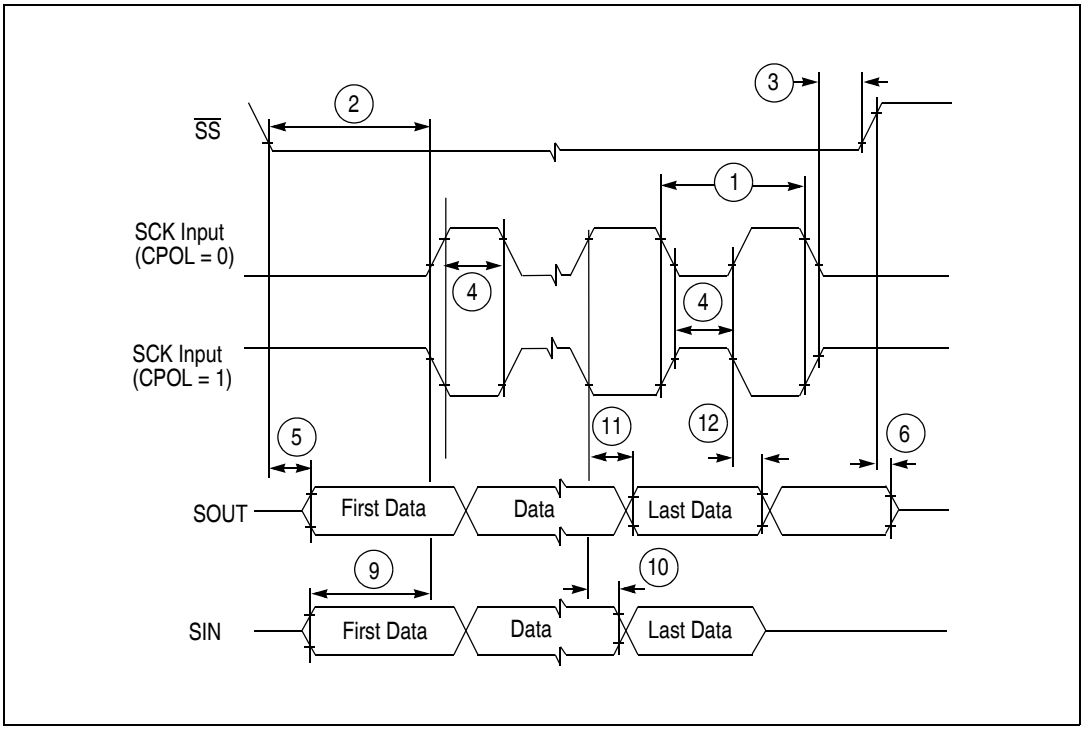

Figure 30. DSPI modified transfer format timing (slave, CPHA = 0)

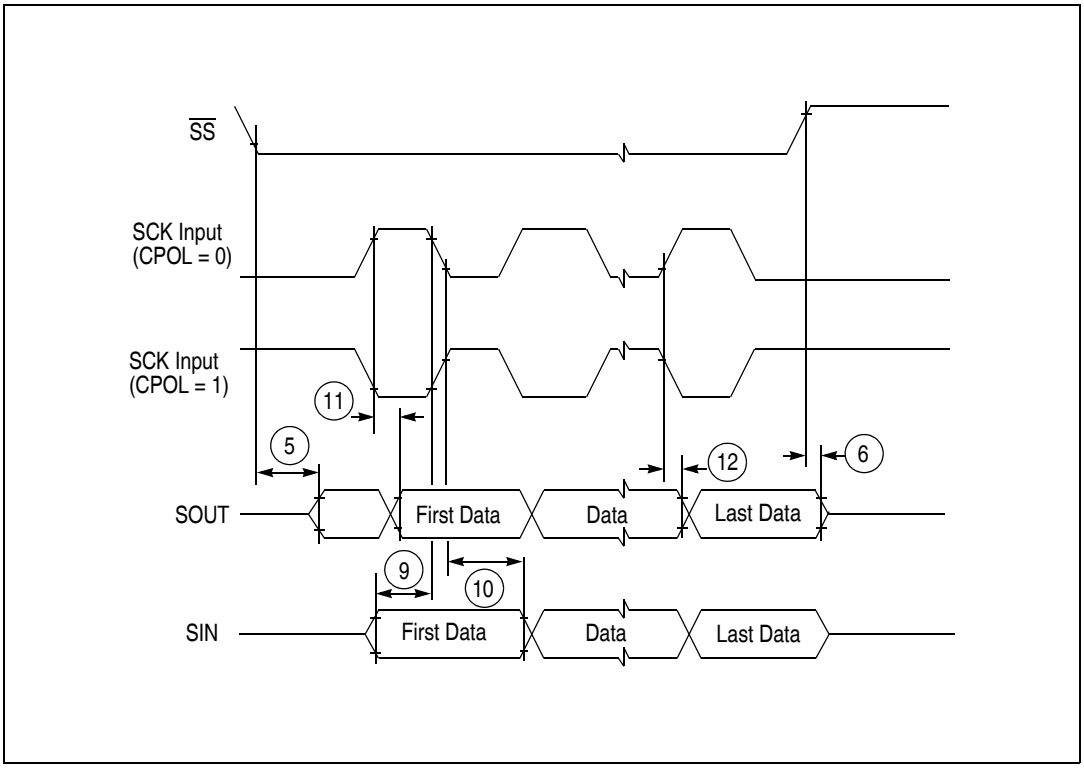

Figure 31. DSPI modified transfer format timing (slave, CPHA = 1)

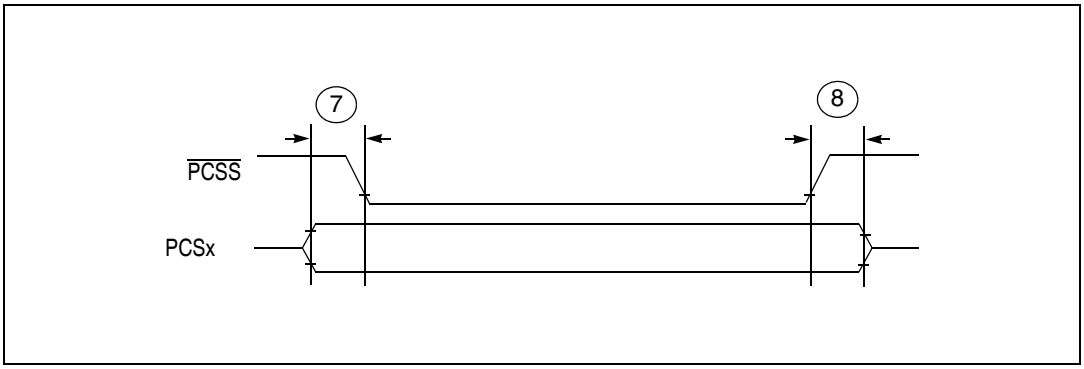

Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.17.10 FlexCAN system clock source

Table 48. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	f_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 49. FlexCAN engine system clock divider

System frequency	Required SIU_SYSDIV[CAN_SRC] value
$\leq f_{CAN\_TH}$	0[1,2]
$> f_{CAN\_TH}$	1[2,3]

1 Divides system clock source for FlexCAN engine by 1

2 System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1

3 Divides system clock source for FlexCAN engine by 2

Figure 34. 176 LQFP package mechanical drawing (part 1)

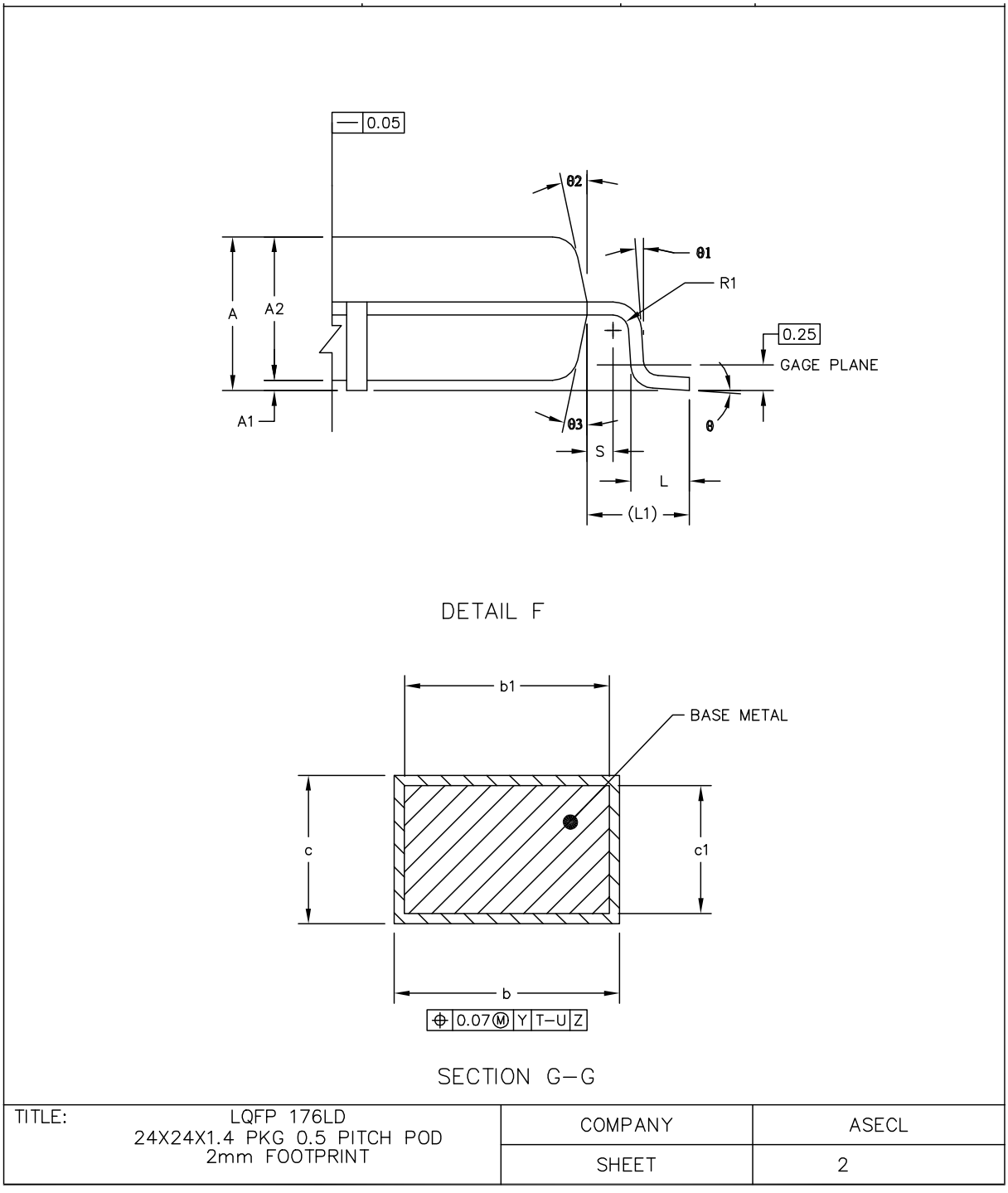

Figure 35. 176 LQFP package mechanical drawing (part 2)

4.1.3 324 TEPBGA

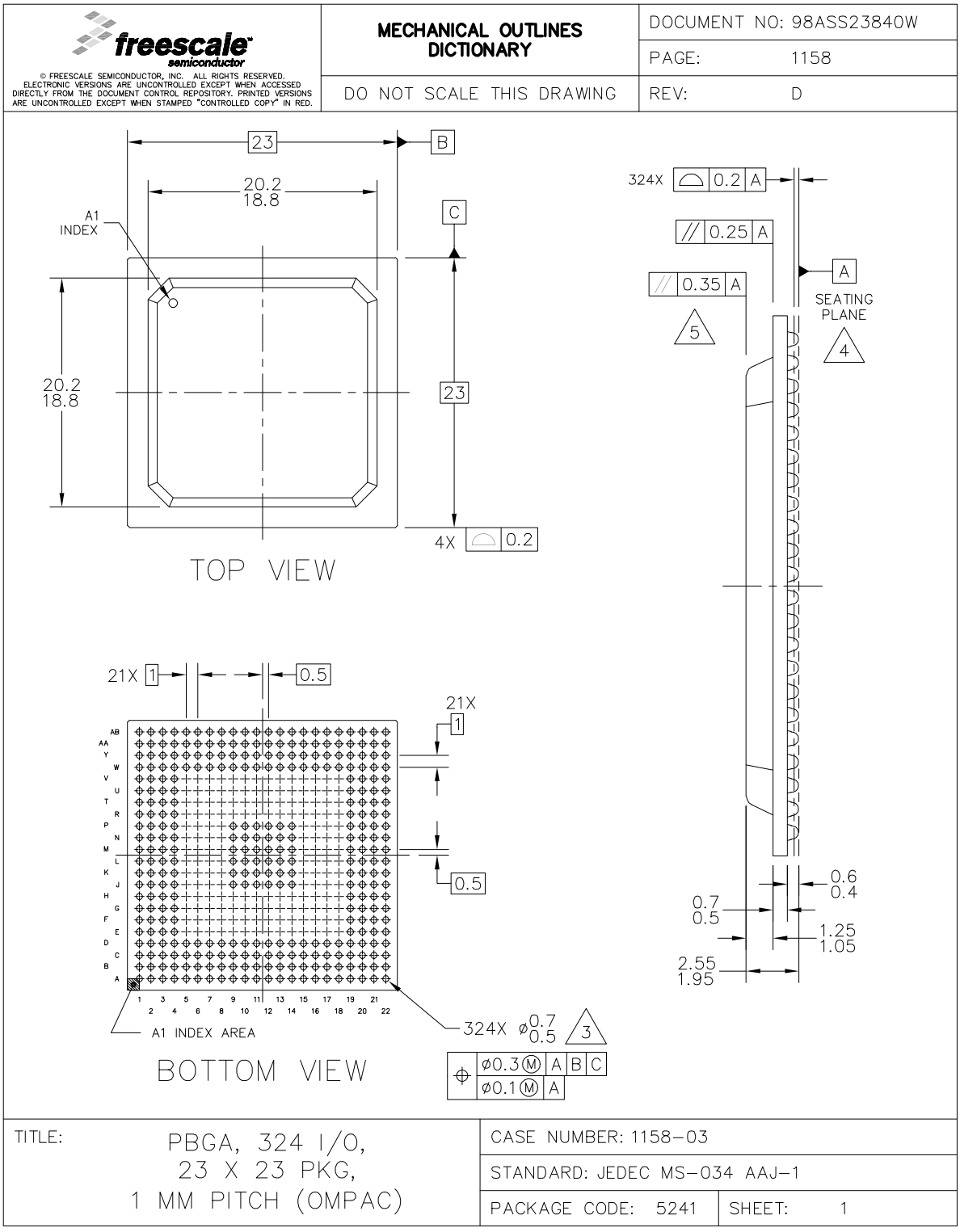

Figure 39. 324 BGA package mechanical drawing (part 1)