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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2623fa20jv

1.3 Pin Descriptions

1.3.1 Pin Arrangement

Figures 1.3 and 1.4 show pin arrangements of the H8S/2623 Group and H8S/2626 Group.

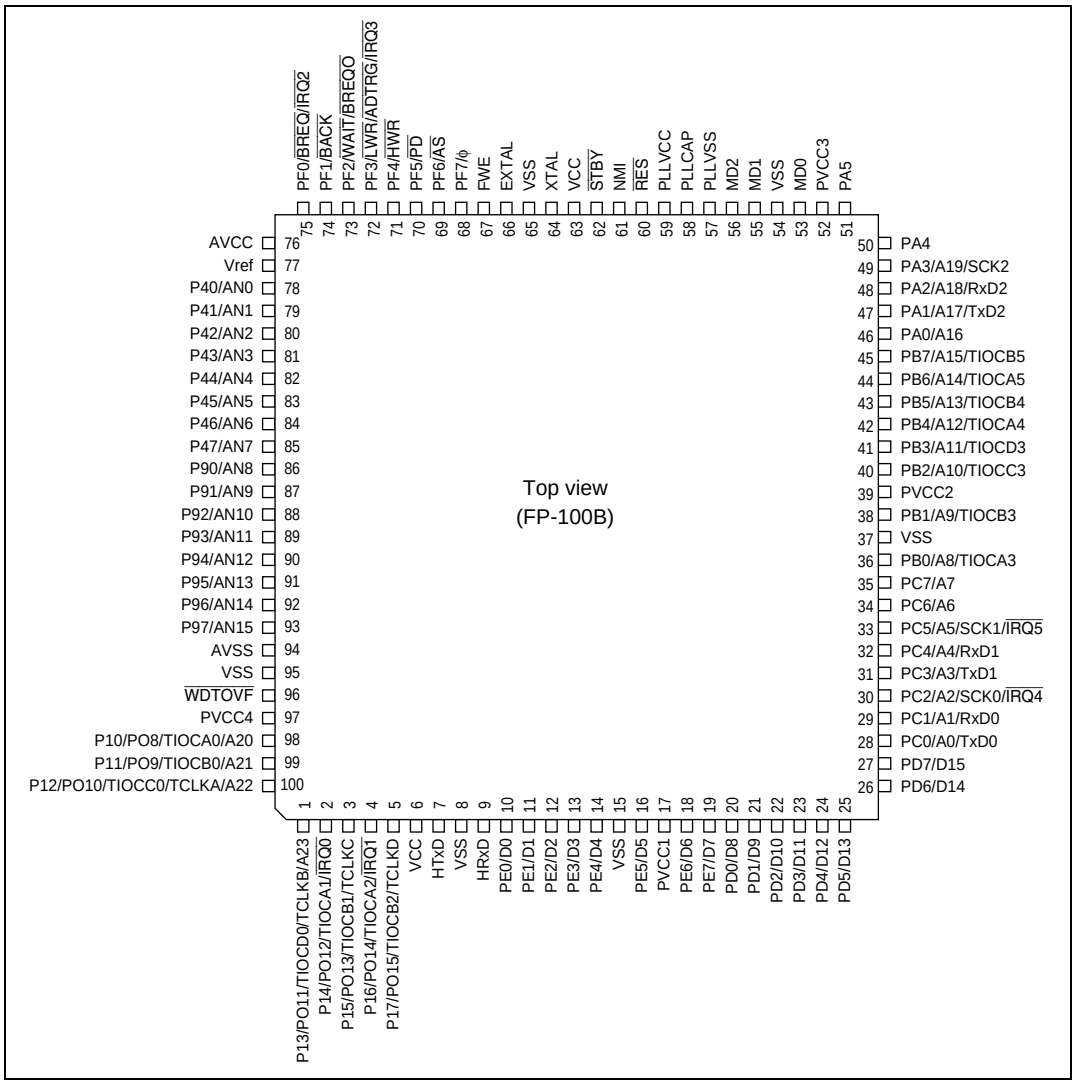


Figure 1.3 Pin Arrangement (FP-100B: Top View) (H8S/2623 Group)

Type	Instruction	Size*1	Function
System control instructions	TRAPA	—	Starts trap-instruction exception handling.
	RTE	—	Returns from an exception-handling routine.
	SLEEP	—	Causes a transition to a power-down state.
	LDC	B/W	(EAs) → CCR, (EAs) → EXR Moves the source operand contents or immediate data to CCR or EXR. Although CCR and EXR are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
	STC	B/W	CCR → (EAd), EXR → (EAd) Transfers CCR or EXR contents to a general register or memory. Although CCR and EXR are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
	ANDC	B	CCR ∧ #IMM → CCR, EXR ∧ #IMM → EXR Logically ANDs the CCR or EXR contents with immediate data.
	ORC	B	CCR ∨ #IMM → CCR, EXR ∨ #IMM → EXR Logically ORs the CCR or EXR contents with immediate data.
	XORC	B	CCR ⊕ #IMM → CCR, EXR ⊕ #IMM → EXR Logically exclusive-ORs the CCR or EXR contents with immediate data.
	NOP	—	PC + 2 → PC Only increments the program counter.

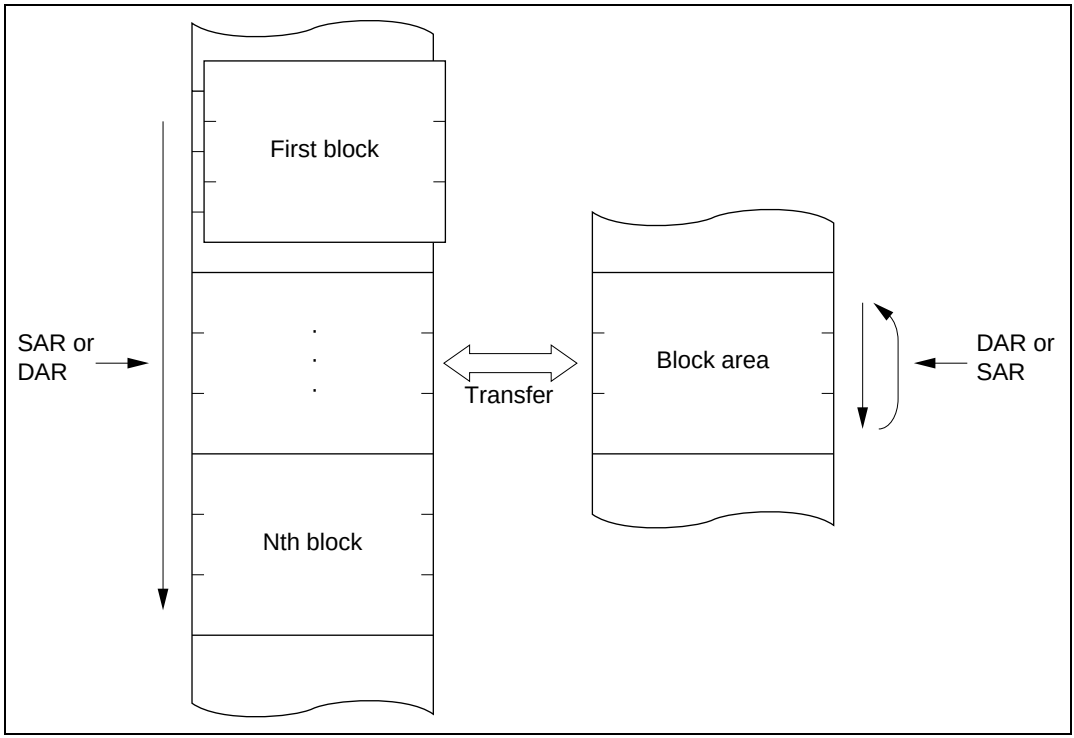


Figure 8.8 Memory Mapping in Block Transfer Mode

Figure 10.8 illustrates periodic counter operation.

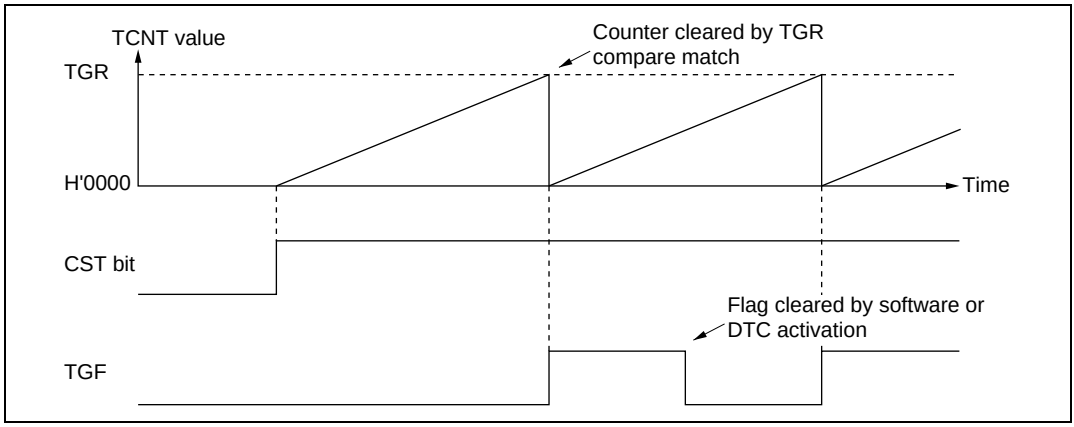


Figure 10.8 Periodic Counter Operation

Waveform Output by Compare Match: The TPU can perform 0, 1, or toggle output from the corresponding output pin using compare match.

- Example of setting procedure for waveform output by compare match

  Figure 10.9 shows an example of the setting procedure for waveform output by compare match

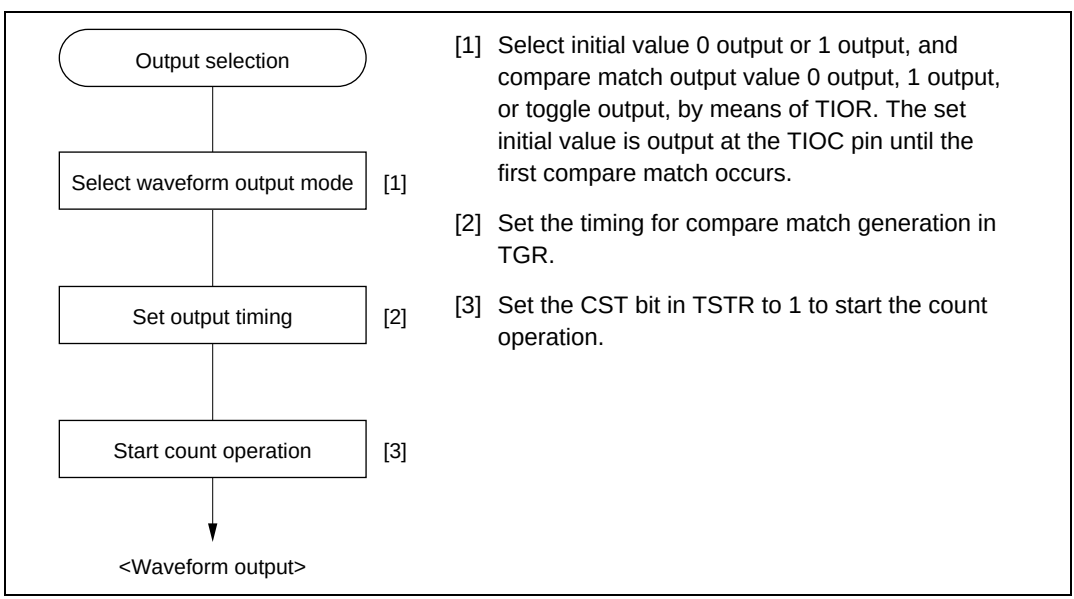


Figure 10.9 Example of Setting Procedure for Waveform Output by Compare Match

12.3 Operation

12.3.1 Watchdog Timer Operation

To use the WDT as a watchdog timer, set the WT/$\overline{IT}$ bit in TCSR and TME bit to 1. Software must prevent TCNT overflows by rewriting the TCNT value (normally be writing H'00) before overflows occurs. This ensures that TCNT does not overflow while the system is operating normally. If TCNT overflows without being rewritten because of a system crash or other error, in the WDT0 the $\overline{WDTOVF}$ signal is output. This is shown in figure 12.4 (a). This $\overline{WDTOVF}$ signal can be used to reset the system. The $\overline{WDTOVF}$ signal is output for 132 states when RSTE = 1, and for 130 states when RSTE = 0.

If TCNT overflows when 1 is set in the RSTE bit in RSTCSR, a signal that resets the chip internally is generated at the same time as the $\overline{WDTOVF}$ signal. This reset can be selected as a power-on reset or a manual reset, depending on the setting of the RSTS bit in RSTCSR. The internal reset signal is output for 518 states.

If a reset caused by a signal input to the $\overline{RES}$ pin occurs at the same time as a reset caused by a WDT overflow, the $\overline{RES}$ pin reset has priority and the WOVF bit in RSTCSR is cleared to 0.

In the case of WDT1, the chip is reset, or an NMI interrupt request is generated, for 516 system clock periods (516ϕ) (515 or 516 states when the clock source is ϕSUB (PSS = 1)). This is illustrated in figure 12.4 (b).

An NMI request from the watchdog timer and an interrupt request from the NMI pin are both treated as having the same vector. So, avoid handling an NMI request from the watchdog timer and an interrupt request from the NMI pin at the same time.

13.1.3 Pin Configuration

Table 13.1 shows the serial pins for each SCI channel.

Table 13.1 SCI Pins

Channel	Pin Name	Symbol*	I/O	Function
0	Serial clock pin 0	SCK0	I/O	SCI0 clock input/output
	Receive data pin 0	RxD0	Input	SCI0 receive data input
	Transmit data pin 0	TxD0	Output	SCI0 transmit data output
1	Serial clock pin 1	SCK1	I/O	SCI1 clock input/output
	Receive data pin 1	RxD1	Input	SCI1 receive data input
	Transmit data pin 1	TxD1	Output	SCI1 transmit data output
2	Serial clock pin 2	SCK2	I/O	SCI2 clock input/output
	Receive data pin 2	RxD2	Input	SCI2 receive data input
	Transmit data pin 2	TxD2	Output	SCI2 transmit data output

Note: * Pin names SCK, RxD, and TxD are used in the text for all channels, omitting the channel designation.

Bit 5

PE	Description	
0	Parity bit addition and checking disabled	(Initial value)
1	Parity bit addition and checking enabled*	

Note: * When the PE bit is set to 1, the parity (even or odd) specified by the O/$\overline{E}$ bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/$\overline{E}$ bit.

Bit 4—Parity Mode (O/$\overline{E}$): Selects either even or odd parity for use in parity addition and checking.

The O/$\overline{E}$ bit setting is only valid when the PE bit is set to 1, enabling parity bit addition and checking, in asynchronous mode. The O/$\overline{E}$ bit setting is invalid in clocked synchronous mode, when parity addition and checking is disabled in asynchronous mode, and when a multiprocessor format is used.

Bit 4

O/$\overline{E}$	Description	
0	Even parity*1	(Initial value)
1	Odd parity*2	

Notes: 1. When even parity is set, parity bit addition is performed in transmission so that the total number of 1 bits in the transmit character plus the parity bit is even.
In reception, a check is performed to see if the total number of 1 bits in the receive character plus the parity bit is even.
2. When odd parity is set, parity bit addition is performed in transmission so that the total number of 1 bits in the transmit character plus the parity bit is odd.
In reception, a check is performed to see if the total number of 1 bits in the receive character plus the parity bit is odd.

Bit 3—Stop Bit Length (STOP): Selects 1 or 2 bits as the stop bit length in asynchronous mode. The STOP bits setting is only valid in asynchronous mode. If clocked synchronous mode is set the STOP bit setting is invalid since stop bits are not added.

Bit 3

STOP	Description	
0	1 stop bit: In transmission, a single 1 bit (stop bit) is added to the end of a transmit character before it is sent.	(Initial value)
1	2 stop bits: In transmission, two 1 bits (stop bits) are added to the end of a transmit character before it is sent.	

17.2.3 Module Stop Control Register C (MSTPCRC)

Bit	:	7	6	5	4	3	2	1	0
		MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCRC is an 8-bit readable/writable register that performs module stop mode control.

When the MSTPC5 bit is set to 1, D/A converter operation is stopped at the end of the bus cycle, and module stop mode is entered. Register read/write accesses are not possible in module stop mode. For details, see section 21B.5, Module Stop Mode.

MSTPCRC is initialized to H'FF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 5—Module Stop (MSTPC5): Specifies module stop mode for the D/A converter (channels 2 and 3).

Bit 5

MSTPC5	Description	
0	D/A converter (channels 2 and 3) module stop mode is cleared	
1	D/A converter (channels 2 and 3) module stop mode is set	(Initial value)

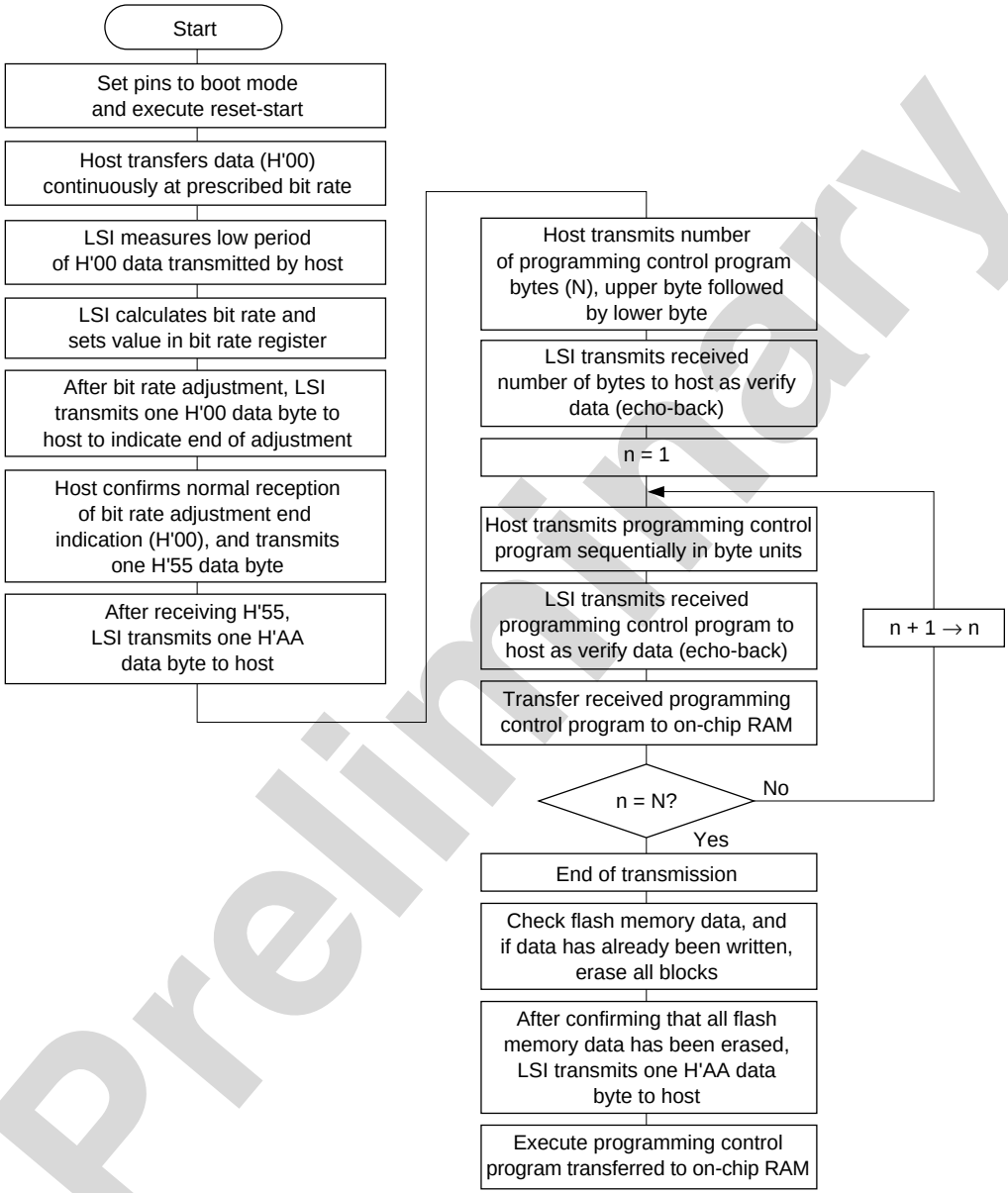
17.3 Operation

The D/A converter has two built-in D/A conversion circuits that can perform conversion independently.

D/A conversion is performed constantly while enabled in DACR23. If the DADR2 or DADR3 value is modified, conversion of the new data begins immediately. The conversion results are output when bits DAOE0 and DAOE1 are set to 1.

An example of D/A conversion on channel 2 is given below. The timing is shown in figure 17.2.

1. Data to be converted is written in DADR2.
2. Bit DAOE0 is set to 1 in DACR23. D/A conversion starts and DA2 becomes an output pin. The conversion result is output after the conversion time. The output value is (DADR2 contents/256) × Vref. Output of this conversion result continues until the value in DADR2 is modified or the DAOE0 bit is cleared to 0.



Note: If a memory cell does not operate normally and cannot be erased, one H'FF byte is transmitted as an erase error, and the erase operation and subsequent operations are halted.

Figure 19.7 Boot Mode Execution Procedure

Figure 19.13 shows the flash memory state transition diagram.

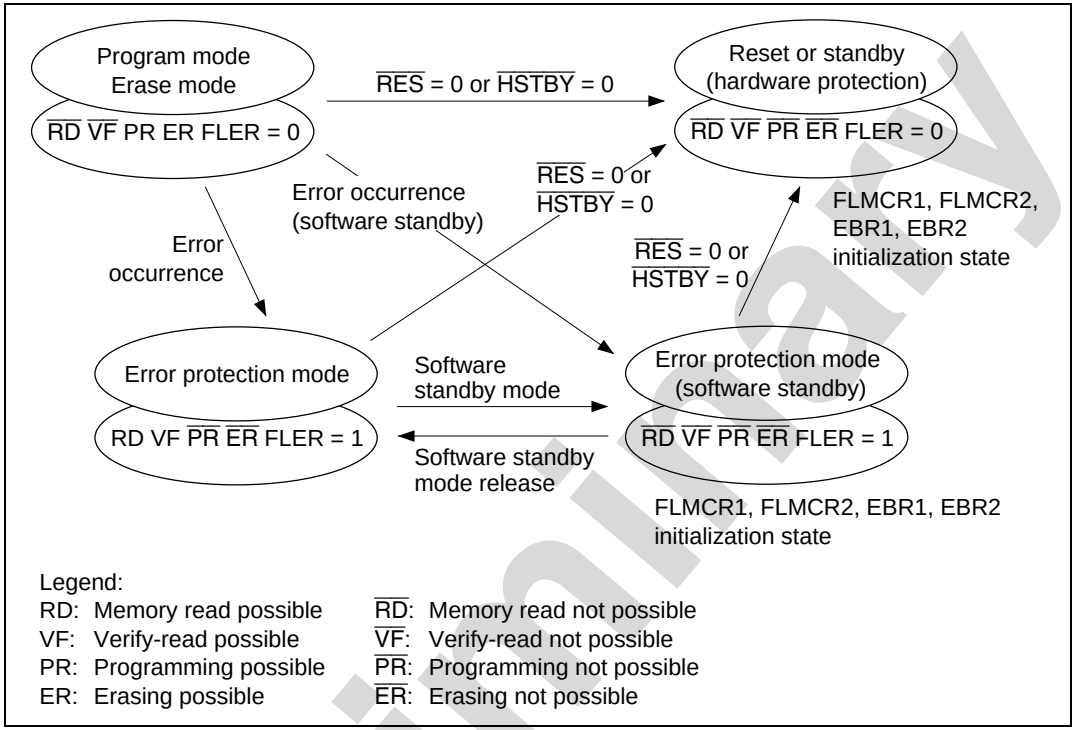


Figure 19.13 Flash Memory State Transitions

Table 21B.2 Power-Down Mode Transition Conditions

Pre-Transition State	Status of Control Bit at Transition				State After Transition Invoked by SLEEP Command	State After Transition Back from Power-Down Mode Invoked by Interrupt
	SSBY	PSS	LSON	DTON		
High-speed/ Medium-speed	0	*	0	*	Sleep	High-speed/Medium-speed
	0	*	1	*	—	—
	1	0	0	*	Software standby	High-speed/Medium-speed
	1	0	1	*	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Sub-active
	1	1	0	1	—	—
	1	1	1	1	Sub-active	—
Sub-active	0	0	*	*	—	—
	0	1	0	*	—	—
	0	1	1	*	Sub-sleep	Sub-active
	1	0	*	*	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Sub-active
	1	1	0	1	High-speed	—
	1	1	1	1	—	—

Legend:

—: Do not set.

*: Don’t care

Table 22.3 Permissible Output Currents — Preliminary —

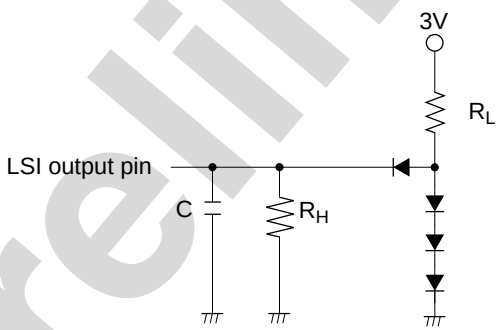
Conditions: V_{CC} = $PLLV_{CC}$ = 3.0 V to 3.6 V, PV_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*

Item			Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	PV_{CC} = 4.5 V to 5.5 V	I_{OL}	—	—	10	mA
Permissible output low current (total)	Total of all output pins	PV_{CC} = 4.5 V to 5.5 V	ΣI_{OL}	—	—	100	mA
Permissible output high current (per pin)	All output pins	PV_{CC} = 4.5 V to 5.5 V	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	PV_{CC} = 4.5 V to 5.5 V	$\Sigma -I_{OH}$	—	—	30	mA

Note: * To protect chip reliability, do not exceed the output current values in table 22.3.

22.3 AC Characteristics

Figure 22.1 show, the test conditions for the AC characteristics.



C = 50 pF: Ports 10 to 13, A to F
(In case of expansion bus control signal output pin setting)
C = 30 pF: All ports
R_L = 2.4 kΩ
R_H = 12 kΩ
Input/output timing measurement levels
- Low level : 0.8 V
- High level : 2.0 V

Figure 22.1 Output Load Circuit

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte	10th byte
MOV	MOV.W @ERs+,Rd	W	6	D	0 ers	rd														
	MOV.W @aa:16,Rd	W	6	B	0	rd														
	MOV.W @aa:32,Rd	W	6	B	2	rd	abs													
	MOV.W Rs,@ERd	W	6	9	1 erd	rs														
	MOV.W Rs,@(d:16,ERd)	W	6	F	1 erd	rs														
	MOV.W Rs,@(d:32,ERd)	W	7	8	0 erd	0	6	B	A	rs	disp									
	MOV.W Rs,@-ERd	W	6	D	1 erd	rs														
	MOV.W Rs,@aa:16	W	6	B	8	rs														
	MOV.W Rs,@aa:32	W	6	B	A	rs	abs													
	MOV.L #xx:32,Rd	L	7	A	0	0 erd	IMM													
	MOV.L ERs,ERd	L	0	F	1 ers	0 erd														
	MOV.L @ERs,ERd	L	0	1	0	0	6	9	0 ers	0 erd										
	MOV.L @(d:16,ERs),ERd	L	0	1	0	0	6	F	0 ers	0 erd	disp									
	MOV.L @(d:32,ERs),ERd	L	0	1	0	0	7	8	0 ers	0	6	B	2	0 erd	disp					
	MOV.L @ERs+,ERd	L	0	1	0	0	6	D	0 ers	0 erd										
	MOV.L @aa:16 ,ERd	L	0	1	0	0	6	B	0	0 erd	abs									
	MOV.L @aa:32 ,ERd	L	0	1	0	0	6	B	2	0 erd	abs									
	MOV.L ERs,@ERd	L	0	1	0	0	6	9	1 erd	0 ers										
	MOV.L ERs,@(d:16,ERd)	L	0	1	0	0	6	F	1 erd	0 ers	disp									
	MOV.L ERs,@(d:32,ERd)*1	L	0	1	0	0	7	8	0 erd	0	6	B	A	0 ers	disp					
	MOV.L ERs,@-ERd	L	0	1	0	0	6	D	1 erd	0 ers										
	MOV.L ERs,@aa:16	L	0	1	0	0	6	B	8	0 ers	abs									
	MOV.L ERs,@aa:32	L	0	1	0	0	6	B	A	0 ers	abs									
MOVFPE	MOVFPE @aa:16,Rd	B	Cannot be used in the H8S/2626 Group or H8S/2623 Group.																	
MOVTPE	MOVTPE Rs,@aa:16	B																		
MULXS	MULXS.B Rs,Rd	B	0	1	C	0	5	0	rs	rd										
	MULXS.W Rs,ERd	W	0	1	C	0	5	2	rs	0 erd										
MULXU	MULXU.B Rs,Rd	B	5	0	rs	rd														
	MULXU.W Rs,ERd	W	5	2	rs	0 erd														

SCR0—Serial Control Register 0 H'FF7A Smart Card Interface

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock enable

SCMR	SMR	SCR Setting		SCK Pin Function
SMIF	C/$\overline{A}$, GM	CKE1	CKE0	
0				See the SCI specification
1	0	0	0	Operates as port I/O pin
			1	Outputs clock as SCK output pin
	1		0	Operates as SCK output pin, with output fixed low
			1	Outputs clock as SCK output pin
		1	0	Operates as SCK output pin, with output fixed high
			1	Outputs clock as SCK output pin

Transmit end interrupt enable

0	Transmit end interrupt (TEI) request disabled
1	Transmit end interrupt (TEI) request enabled

Multiprocessor interrupt enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive enable

0	Reception disabled
1	Reception enabled

Transmit enable

0	Transmission disabled
1	Transmission enabled

Receive interrupt enable

0	Receive data full interrupt (RXI) request and receive error interrupt (ERI) request disabled
1	Receive data full interrupt (RXI) request and receive error interrupt (ERI) request enabled

Transmit interrupt enable

0	Transmit data empty interrupt (TXI) request disabled
1	Transmit data empty interrupt (TXI) request enabled

Note: For details of how to clear interrupt requests, see section 13.2.6, Serial Control Register (SCR).

SMR2—Serial Mode Register 2 **H'FF88** **Smart Card Interface**

Bit :	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock select

0	0	φ clock
	1	φ/4 clock
1	0	φ/16 clock
	1	φ/64 clock

Basic clock pulse

0	0	32 clock periods
	1	64 clock periods
1	0	372 clock periods
	1	256 clock periods

Parity mode

0	Even parity*1
1	Odd parity*2

Notes: 1. When even parity is set, parity bit addition is performed in transmission so that the total number of 1 bits in the transmit character plus the parity bit is even.
In reception, a check is performed to see if the total number of 1 bits in the receive character plus the parity bit is even.
2. When odd parity is set, parity bit addition is performed in transmission so that the total number of 1 bits in the transmit character plus the parity bit is odd.
In reception, a check is performed to see if the total number of 1 bits in the receive character plus the parity bit is odd.

Parity enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Note: When the smart card interface is used, be sure to make the 1 setting.

Block transfer mode

0	Normal smart card interface mode operation • Error signal transmission/detection and automatic data retransmission performed • TXI interrupt generated by TEND flag • TEND flag set 12.5 etu after start of transmission (11.0 etu in GSM mode)
1	Block transfer mode operation • Error signal transmission/detection and automatic data retransmission not performed • TXI interrupt generated by TDRE flag • TEND flag set 11.5 etu after start of transmission (11.0 etu in GSM mode)

GSM mode

0	Normal smart card interface mode operation • TEND flag generation 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generation 11.0 etu after beginning of start bit • High/low fixing control possible in addition to clock output on/off control (set by SCR)

Note: etu: Elementary Time Unit (time for transfer of 1 bit)

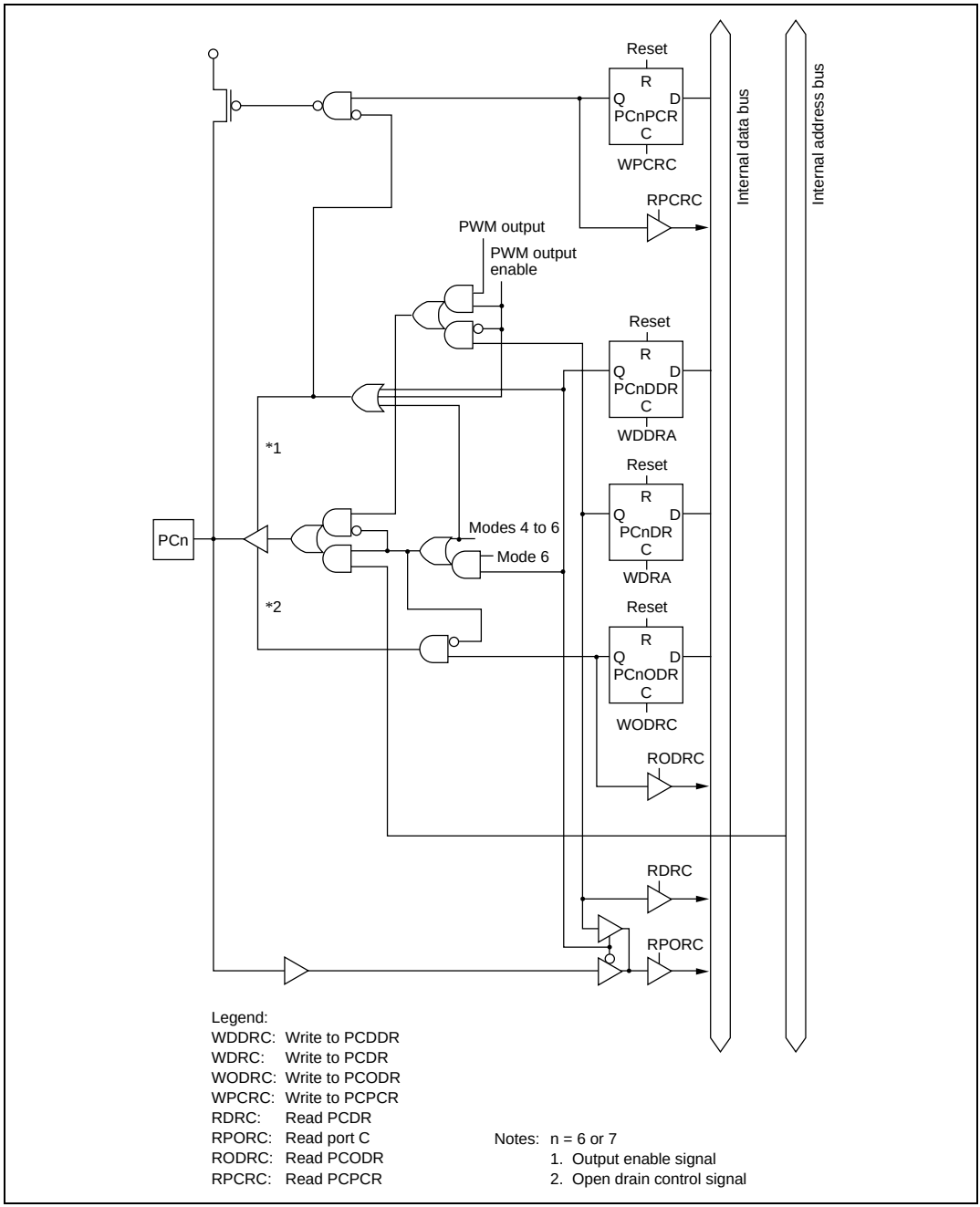


Figure C.6 (d) Port C Block Diagram (Pins PC6 and PC7)

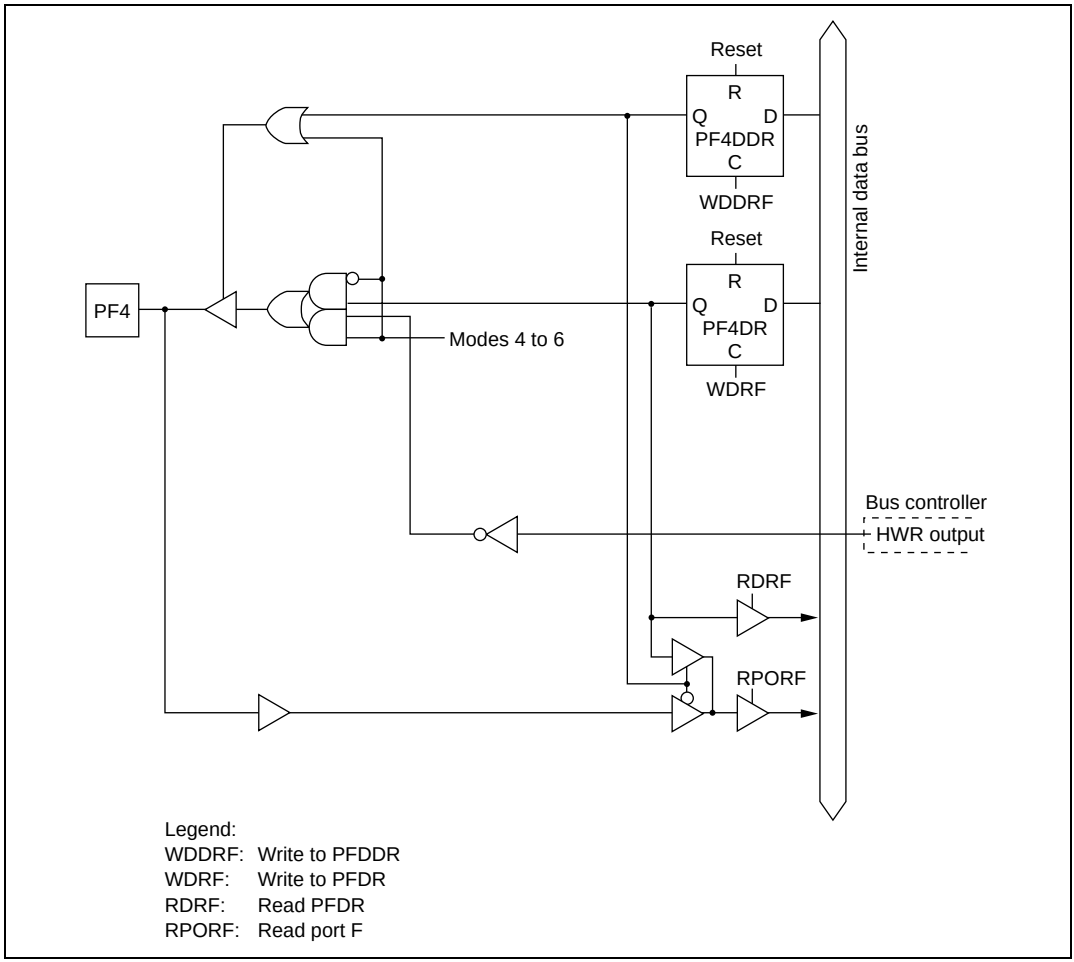
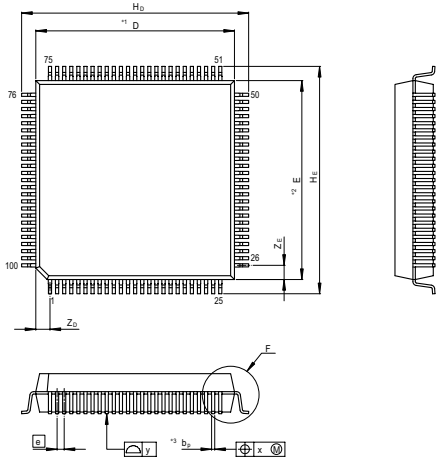


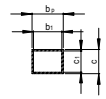
Figure C.9 (f) Port F Block Diagram (Pin PF4)

Appendix G Package Dimensions

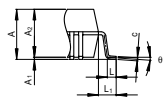
Figure G.1 shows the FP-100B package dimensions of the H8S/2626 Group and H8S/2623 Group.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x14-0.50	PRQP0100KA-A	FP-100B/FP-100BV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	2.70	—
H_D	15.7	16.0	16.3
H_E	15.7	16.0	16.3
A	—	—	3.05
A_1	0.00	0.12	0.25
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure G.1 FP-100B Package Dimensions