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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e051ddg

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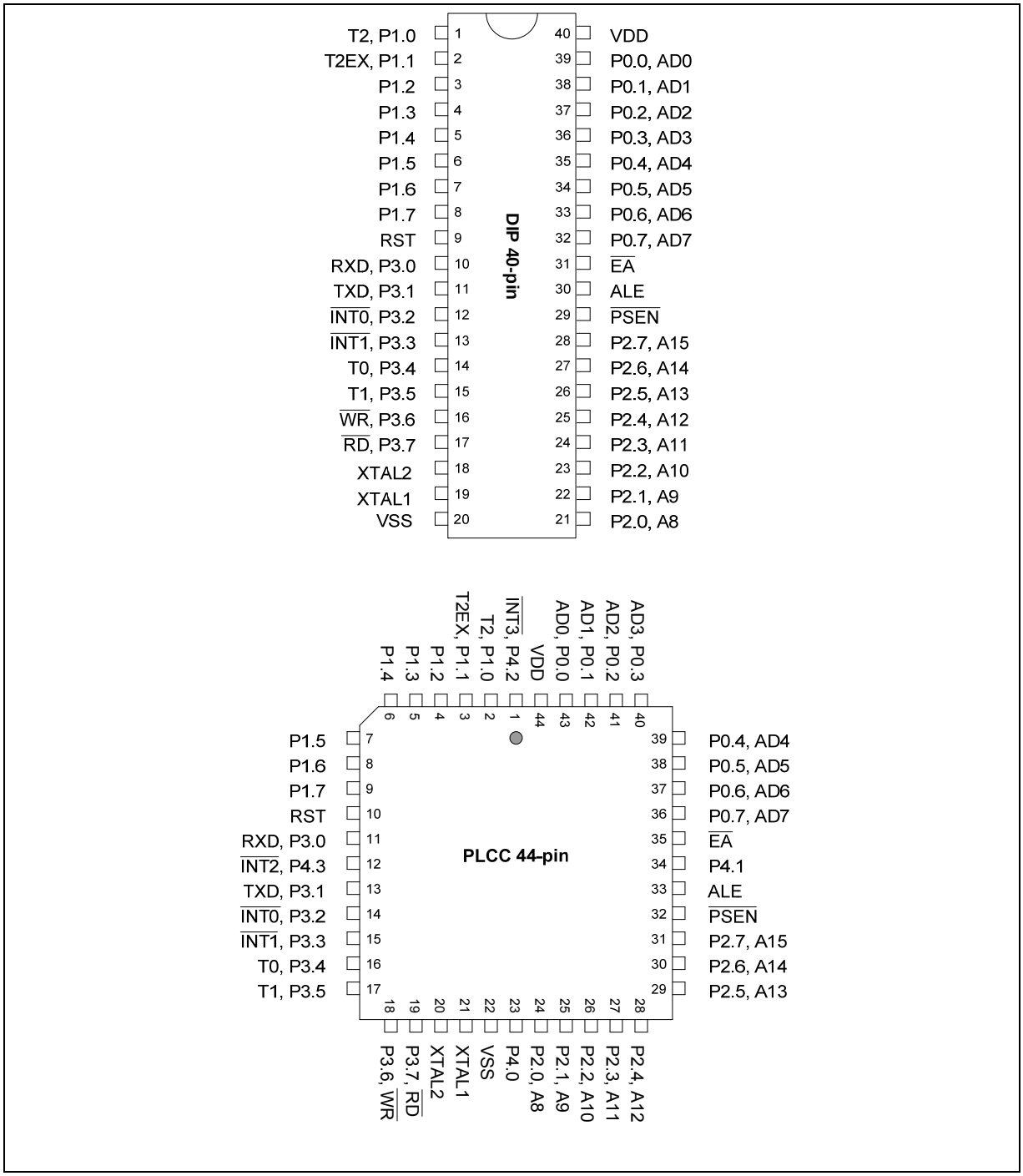
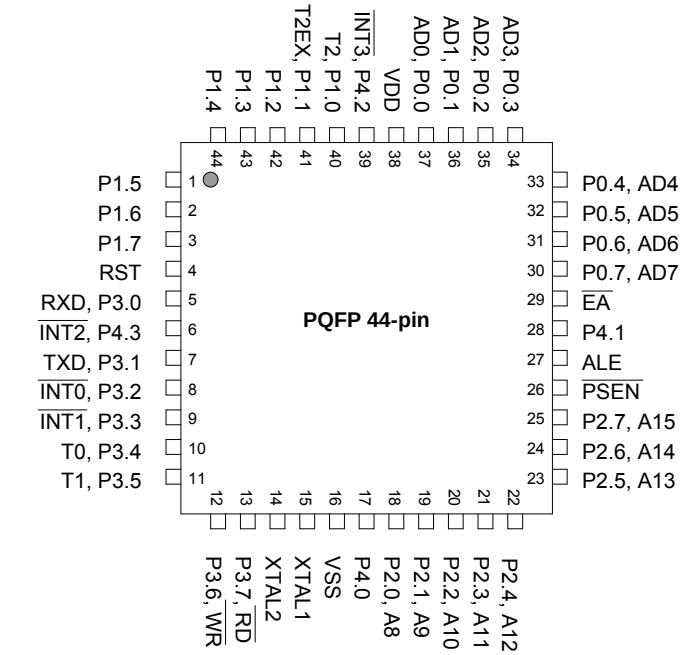
3 PARTS INFORMATION LIST

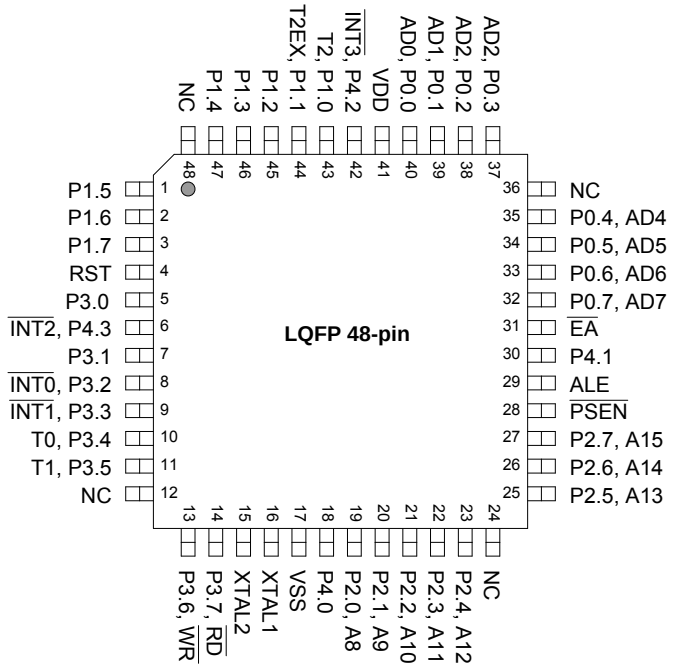
PART NO.	RAM	LDROM SIZE	APROM SIZE	PACKAGE	Temperature grade
W78E054DDG	256 Bytes	2K Bytes	14K Bytes	DIP-40 Pin	-40°C~85°C
		0	16K Bytes		
W78E054DPG		2K Bytes	14K Bytes	PLCC-44 Pin	-40°C~85°C
		0	16K Bytes		
W78E054DFG		2K Bytes	14K Bytes	PQFP-44 Pin	-40°C~85°C
		0	16K Bytes		
W78E054DLG		2K Bytes	14K Bytes	LQFP-48 Pin	-40°C~85°C
		0	16K Bytes		
W78E052DDG		2K Bytes	8K Bytes	DIP-40 Pin	-40°C~85°C
W78E052DPG				PLCC-44 Pin	-40°C~85°C
W78E052DFG				PQFP-44 Pin	-40°C~85°C
W78E052DLG				LQFP-48 Pin	-40°C~85°C
W78E051DDG		2K Bytes	4K Bytes	DIP-40 Pin	-40°C~85°C
W78E051DPG				PLCC-44 Pin	-40°C~85°C
W78E051DFG				PQFP-44 Pin	-40°C~85°C
W78E051DLG				LQFP-48 Pin	-40°C~85°C

Table 3–1: Lad Free (RoHS) Parts information list

4 PIN CONFIGURATIONS




PQFP 44-pin
1 P1.5
2 P1.6
3 P1.7
4 RST
5 RXD, P3.0
6 INT2, P4.3
7 TXD, P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 P3.6, WR
13 P3.7, RD
14 XTAL2
15 XTAL1
16 VSS
17 P4.0
18 P2.0, A8
19 P2.1, A9
20 P2.2, A10
21 P2.3, A11
22 P2.4, A12
23 P2.5, A13
24 P2.6, A14
25 P2.7, A15
26 PSEN
27 ALE
28 P4.1
29 EA
30 P0.7, AD7
31 P0.6, AD6
32 P0.5, AD5
33 P0.4, AD4
34 AD3, P0.3
35 AD2, P0.2
36 AD1, P0.1
37 AD0, P0.0
38 VDD
39 INT3, P4.2
40 T2, P1.0
41 T2EX, P1.1
42 P1.2
43 P1.3
44 P1.4


LQFP 48-pin
1 P1.5
2 P1.6
3 P1.7
4 RST
5 P3.0
6 INT2, P4.3
7 P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 NC
13 P3.6, WR
14 P3.7, RD
15 XTAL2
16 XTAL1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC
25 P2.5, A13
26 P2.6, A14
27 P2.7, A15
28 PSEN
29 ALE
30 P4.1
31 EA
32 P0.7, AD7
33 P0.6, AD6
34 P0.5, AD5
35 P0.4, AD4
36 NC
37 AD2, P0.3
38 AD2, P0.2
39 AD1, P0.1
40 AD0, P0.0
41 VDD
42 INT3, P4.2
43 T2, P1.0
44 T2EX, P1.1
45 P1.2
46 P1.3
47 P1.4
48 NC

8 MEMORY ORGANIZATION

The W78E054D/W78E052D/W78E051D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

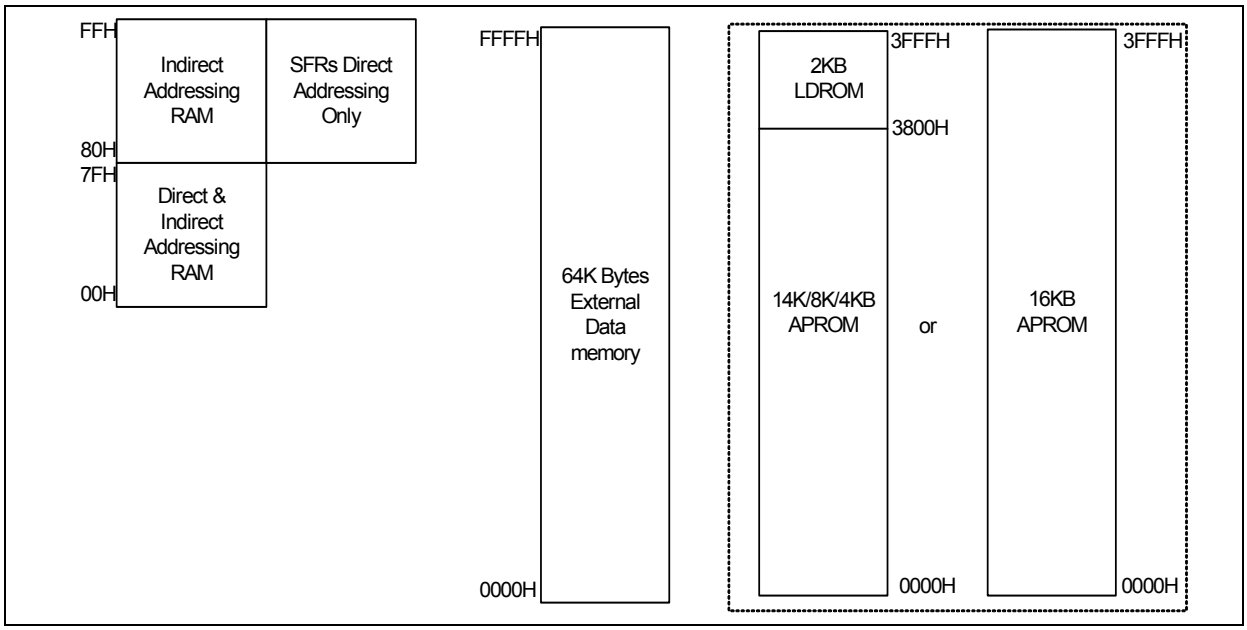


Figure 8–1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E054D/W78E052D/W78E051D series can be up to 16K/8K/4K bytes (2K bytes for ISP F/W, share with the W78E054D) long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E054D/W78E052D/W78E051D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

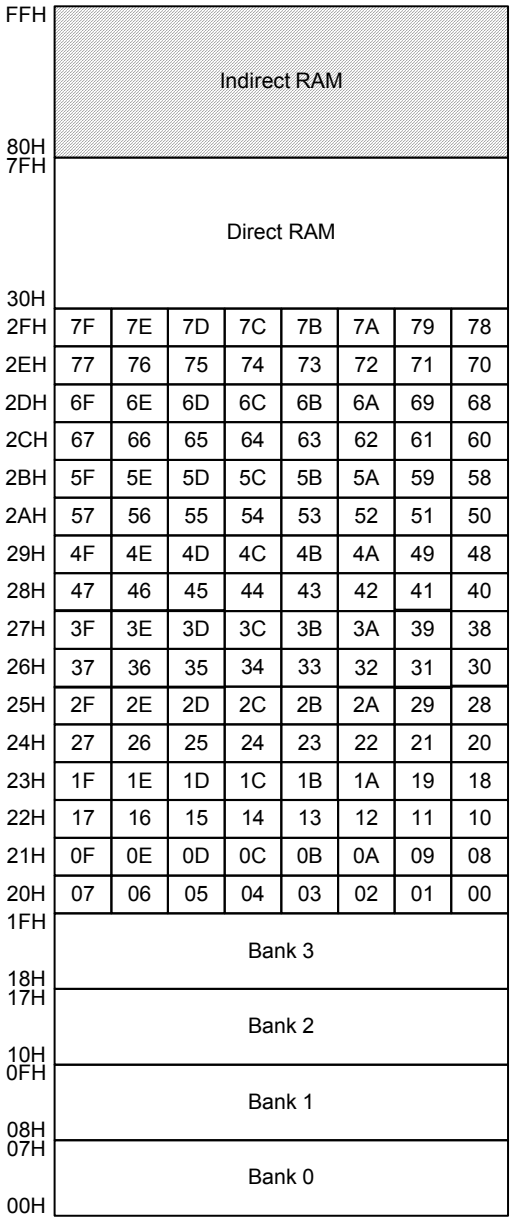


Figure 8–3 Scratch-pad RAM

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78E054D/W78E052D/W78E051D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

9 SPECIAL FUNCTION REGISTERS

The W78E054D/W78E052D/W78E051D series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W78E054D/W78E052D/W78E051D series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8	P4								DF
D0	PSW								D7
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CF
C0	XICON				SFRAL	SFRAH	SFRRD	SFRCN	C7
B8	IP						EAPAGE	CHPCON	BF
B0	P3							IPH	B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	WDTC	8F
80	P0	SP	DPL	DPH			P0UPR	PCON	87

Table 9–1: Special Function Register Location Table

Note:

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

		Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

AUXR

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALE_OFF

Mnemonic: AUXR Address: 8Eh

7	SWRST	When this bit is set to 1 and ENP is set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation.
1	ISP	The ISP function Select. When this bit is set to 1 and ENP is set to 1. It will run ISP function.
0	ENP	When this bit is set to 1 and SWRST is set to 1. It will enforce microcontroller reset to initial condition just like power on reset. When this bit is set to 1 and ISP is set to 1. It will run ISP function

Note1: CHPCON = 0x81, it is Software reset

Note2: CHPCON = 0x03, ISP function is enabled.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	External interrupt 3 priority is higher if set this bit to 1
6	EX3	Enable External interrupt 3 if set this bit to 1
5	IE3	If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
4	IT3	External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
3	PX2	External interrupt 2 priority is higher if set this to 1
2	EX2	Enable External interrupt 2 if set this bit to 1
1	IE2	If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
0	IT2	External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

SFR program of address low

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL Address: C4h

BIT	NAME	FUNCTION
7-0	SFRAL.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAL contains the low-order byte of address.

SFR program of address high

Bit:	7	6	5	4	3	2	1	0

SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH Address: C5h

BIT	NAME	FUNCTION
7-0	SFRAH.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAH contains the high-order byte of address.

SFR program For Data

Bit: 7 6 5 4 3 2 1 0

SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

Mnemonic: SFRFD Address: C6h

BIT	NAME	FUNCTION
7-0	SFRFD.[7:0]	The programming data for on-chip flash memory in programming mode.

SFR for Program Control

Bit: 7 6 5 4 3 2 1 0

-		OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: C7h

BIT	NAME	FUNCTION
5	OEN	FLASH EPROM output enable.
4	CEN	FLASH EPROM chip enable.
3-0	CTRL[3:0]	CTRL[3:0]: The flash control signals

Mode	OEN	CEN	CTRL<3:0>	SFRAH, SFRAL	SFRFD
Flash Standby	1	1	X	X	X
Read Company ID	0	0	1011	0FFh, 0FFh	Data out
Read Device ID High	0	0	1100	0FFh, 0FFh	Data out
Read Device ID Low	1	0	1100	0FFh, 0FEh	Data out
Erase APROM	1	0	0010	X	X
Erase Verify APROM	0	0	1001	Address in	Data out
Program APROM	1	0	0001	Address in	Data in
Program Verify APROM	0	0	1010	Address in	Data out
Read APROM	0	0	0000	Address in	Data out

Timer 2 Control

Bit: 7 6 5 4 3 2 1 0

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Op-code	HEX Code	Bytes	W78E054D/W78E052D/W78E051D series Clock cycles
SUBB A, R4	9C	1	12
SUBB A, R5	9D	1	12
SUBB A, R6	9E	1	12
SUBB A, R7	9F	1	12
SUBB A, @R0	96	1	12
SUBB A, @R1	97	1	12
SUBB A, direct	95	2	12
SUBB A, #data	94	2	12
INC A	04	1	12
INC R0	08	1	12
INC R1	09	1	12
INC R2	0A	1	12
INC R3	0B	1	12
INC R4	0C	1	12
INC R5	0D	1	12
INC R6	0E	1	12
INC R7	0F	1	12
INC @R0	06	1	12
INC @R1	07	1	12
INC direct	05	2	12
INC DPTR	A3	1	24
DEC A	14	1	12
DEC R0	18	1	12
DEC R1	19	1	12
DEC R2	1A	1	12
DEC R3	1B	1	12
DEC R4	1C	1	12
DEC R5	1D	1	12
DEC R6	1E	1	12
DEC R7	1F	1	12
DEC @R0	16	1	12
DEC @R1	17	1	12
DEC direct	15	2	12

Op-code	HEX Code	Bytes	W78E054D/W78E052D/W78E051D series Clock cycles
CJNE @R0, #data, rel	B6	3	24
CJNE @R1, #data, rel	B7	3	24
CJNE R0, #data, rel	B8	3	24
CJNE R1, #data, rel	B9	3	24
CJNE R2, #data, rel	BA	3	24
CJNE R3, #data, rel	BB	3	24
CJNE R4, #data, rel	BC	3	24
CJNE R5, #data, rel	BD	3	24
CJNE R6, #data, rel	BE	3	24
CJNE R7, #data, rel	BF	3	24
DJNZ R0, rel	D8	2	24
DJNZ R1, rel	D9	2	24
DJNZ R5, rel	DD	2	24
DJNZ R2, rel	DA	2	24
DJNZ R3, rel	DB	2	24
DJNZ R4, rel	DC	2	24
DJNZ R6, rel	DE	2	24
DJNZ R7, rel	DF	2	24
DJNZ direct, rel	D5	3	24

Table 10-1: Instruction Set for W78E054D/W78E052D/W78E051D

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH	IP/ XICON.7/ XICON.3	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being executed.
3. The current instruction does not involve a write to IE, IP, IPH, XICON registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on the below table. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, IP, IPH and then executes a MUL or DIV instruction.

13.4 Interrupt Inputs

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least one machine cycle to ensure proper sampling. If the external interrupt is high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the W78E054D/W78E052D/W78E051D is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

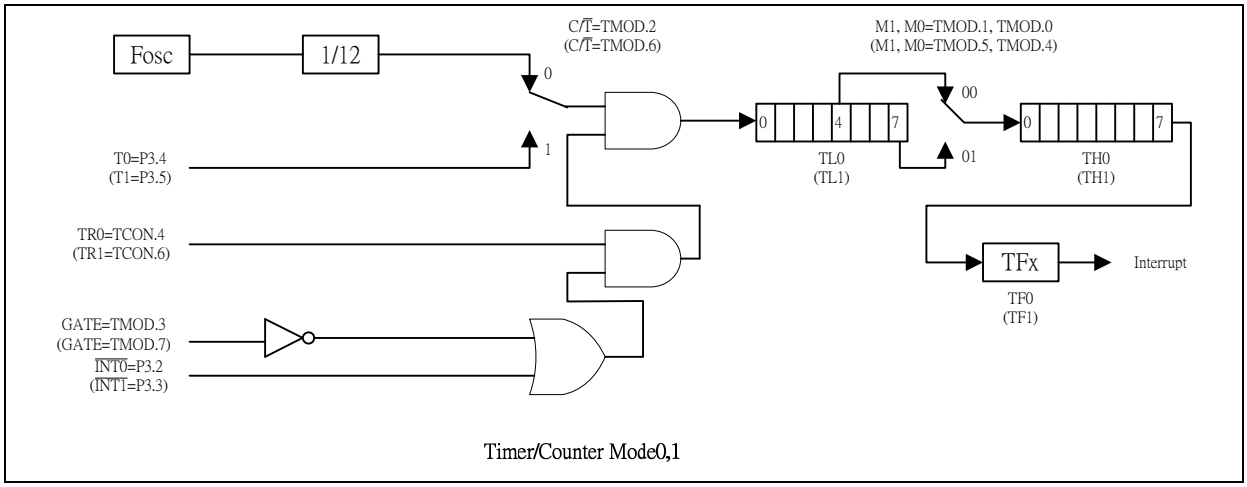


Figure 14–1 Timer/Counters 0 & 1 in Mode 0, 1

14.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of clock/12 or pulses on pin Tn.

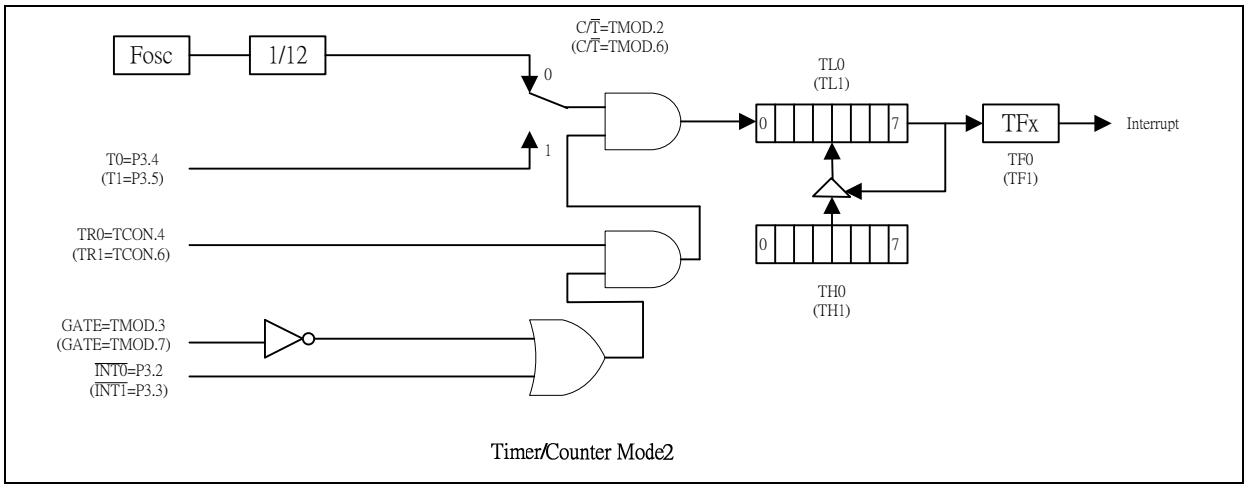


Figure 14–2 Timer/Counter 0 & 1 in Mode 2

14.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0

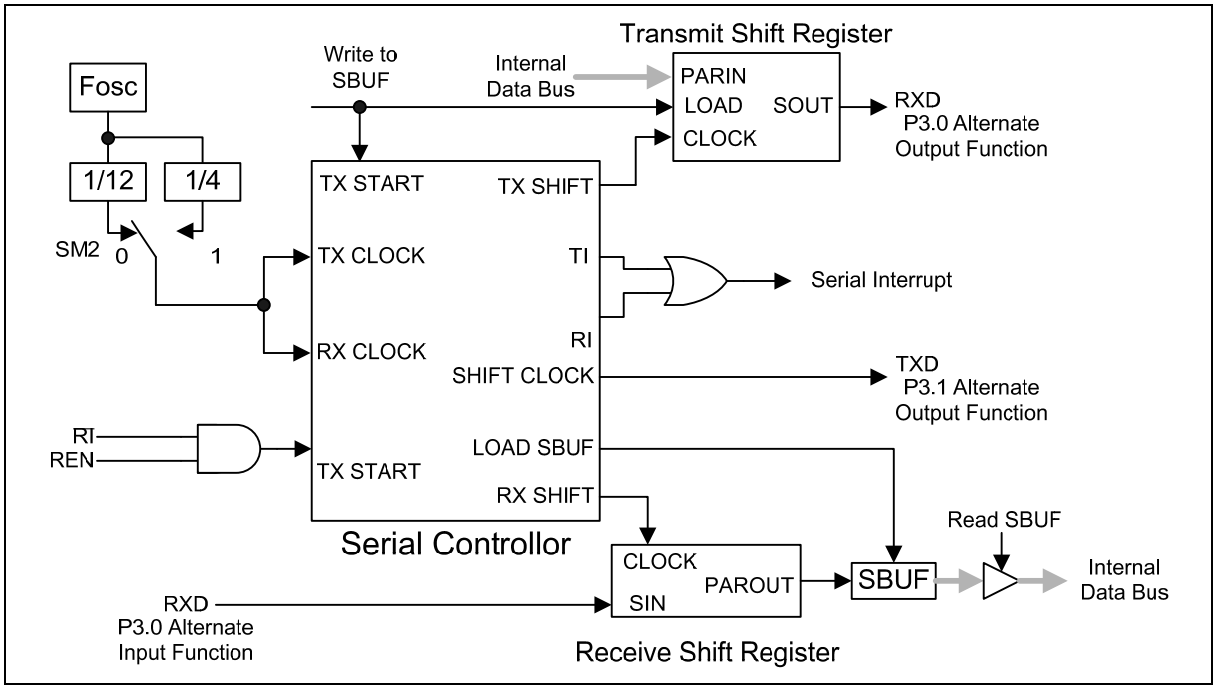


Figure 16–1 Serial port mode 0

The TI flag is set high in S6P2 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in S6P2 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.

grammable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

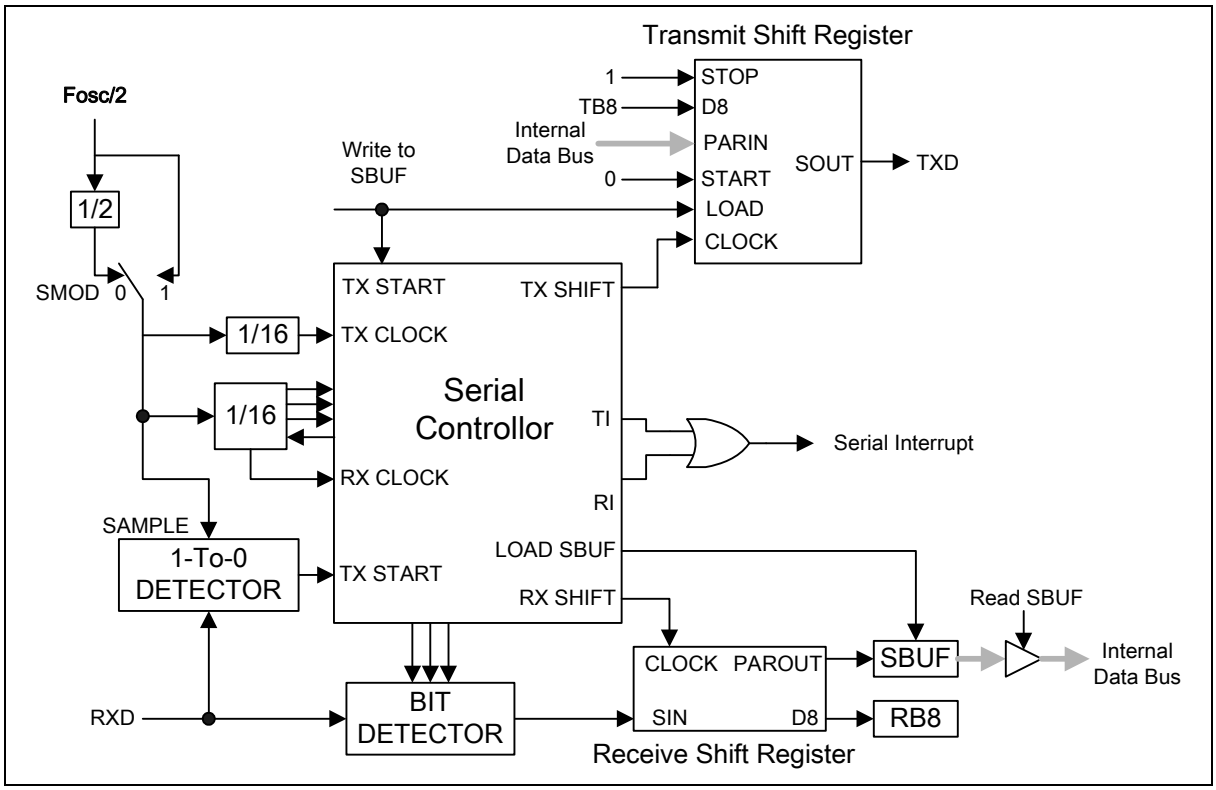


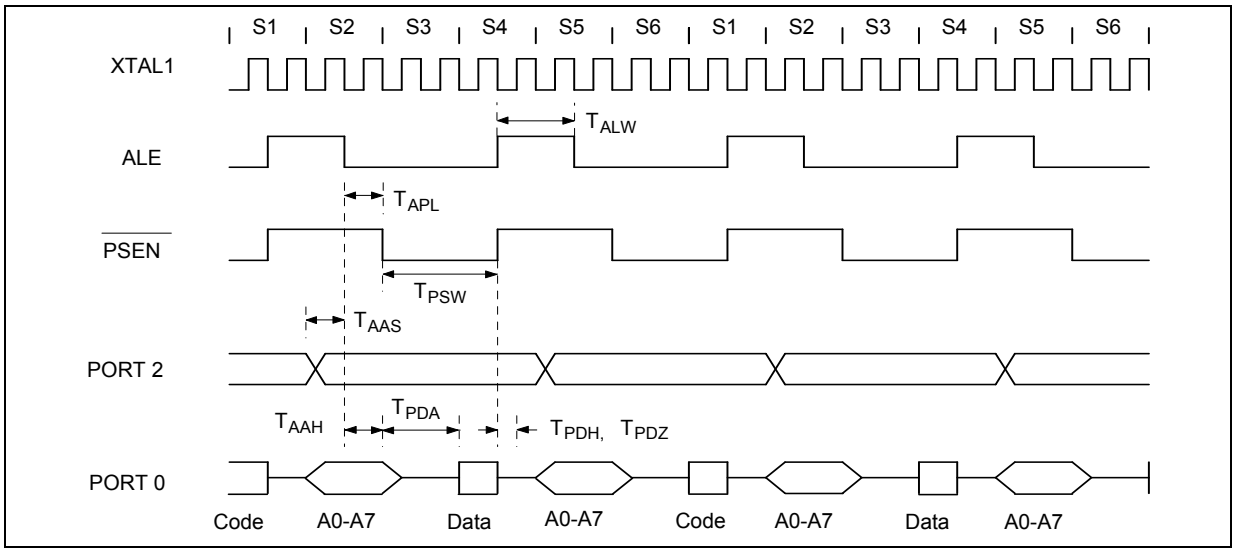
Figure 16–3 Serial port mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

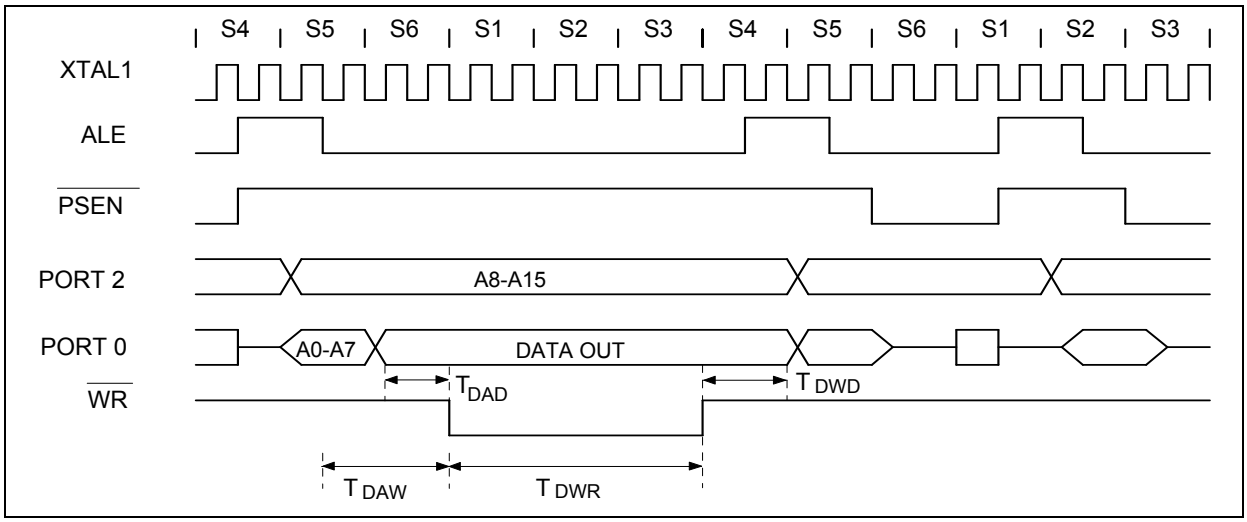
1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

20.4 TIMING waveforms

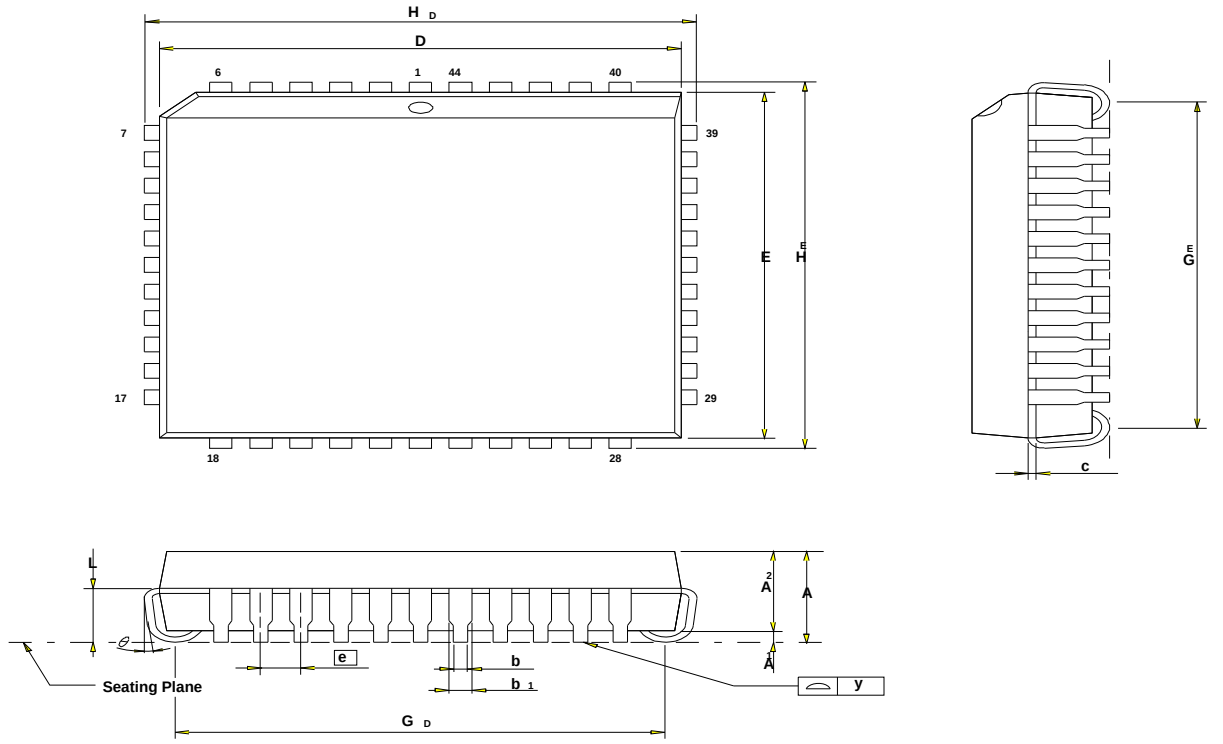
20.4.1 Program Fetch Cycle



20.4.2 Data Read Cycle

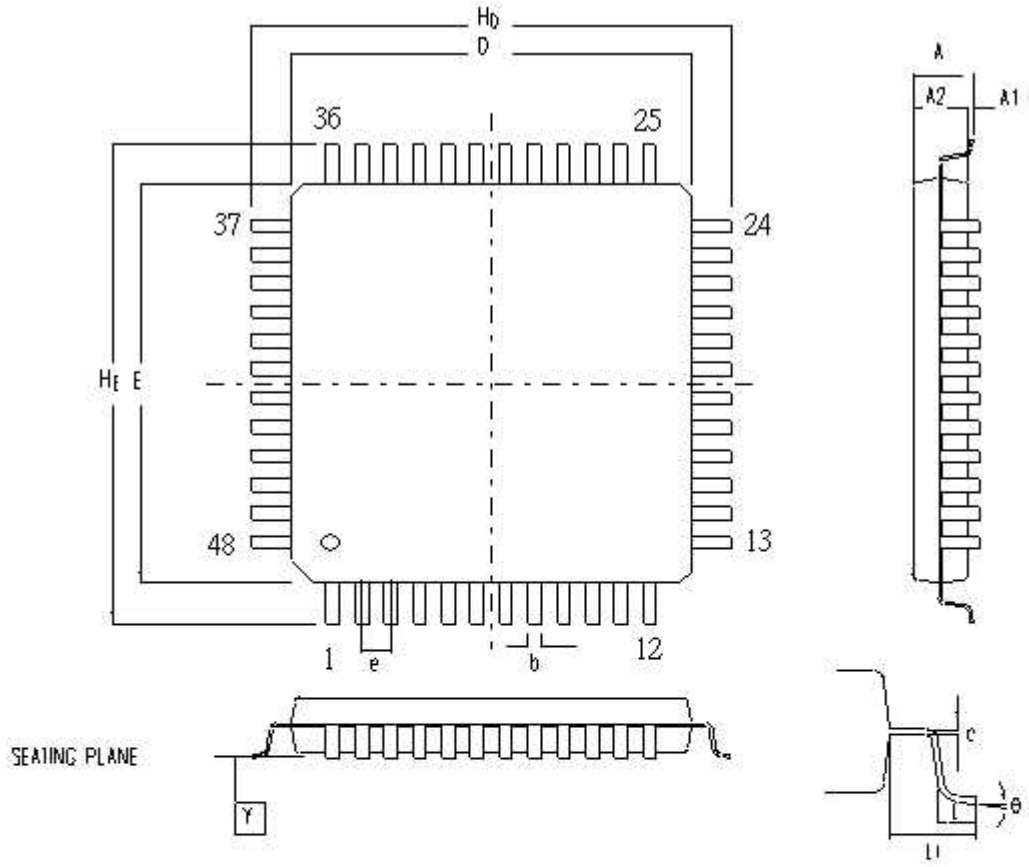


23.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.185	——	——	4.70
A 1	0.020	——	——	0.51	——	——
A 2	0.145	0.150	0.155	3.68	3.81	3.94
b 1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G D	0.590	0.610	0.630	14.99	15.49	16.00
G E	0.590	0.610	0.630	14.99	15.49	16.00
H D	0.680	0.690	0.700	17.27	17.53	17.78
H E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	——	——	0.004	——	——	0.10

23.4 48-pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°