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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Not For New Designs
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e051dfg

Email: info@E-XFL.COM

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2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
 - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
 - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4V to 5.5V
- Temperature grade is (-40°C~85°C)
- Pin and Instruction-sets compatible with MCS-51
- 256 bytes of on-chip scratchpad RAM
- 16K/8K/4K bytes electrically erasable/programmable Flash EPROM
- 2K bytes LDROM support ISP function (Reference Application Note)
- 64KB program memory address space
- 64KB data memory address space
- Four 8-bit bi-directional ports
- 8-sources, 4-level interrupt capability
- One extra 4-bit bit-addressable I/O port, additional INT2 / INT3 (available on PQFP, PLCC and LQFP package)
- Three 16-bit timer/counters
- One full duplex serial port
- Watchdog Timer
- EMI reduction mode
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages: DIP40, PLCC44, PQFP44, LQFP48

4 PIN CONFIGURATIONS





7.6 Data Pointers

The data pointer of W78E054D/W78E052D/W78E051D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78E054D/W78E052D/W78E051D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78E054D/W78E052D/W78E051D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E054D/W78E052D/W78E051D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

7.7.5 Scratch-pad RAM

The W78E054D/W78E052D/W78E051D series has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

7.7.6 Stack Pointer

The W78E054D/W78E052D/W78E051D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E054D/W78E052D/W78E051D. Hence the size of the stack is limited by the size of this RAM.

8.2.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

8.2.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

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	-	-	-	-	-		-	-	P0UP			
Mnem	Inemonic: P0UPR Address: 86h											
BIT	NAME	FUNCTION	FUNCTION									
0	P0UP	0: Port 0 pins are open-drain.										
		1: Port 0 pir	ns are interr	nally pulled-	up. Port	0 is s	structurally t	he same as	Port 2.			

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnem	onic: PCO	N Address: 87h
BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.
6	SMOD 0	 Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (stan- dard 8052 function).
		1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	-	Reserved
4	POR	0: Cleared by software.
		1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnem	onic: TCO	N Address: 88h
BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared auto- matically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared auto- matically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

BIT	NAME	FUNCTION
7	CY	Carry flag:
		Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry:
		Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0:
		The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag:
		Set when a carry was generated from the seventh bit but not from the 8 th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1:
		The General purpose flag that can be set or cleared by the user by software.
0	Р	Parity flag:
		Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4

Address: D8h

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$, $\overline{INT3}$).

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0				
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0				
Mnem	Vnemonic: ACC Address: E0h											
Bit	Name	Function										
7-0	ACC	The A or A	The A or ACC register is the standard 8052 accumulator.									

B Register

Bit:	7	6	5	4	3	2	1	0			
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0			
Mnem	Vnemonic: B Address: F0h										
Bit	Name	Function									

11 POWER MANAGEMENT

The W78E054D/W78E052D/W78E051D has several features that help the user to control the power consumption of the device. The power saved features have basically the POWER DOWN mode and the IDLE mode of operation.

11.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 24 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately.

11.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W78E054D/W78E052D/W78E051D will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detects. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W78E054D/W78E052D/W78E051D can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the high level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there.

service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, IP, IPH and then executes a MUL or DIV instruction.

13.4 Interrupt Inputs

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least one machine cycle to ensure proper sampling. If the external interrupt is high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the W78E054D/W78E052D/W78E051D is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.



Figure 14-4 16-Bit Capture Mode

14.3.2 Auto-Reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the CP / RL2 bit in the T2CON register and clearing the DCEN bit in T2MOD(bit0) register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from 0FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.



Figure 14–5 16-Bit Auto-reload Mode, Counting Up

14.3.3 Auto-reload Mode, Counting Up/Down

Timer/Counter 2 will be in auto-reload mode as an up/down counter if CP / $\overline{RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture registers. The next down count following the case where the contents of Timer/Counter equal the capture registers will load a 0FFFFh into Timer/Counter 2. In either event a reload will set the TF2 bit. A reload will also toggle the EXF2 bit. However, the EXF2 bit cannot generate an interrupt while in this mode.



Figure 14–6 16-Bit Auto-reload Mode, Counting Up

14.3.4 Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from 0FFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.



Figure 14–7 Baud Rate Generator Mode

16 SERIAL PORT

Serial port in this device is a full duplex port. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half-duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half-duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W78E054D/W78E052D/W78E051D.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.



Figure 16–1 Serial port mode 0

The TI flag is set high in S6P2 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in S6P2 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.

Bit 0: Lock bits

0: Lock enable

1: Lock disable

This bit is used to protect the customer's program code in the W78E054D/W78E052D/W78E051D. It may be set after the programmer finishes the programming and verifies sequence. Once these bits are set to logic 0, both the FLASH data and Special Setting Registers cannot be accessed again.

Bit 1: MOVC inhibit

0: MOVC inhibit enable

1: MOVC inhibit disable

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Bit 2: CBS

Config boot select at Power-on reset and external reset. CBS=1: Boot from APROM block (default). CBS=0: Boot from LDROM block (0x3800).

Bit 3: NSR (Noise Sensitivity Reduction)

NSR=1: Noise Sensitivity Reduction is disabled. NSR=0: Noise Sensitivity Reduction is enabled.

Bit 4: Must be "1"

Bit 5: Machine Cycle Select

This bit is select MCU core, default value is logic 1, and the MCU core is 12T per instruction. Once this bit is set to logic 0, the MCU core is 6T per instruction.

Bit 6: Must be "1"

Bit 7: Crystal Select

0 (24MHz): If system clock is slower than 24MHz, programming "0". It can reduce EMI effect and save the power consumption.

1 (40MHz): If system clock is faster than 24MHz, programming "1".

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a limited number of samples.

*2: Pins of ports 1~4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

- *3: Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: Maximum I_{OL} per port pin: 20mA Maximum I_{OL} per 8-bit port: 40mA Maximum total I_{OL} for all outputs: 100mA
- *4: If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification. If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

Voltage	Max. Frequency	6T/12T mode	Note
4.5-5.5V	40MHz	12T	
4.5-5.5V	20MHz	6T	
2.4V	20MHz	12T	
2.4V	10MHz	6T	

*5: Tested while CPU is kept in reset state and EA=H, Port0=H.

Frequency VS Voltage Table

20.3 AC ELECTRICAL CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation.

20.3.1 Clock Input Waveform

XTAL1		
	FOP, TCP	

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:

- 1. The clock may be stopped indefinitely in either state.
- 2. The TCP specification is used as a reference in other specifications.

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20.4.3 Data Write Cycle



20.4.4 Port Access Cycle



21 APPLICATION CIRCUITS

21.1 External Program Memory and Crystal



Figure A



21.2 Expanded External Data Memory and Oscillator

Figure B

23.3 44-pin PQFP

