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Details

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Product Status	Not For New Designs
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e051dlg

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W78E054D/W78E052D/W78E051D Data Sheet

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8 MEMORY ORGANIZATION

The W78E054D/W78E052D/W78E051D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction opcodes, while the Data Memory is used to store data or for memory mapped devices.



Figure 8–1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E054D/W78E052D/W78E051D series can be up to 16K/8K/4K bytes (2K bytes for ISP F/W, share with the W78E054D) long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E054D/W78E052D/W78E051D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.



256 bytes RAM and SFR Data Memory Space

Figure 8-2 W78E054D/W78E052D/W78E051D RAM and SFR Memory Map

Since the scratch-pad RAM is only 256bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB		BIT A	DDRESS, S	SYMBOL			LSB	RESET
В	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
P4	Port 4	D8H					INT2	INT3			0000 1111B
PSW	Program status word	D0H	(D7)	(D6)	(D5)	(D4)	(D3)	(D2)	(D1)	(D0)	0000 0000B
			CY	AC	F0	RS1	RS0	OV	F1	Р	
TH2	T2 reg. high	CDH									0000 0000B
TL2	T2 reg. low	ССН									0000 0000B
RCAP2H	T2 capture low	CBH									0000 0000B
RCAP2L	T2 capture high	CAH									0000 0000B
T2MOD	Timer 2 Mode	C9								DCEN	0000 0000B
T2CON	Timer 2 control	С8Н	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
SFRCN	SFR program of control	C7H			NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	0000 0000B
SFRRD	SFR program of data register	C6H									0000 0000B
SFRAH	SFR program of address high byte	C5H									0000 0000B
SFRAL	SFR program of address low byte	C4H									0000 0000B
XICON	External interrupt control	C0H	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2	0000 0000B
CHPCON	Chip control	BFH	SWRST	-		-	-	-	FBOOTS L	ENP	0000 0000B
EAPAGE	Erase page operation modes	BEH							EAPG1	EAPG0	0000 0000B
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	1100 0000B
IPH	Interrupt priority High	B7H									0000 0000B
P3	Port 3	вон	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0100 0000B
P2	Port 2	A0H	(A7)	(A6)	(A5)	(A4)	(A3)	(A2)	(A1)	(A0)	1111 1111B
SBUE	Serial huffer	ഫപ	713		A13	712	711	710	7.5	7.0	0000 00008
SCON	Serial control	08H	(0E)	(0E)	(0D)	(00)	(0R)	(04)	(00)	(08)	
3001	Senal control	901	(9F) SM0/FE	(9⊑) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 00008
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91) T2EX	(90) T2	1111 1111B
WDTC	Watchdog control	8FH	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0	0000 0000B
AUXR	Auxiliary	8EH	-	-	-	-				ALEOFF	0000 0110B
TH1	Timer high 1	8DH									0000 0000B
TH0	Timer high 0	8CH									0000 0000B
TL1	Timer low 1	8BH									0000 0000B
TL0	Timer low 0	8AH									0000 0000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	MO	0000 0000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power control	87H	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL	0011 0000B
P0UPR	Port 0 pull up option Register	86H	-	-	-	-	-	-	-	P0UP	0000 0001B
DPH	Data pointer high	83H									0000 0000B

W78E054D/W78E052D/W78E051D Data Sheet

Address: 80h

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DPL	Data pointer low	82H									0000 0000B
SP	Stack pointer	81H									0000 0111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	1111 1111B

9.1 SFR Detail Bit Descriptions

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0

BIT	NAME	FUNCTION
7-0	P0.[7:0]	Port 0 is an open-drain bi-directional I/O port if SFR P0UPR.0 (bit P0UP) clear to "0", and when SFR P0UPR.0 (bit P0UP) set to "1", Port 0 pins are internally pulled-up. This port also provides a multiplexed low order address/data bus during accesses to external memory.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
Mnem	onic: SP						Ac	dress: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
Mnem	onic: DPL						Ac	dress: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
Mnem	onic: DPH						Ac	ddress: 83h
BIT	BIT NAME FUNCTION							
7-0 DPH.[7:0] This is the high byte of the standard 8052 16-bit data pointer.								

Port 0 Pull Up Option Register

Bit: 7 6 5 4 3 2 1 0	6 5 4 3 2 1	0
----------------------	-------------	---

4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{\text{INT0}}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

7	6	5	4	3	2	1	0
GATE	C/\overline{T}	M1	M0	GATE	C/\overline{T}	M1	M0
TIMER1				TIMER0			

-

Bit:

Mnem	Inemonic: TMOD			
BIT	NAME	FUNCTION		
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.		
6	C/T	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.		
5	M1	Timer 1 mode select bit 1. See table below.		
4	M0	Timer 1 mode select bit 0. See table below.		
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.		
2	C/T	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.		
1	M1	Timer 0 mode select bit 1. See table below.		
0	M0	Timer 0 mode select bit 0. See table below.		

M1, M0: Mode Select bits:

M1	MO	MODE
0	0	Mode 0: 13-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1)

Mnemonic: SCON

Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable:
		0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0	
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	
Mnemonic: SBUF Address: 99h									

Mnemonic: SBUF

W78E054D/W78E052D/W78E051D Data Sheet

EAPAGE ERASE PAGE Operation Modes									
Bit:	7	6	5	4	3	2	1	0	
	-	-	-	-	-	-	EAPG1	EAPG0	
Mnem	onic: EAP	AGE						Address: BD	
BIT	NAME	FUNCTI	ON						
1	EAPG1	1: To eas	se PAGE1 w	hen ease co	mmand is	set. (LDROM)		
0	EAPG0	1: To eas	o ease PAGE0 when ease command is set. (APROM)						
;CPU	CPU Clock = 12MHz/12T mode								
READ_	TIME	ΕÇ	QU 1						
PROGF	RAM_TIME	EÇ	QU 50						
ERASE	E_TIME	ΕÇ	QU 500	00					
Erase	e_APROM:								
n	nov	EAPAGE, #01	lh	;set EAD	PAGE is A	APROM			
n	nov	SFRCN, #ERA	ASE_ROM						
n	nov	TLO,#LOW	(65536-ER <i>I</i>	ASE_TIME)					
n	nov	TH0, #HIGH	(65536-ER <i>P</i>	ASE_TIME)					
S	setb	TR0							
n	nov	CHPCON, #00	0000011b						
n	nov	EAPAGE, #00)h	;clear H	EAPAGE				
c	clr	TF0							
C	clr	TR0							
r	ret								
Erase	e LDROM:								
n	nov	EAPAGE, #02	2h	;set EAD	PAGE is I	DROM			
n	nov	SFRCN, #ERA	ASE ROM			-			
n	nov	TLO, #LOW	65536-ERA	ASE TIME)					
n	nov	TH0, #HIGH((65536-ERA	ASE TIME)					
-	setb	TR0	(00000 211						
n	nov	CHPCON.#0(000011b						
n	nov	EAPAGE, #00)h	iclear H	CAPAGE				
c.	-lr	TF0		/01001					
	rlr	TR0							
ר ז	ret	1110							
-									
Chip (Control								
Bit:	7	6	5	4	3	2	1	0	
	SWRST		-	-	-	-	ISP	ENP	
Mnem	onic: CHF	CON						Address: BFh	
Bit	Name	Fu	nction						
<u> </u>									

W78E054D/W78E052D/W78E051D Data Sheet

Op-code	HEX Code	Bytes	W78E054D/W78E052D/W78E051D series Clock cycles
MUL AB	A4	1	48
DIV AB	84	1	48
DA A	D4	1	12
ANL A, R0	58	1	12
ANL A, R1	59	1	12
ANL A, R2	5A	1	12
ANL A, R3	5B	1	12
ANL A, R4	5C	1	12
ANL A, R5	5D	1	12
ANL A, R6	5E	1	12
ANL A, R7	5F	1	12
ANL A, @R0	56	1	12
ANL A, @R1	57	1	12
ANL A, direct	55	2	12
ANL A, #data	54	2	12
ANL direct, A	52	2	12
ANL direct, #data	53	3	24
ORL A, R0	48	1	12
ORL A, R1	49	1	12
ORL A, R2	4A	1	12
ORL A, R3	4B	1	12
ORL A, R4	4C	1	12
ORL A, R5	4D	1	12
ORL A, R6	4E	1	12
ORL A, R7	4F	1	12
ORL A, @R0	46	1	12
ORL A, @R1	47	1	12
ORL A, direct	45	2	12
ORL A, #data	44	2	12
ORL direct, A	42	2	12
ORL direct, #data	43	3	24
XRL A, R0	68	1	12

Op-code	HEX Code	Bytes	W78E054D/W78E052D/W78E051D series Clock cycles
MOV direct, R2	8A	2	24
MOV direct, R3	8B	2	24
MOV direct, R4	8C	2	24
MOV direct, R5	8D	2	24
MOV direct, R6	8E	2	24
MOV direct, R7	8F	2	24
MOV direct, @R0	86	2	24
MOV direct, @R1	87	2	24
MOV direct, direct	85	3	24
MOV direct, #data	75	3	24
MOV DPTR, #data 16	90	3	24
MOVC A, @A+DPTR	93	1	24
MOVC A, @A+PC	83	1	24
MOVX A, @R0	E2	1	24
MOVX A, @R1	E3	1	24
MOVX A, @DPTR	E0	1	24
MOVX @R0, A	F2	1	24
MOVX @R1, A	F3	1	24
MOVX @DPTR, A	F0	1	24
PUSH direct	C0	2	24
POP direct	D0	2	24
XCH A, R0	C8	1	12
XCH A, R1	C9	1	12
XCH A, R2	CA	1	12
XCH A, R3	СВ	1	12
XCH A, R4	CC	1	12
XCH A, R5	CD	1	12
XCH A, R6	CE	1	12
XCH A, R7	CF	1	12
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12

Op-code	HEX Code	Bytes	W78E054D/W78E052D/W78E051D series Clock cycles
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24
JB bit, rel	20	3	24
JNB bit, rel	30	3	24
JBC bit, rel	10	3	24
CJNE A, direct, rel	B5	3	24
CJNE A, #data, rel	B4	3	24

14 PROGRAMMABLE TIMERS/COUNTERS

The W78E054D/W78E052D/W78E051D series have Three 16-bit programmable timer/counters. A machine cycle equals 12 or 6 oscillator periods, and it depends on 12T mode or 6T mode that the user configured this device.

14.1 Timer/Counters 0 & 1

W78E054D/W78E052D/W78E051D has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the " $^{C/T}$ " bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

14.2 Time-Base Selection

W78E054D/W78E052D/W78E051D provides users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on W78E054D/W78E052D/W78E051D and the standard 8051 can be matched. This is the default mode of operation of the W78E054D/W78E052D/W78E051D timers.

14.2.1 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or \overline{INTx} is 1. When C/\overline{T} is 0, the timer/counter counts clock cycles; when C/\overline{T} is 1, it counts falling edges on T0 (Timer 0) or T1 (Timer 1). For clock cycles, the time base be 1/12 speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled.

14.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of 0FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if

16 SERIAL PORT

Serial port in this device is a full duplex port. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half-duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half-duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W78E054D/W78E052D/W78E051D.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.



Figure 16–1 Serial port mode 0

The TI flag is set high in S6P2 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in S6P2 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.



19 CONFIG BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E054D/W78E052D/W78E051D has a Special Setting Register, the config Bits, which cannot be accessed in normal mode. The Security register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers cannot be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



20 ELECTRICAL CHARACTERISTICS

20.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	2.4	5.5	V
Input Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V
Operating Temperature (W78E054D/W78E052D/W78 E051D)	T _A	-40	+85	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

20.2 DC ELECTRICAL CHARACTERISTICS

 $T_A = -40^{\circ}C \sim +85^{\circ}C$, $V_{DD} = 2.4V \sim 5.5V$, $V_{SS} = 0V$

Sym	Parameter	Test Condition	Min	Typ ^{*1}	Мах	Unit
VIL	Input Low Voltage (Ports 0~4, /EA, XTAL1, RST)	2.4 < V _{DD} < 5.5V	-0.5		0.2V _{DD} -0.1	V
V _{IH}	Input High Voltage (Ports 0~4, /EA)	2.4 < V _{DD} < 5.5V	0.2V _{DD} +0.9		V _{DD} + 0.5	V
V _{IH1}	Input High Voltage (XTAL1, RST)	2.4 < V _{DD} < 5.5V	$0.7V_{DD}$		V _{DD} + 0.5	V
V _{oL}	Output Low Voltage (Ports 0~4, ALE, /PSEN)	V_{DD} =4.5V, I_{OL} = 12.0mA ^{*3,*4} V_{DD} =2.4V, I_{OL} = 10mA ^{*3,*4}			0.4	V
V _{OH1}	Output High Voltage (Ports 1~4)	V _{DD} =4.5V, I _{OH} = -300μA ^{*4} V _{DD} =2.4V, I _{OH} = -35μA ^{*4}	2.4 2.0			V
V _{OH2}	Output High Voltage (Ports 0 & 2 in external bus mode, ALE, /PSEN)	V _{DD} =4.5V, I _{OH} = -8.0mA ^{*4} V _{DD} =2.4V, I _{OH} = -2.2mA ^{*4}	2.4 2.0			V
I _{IL}	Logical 0 Input Current (Ports 1~4)	V_{DD} =5.5V, V_{IN} =0.4V		-45	-50	μA
ITL	Logical 1-to-0 Transition Current (Ports 1~4) ^{*2}	V _{DD} =5.5V, V _{IN} =2.0V		-510	-650	μA
ILI	Input Leakage Current (Port 0)	0 < V _{IN} < V _{DD} +0.5		±0.1	±10	μA
		Active mode ^{*5} @12MHz, V _{DD} =5.0V @40MHz, V _{DD} =5.0V @12MHz, V _{DD} =3.3V @20MHz, V _{DD} =3.3V		9.5 16.0 3.1 3.7		mA
I _{DD}	Power Supply Current	Idle mode @12MHz, V _{DD} =5.0V @40MHz, V _{DD} =5.0V @12MHz, V _{DD} =3.3V @20MHz, V _{DD} =3.3V		3.5 9.2 1.2 1.7		mA
		Power-down mode		<1	50	μA
R _{RST}	RST-pin Internal Pull- down Resistor	2.4 < V _{DD} < 5.5V	100		225	KΩ

Note:

*1: Typical values are not guaranteed. The values listed are tested at room temperature and based on

23 PACKAGE DIMENSIONS

23.1 40-pin DIP

