Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e051dpg

1 GENERAL DESCRIPTION

The W78E054D/W78E052D/W78E051D series is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78E054D/ W78E052D/ W78E051D series is fully compatible with the standard 8052.

The W78E054D/W78E052D/W78E051D series contains 16K/8K/4K bytes Flash EPROM programmable by hardware writer; a 256 bytes RAM; four 8-bit bi-directional (P0, P1, P2, P3) and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by 8 sources 4-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E054D/W78E052D/W78E051D series allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E054D/W78E052D/W78E051D series microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor. The W78E054D/W78E052D/W78E051D series contains In-System Programmable (ISP) 2KB LDROM for loader program, operating voltage from 3.3V to 5.5V.

Note: If the applied V_{DD} is not stable, especially with long transition time of power on/off, it's recommended to apply an external RESET IC to the RST pin for improving the stability of system.

7.6 Data Pointers

The data pointer of W78E054D/W78E052D/W78E051D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78E054D/W78E052D/W78E051D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78E054D/W78E052D/W78E051D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E054D/W78E052D/W78E051D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

7.7.5 Scratch-pad RAM

The W78E054D/W78E052D/W78E051D series has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

7.7.6 Stack Pointer

The W78E054D/W78E052D/W78E051D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E054D/W78E052D/W78E051D. Hence the size of the stack is limited by the size of this RAM.

8 MEMORY ORGANIZATION

The W78E054D/W78E052D/W78E051D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

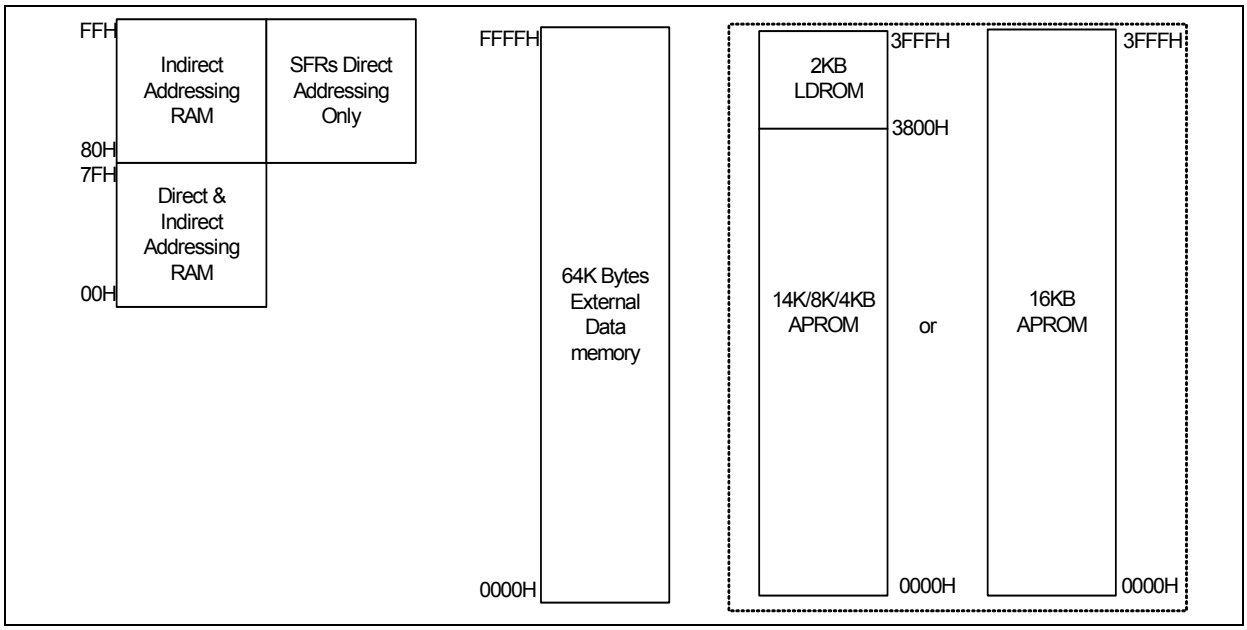


Figure 8–1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E054D/W78E052D/W78E051D series can be up to 16K/8K/4K bytes (2K bytes for ISP F/W, share with the W78E054D) long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E054D/W78E052D/W78E051D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

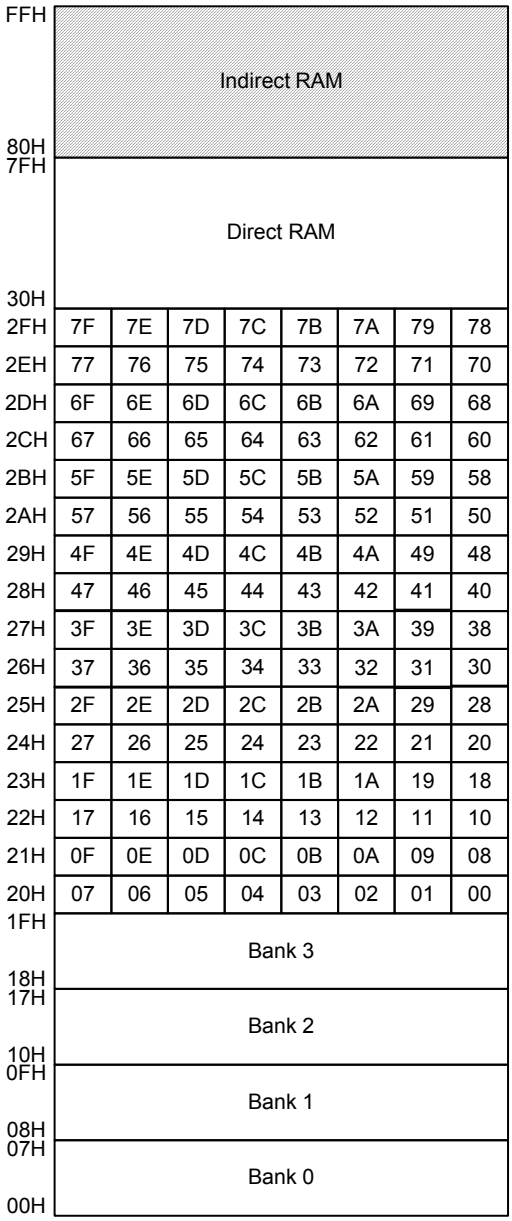


Figure 8–3 Scratch-pad RAM

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78E054D/W78E052D/W78E051D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

DPL	Data pointer low	82H									0000 0000B
SP	Stack pointer	81H									0000 0111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	1111 1111B

9.1 SFR Detail Bit Descriptions

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

BIT	NAME	FUNCTION
7-0	P0.[7:0]	Port 0 is an open-drain bi-directional I/O port if SFR P0UPR.0 (bit P0UP) clear to “0”, and when SFR P0UPR.0 (bit P0UP) set to “1”, Port 0 pins are internally pulled-up. This port also provides a multiplexed low order address/data bus during accesses to external memory.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

Port 0 Pull Up Option Register

Bit:	7	6	5	4	3	2	1	0

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7-0	P2.[7:0]	Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	-	Reserved
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$

7	SWRST	When this bit is set to 1 and ENP is set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation.
1	ISP	The ISP function Select. When this bit is set to 1 and ENP is set to 1. It will run ISP function.
0	ENP	When this bit is set to 1 and SWRST is set to 1. It will enforce microcontroller reset to initial condition just like power on reset. When this bit is set to 1 and ISP is set to 1. It will run ISP function

Note1: CHPCON = 0x81, it is Software reset

Note2: CHPCON = 0x03, ISP function is enabled.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	External interrupt 3 priority is higher if set this bit to 1
6	EX3	Enable External interrupt 3 if set this bit to 1
5	IE3	If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
4	IT3	External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
3	PX2	External interrupt 2 priority is higher if set this to 1
2	EX2	Enable External interrupt 2 if set this bit to 1
1	IE2	If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
0	IT2	External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

SFR program of address low

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL Address: C4h

BIT	NAME	FUNCTION
7-0	SFRAL.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAL contains the low-order byte of address.

SFR program of address high

Bit:	7	6	5	4	3	2	1	0

Op-code	HEX Code	Bytes	W78E054D/W78E052D/W78E051D series Clock cycles
SUBB A, R4	9C	1	12
SUBB A, R5	9D	1	12
SUBB A, R6	9E	1	12
SUBB A, R7	9F	1	12
SUBB A, @R0	96	1	12
SUBB A, @R1	97	1	12
SUBB A, direct	95	2	12
SUBB A, #data	94	2	12
INC A	04	1	12
INC R0	08	1	12
INC R1	09	1	12
INC R2	0A	1	12
INC R3	0B	1	12
INC R4	0C	1	12
INC R5	0D	1	12
INC R6	0E	1	12
INC R7	0F	1	12
INC @R0	06	1	12
INC @R1	07	1	12
INC direct	05	2	12
INC DPTR	A3	1	24
DEC A	14	1	12
DEC R0	18	1	12
DEC R1	19	1	12
DEC R2	1A	1	12
DEC R3	1B	1	12
DEC R4	1C	1	12
DEC R5	1D	1	12
DEC R6	1E	1	12
DEC R7	1F	1	12
DEC @R0	16	1	12
DEC @R1	17	1	12
DEC direct	15	2	12

11 POWER MANAGEMENT

The W78E054D/W78E052D/W78E051D has several features that help the user to control the power consumption of the device. The power saved features have basically the POWER DOWN mode and the IDLE mode of operation.

11.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 24 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately.

11.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W78E054D/W78E052D/W78E051D will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detects. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W78E054D/W78E052D/W78E051D can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the high level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there.

Each interrupt source can be individually programmed to one of 2 priority levels by setting or clearing bits in the IP registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and External interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Interrupt Priority	Flag cleared by	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	IPH.0, IP.0	Hardware, software	1(highest)	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	IPH.1, IP.1	Hardware, software	2	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IPH.2, IP.2	Hardware, software	3	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	IPH.3, IP.3	Hardware, software	4	No
Serial Port	RI + TI	0023H	ES (IE.4)	IPH.4, IP.4	Software	5	No
Timer 2 Over-flow/Match	TF2	002BH	ET2 (IE.5)	IPH.5, IP.5	Software	6	No
External Interrupt 2	IE2	0033H	EX2 (XICON.2)	IPH.6, PX2	Hardware, software	7	Yes
External Interrupt 3	IE3	003BH	EX3 (XICON.6)	IPH.7, PX3	Hardware, software	8(lowest)	Yes

Table 13–2 Summary of interrupt sources

13.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ and $\overline{INT1}$, they are sampled at S5P2 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the

14 PROGRAMMABLE TIMERS/COUNTERS

The W78E054D/W78E052D/W78E051D series have Three 16-bit programmable timer/counters. A machine cycle equals 12 or 6 oscillator periods, and it depends on 12T mode or 6T mode that the user configured this device.

14.1 Timer/Counters 0 & 1

W78E054D/W78E052D/W78E051D has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

14.2 Time-Base Selection

W78E054D/W78E052D/W78E051D provides users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on W78E054D/W78E052D/W78E051D and the standard 8051 can be matched. This is the default mode of operation of the W78E054D/W78E052D/W78E051D timers.

14.2.1 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (Timer 0) or T1 (Timer 1). For clock cycles, the time base be 1/12 speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled.

14.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of 0FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

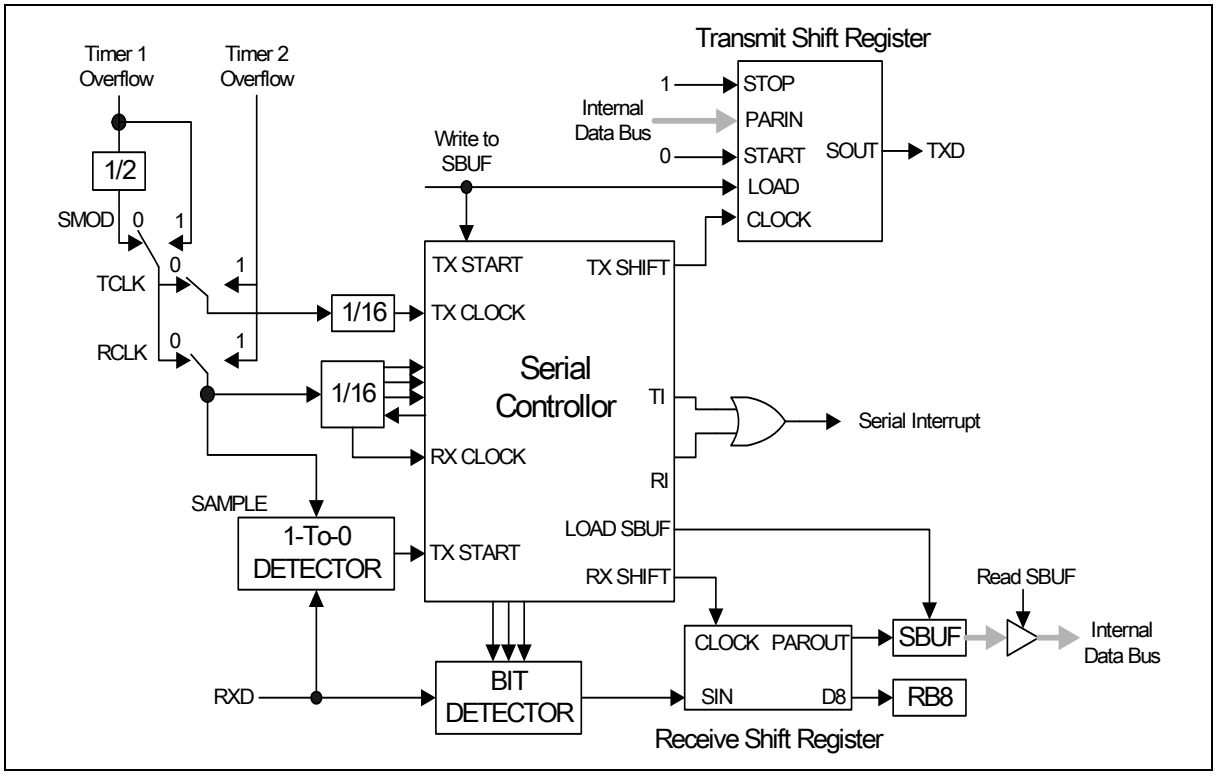


Figure 16–2 Serial port mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (1). The 9th bit received is put into RB8. The baud rate is pro-

17 FLASH ROM CODE BOOT MODE SLECTION

The W78E054D/W78E052D/W78E051D boots from APROM program (16K/8K/4K bytes) or LDROM program (2K bytes) at power on reset or external reset.

BOOT MODE Select by CONFIG bits

CBS (CONFIG.2)	Config boot select at Power-on reset and external reset. 1: Boot from APROM (0x0000). 0: Boot from LDROM (0x3800).

Bit 0: Lock bits
0: Lock enable
1: Lock disable
This bit is used to protect the customer's program code in the W78E054D/W78E052D/W78E051D. It may be set after the programmer finishes the programming and verifies sequence. Once these bits are set to logic 0, both the FLASH data and Special Setting Registers cannot be accessed again.

Bit 1: MOVC inhibit
0: MOVC inhibit enable
1: MOVC inhibit disable
This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Bit 2: CBS
Config boot select at Power-on reset and external reset.
CBS=1: Boot from APROM block (default).
CBS=0: Boot from LDROM block (0x3800).

Bit 3: NSR (Noise Sensitivity Reduction)
NSR=1: Noise Sensitivity Reduction is disabled.
NSR=0: Noise Sensitivity Reduction is enabled.

Bit 4: Must be “1”

Bit 5: Machine Cycle Select
This bit is select MCU core, default value is logic 1, and the MCU core is 12T per instruction. Once this bit is set to logic 0, the MCU core is 6T per instruction.

Bit 6: Must be “1”

Bit 7: Crystal Select
0 (24MHz): If system clock is slower than 24MHz, programming “0”. It can reduce EMI effect and save the power consumption.
1 (40MHz): If system clock is faster than 24MHz, programming “1”.

a limited number of samples.

*2: Pins of ports 1~4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

*3: Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20mA
Maximum I_{OL} per 8-bit port: 40mA
Maximum total I_{OL} for all outputs: 100mA

*4: If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification.
If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

*5: Tested while CPU is kept in reset state and EA=H, Port0=H.

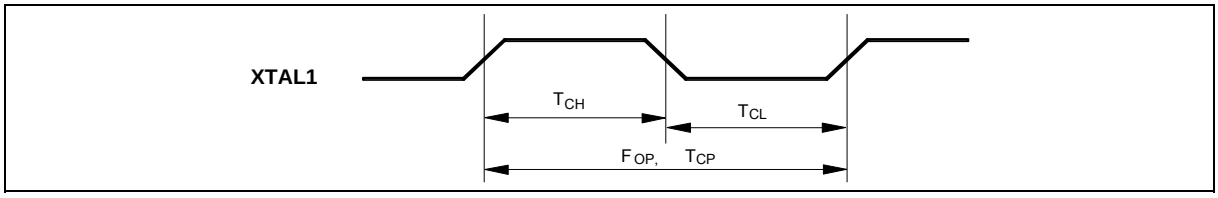
Voltage	**Max.** Frequency	6T/12T mode	Note
4.5-5.5V	40MHz	12T	
4.5-5.5V	20MHz	6T	
2.4V	20MHz	12T	
2.4V	10MHz	6T	

Frequency VS Voltage Table

20.3 AC ELECTRICAL CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation.

20.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.

ALE Low to $\overline{WR}$ Low	Tdaw	3 TCP -Δ	-	3 TCP +Δ	nS
Data Valid to $\overline{WR}$ Low	Tdad	1 TCP -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	Tdwd	1 TCP -Δ	-	-	nS
$\overline{WR}$ Pulse Width	Tdwr	6 TCP -Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

20.3.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	Tpds	1 TCP	-	-	nS
Port Input Hold from ALE Low	Tpdh	0	-	-	nS
Port Output to ALE	Tpda	1 TCP	-	-	nS

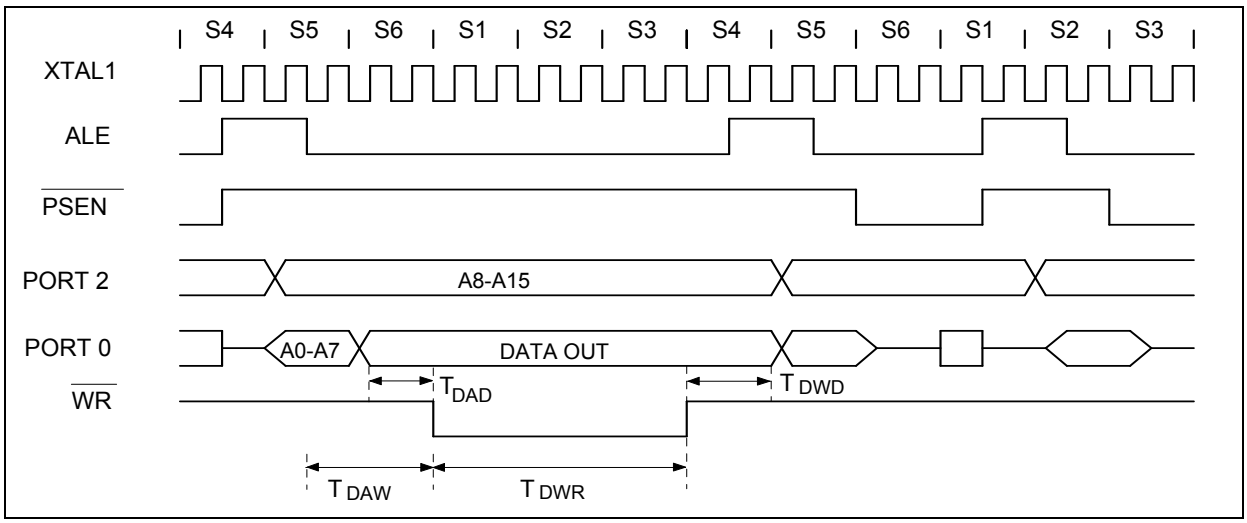
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

20.3.6 Program Operation

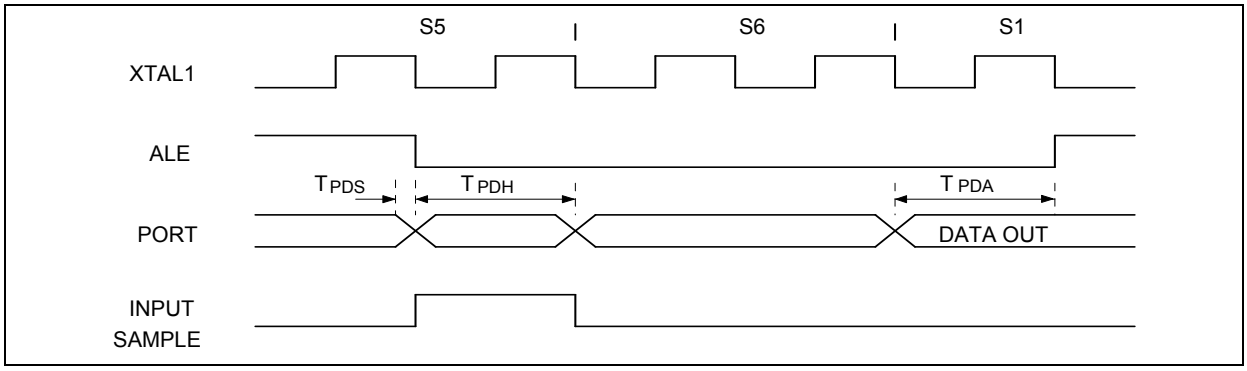
PARAMETER	Symbol	Min.	TYP.	Max.	Unit
VPP Setup Time	TVPS	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
Data Hold Time	TDH	2.0	-	-	μS
Address Setup Time	TAS	2.0	-	-	μS
Address Hold Time	TAH	0	-	-	μS
$\overline{CE}$ Program Pulse Width for Program Operation	TPWP	290	300	310	μS
OECTRL Setup Time	TOCS	2.0	-	-	μS
OECTRL Hold Time	TOCH	2.0	-	-	μS
$\overline{OE}$ Setup Time	TOES	2.0	-	-	μS
$\overline{OE}$ High to Output Float	TDFP	0	-	130	nS
Data Valid from $\overline{OE}$	TOEV	-	-	150	nS

Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the $\overline{PSEN}$ pin must pull in VIH status.

20.4.3 Data Write Cycle



20.4.4 Port Access Cycle



```
    mov     TMOD,#01h           ;Set Timer0 as mode1
    call    Read_Company_ID
    call    Read_Device_ID_HIGH
    call    Read_Device_ID_LOW
    call    Erase_APROM
    call    Erase_Verify_ROM
    call    Program_APROM
    call    Program_Verify_APROM
    call    Software_Reset
    sjmp    $
;*********************************************************************
; * Read_Company_ID
;*********************************************************************
Read_Company_ID:
    mov     SFRCN,#READ_CID
    mov     TL0,#LOW (65536-READ_TIME)
    mov     TH0,#HIGH(65536-READ_TIME)
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    mov     A,SFRFD             ;check Read company ID
    cjne    A,#0DAh,CID_Error
    ret
CID_Error:
    mov     P1,#01h
    sjmp    $
;*********************************************************************
; * read device ID high
;*********************************************************************
Read_Device_ID_HIGH:
    mov     SFRAL,#0FFh
    mov     SFRAH,#0FFh
    mov     SFRCN,#READ_DID
    mov     TL0,#LOW (65536-READ_TIME)
    mov     TH0,#HIGH(65536-READ_TIME)
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    mov     A,SFRFD             ;read device id high byte
    ret
;*********************************************************************
; * read device ID low
```

```
    mov     R1,DPH
    cjne    R1,#HIGH(APROM_END_ADDRESS),wr_lp
    ret
;*****************************************************************************
;*Program Verify APROM BANK, read APROM 55h,AAh,55h,AAh........
;*****************************************************************************
Program_Verify_APROM:
    mov     SFRCN,#PROGRAM_VERIFY_ROM
    mov     DPTR,#0000h
    mov     B,#055h
rd_lp:
    mov     TH0,#HIGH(65536-READ_TIME)
    mov     TL0,#LOW (65536-READ_TIME)
    mov     SFRAL,DPL
    mov     SFRAH,DPH
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    mov     A,SFRFD
    cjne    A,B,Program_Fail
    mov     A,B
    cpl     A
    mov     B,A
    inc     DPTR
    mov     R0,DPL
    cjne    R0,#LOW (APROM_END_ADDRESS),rd_lp
    mov     R1,DPH
    cjne    R1,#HIGH(APROM_END_ADDRESS),rd_lp
    ret
Program_Fail:
    mov     P1,#03h
    sjmp    $
;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU TO APROM
;*****************************************************************************
Software_Reset:
    MOV     CHPCON,#081h    ;CHPCON=081h, SOFTWARE RESET to APROM.
    sjmp    $
    end
```