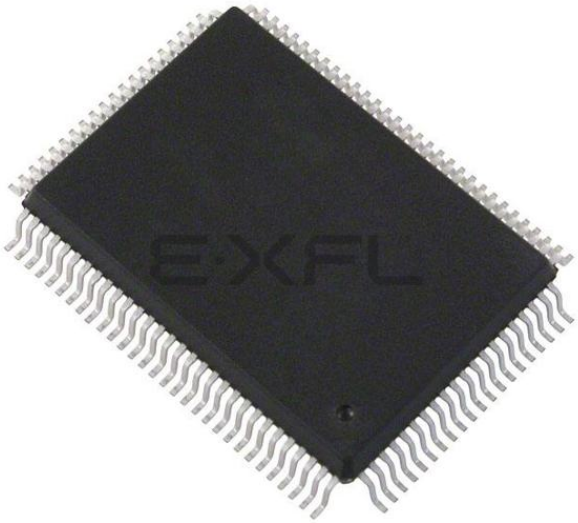

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8/16-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia186espqf100ir03

Table 2. IA186ES TQFP Alphabetic Pin Listing

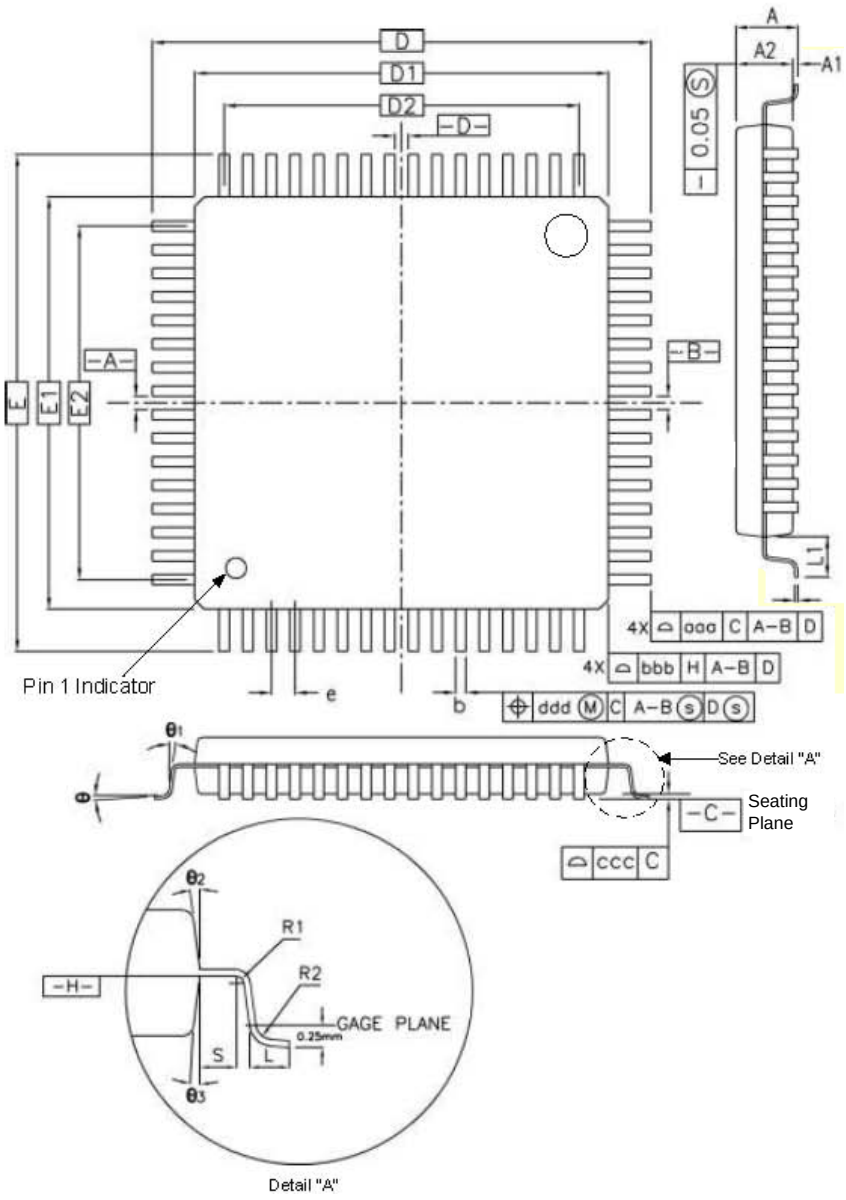
Name	Pin
a0	63
a1	62
a2	60
a3	59
a4	58
a5	57
a6	56
a7	55
a8	54
a9	53
a10	52
a11	51
a12	50
a13	49
a14	48
a15	47
a16	46
a17/pio7	45
a18/pio8	43
a19/pio9	42
ad0	1
ad1	3
ad2	5
ad3	7
ad4	9
ad5	11
ad6	14
ad7	17
ad8	2
ad9	4
ad10	6
ad11	8
ad12	10
ad13	13

Name	Pin
ad14	16
ad15	18
ale	30
ardy	30
bhe_n/aden_n	27
clkouta	39
clkoutb	40
cts0_n/enrx0_n/pio21	23
den_n/ds_n/pio5	72
drq0/int5/pio12	100
drq1/int6/pio13	99
dt/r_n/pio4	71
gnd	12
gnd	36
gnd	41
gnd	64
gnd	87
gnd	93
hlda	67
hold	68
int0	79
int1/select_n	78
int2/inta0_n/pwd/pio31	77
int3/inta1_n/irq	76
int4/pio30	75
lcs_n/once0_n	81
mcs0_n/pio14	73
mcs1_n/pio15	74
mcs2_n/pio24	91
mcs3_n/rfsh_n/pio25	92
nmi	70
pcs0_n/pio16	89
pcs1_npio	88

Name	Pin
pcs2_n/cts1_n/enrx1_n/pio18	86
pcs3_n/rts1_n/rtr1_n/pio19	85
pcs5_n/a1/pio3	83
pcs6_n/a2/pio2	82
rd_n	29
res_n	94
rts0_n/rtr0_n/pio20	26
rxd0/pio23	24
rxd1/pio28	22
s0_n	34
s1_n	33
s2_n	32
s6/lock_n/clkdiv2_n/pio29	19
srdy/pio6	69
tmrin0/pio11	98
tmrin1/pio0	95
tmrout0/pio10	97
tmrout1/pio1	96
txd0/pio22	25
txd1/pio27	21
ucs_n/once1_n	80
uzi_n/pio26	20
v_{CC}	15
v_{CC}	38
v_{CC}	44
v_{CC}	61
v_{CC}	84
v_{CC}	90
whb_n	65
wlb_n	66
wr_n	28
x1	36
x2	37

2.1.3 TQFP Physical Dimensions

The physical dimensions for the TQFP are as shown in Figure 3.



Legend:

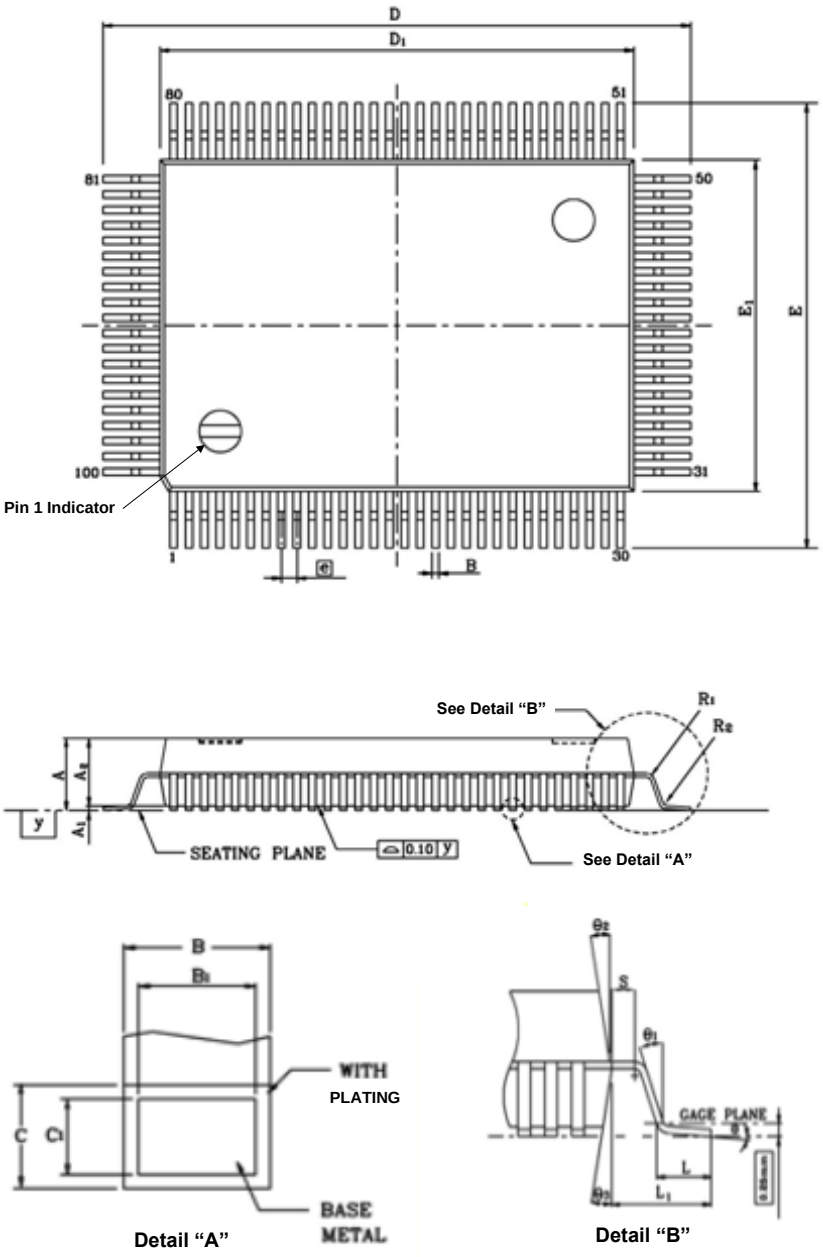
Symbol	Millimeter Min	Nom	Max	Inch Min	Nom	Max
A	–	–	1.20	–	–	0.047
A1	0.05	–	0.15	0.002	–	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.09	–	0.20	0.004	–	0.008
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.00			0.472		
e	0.50 BSC.			0.02 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.00			0.472		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	–	–	0.003	–	–
R2	0.08	–	0.20	0.003	–	0.008
S	0.20	–	–	0.008	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Note:
Control dimensions are in millimeters.

Figure 3. TQFP Package Dimensions

2.1.6 PQFP Physical Dimensions

The physical dimensions for the PQFP are as shown in Figure 6.



Legend						
	Millimeter			Inch		
Symbol	Min	Nom	Max	Min	Nom	Max
A	–	–	3.40	–	–	0.134
A_1	0.25	–	–	0.010	–	–
A_2	2.73	2.85	2.97	0.107	0.112	0.117
B	0.25	0.30	0.38	0.010	0.012	0.015
B_1	0.22	0.30	0.33	0.009	0.012	0.013
C	0.13	0.15	0.23	0.005	0.006	0.009
C_1	0.11	0.15	0.17	0.004	0.006	0.007
D	23.00	23.20	23.40	0.906	0.913	0.921
D_1	19.90	20.00	20.10	0.783	0.787	0.791
E	17.00	17.20	17.40	0.669	0.677	0.685
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.65 BSC.			0.026 BSC.		
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 BSC.			0.063 BSC.		
R_1	0.13	–	–	0.005	–	–
R_2	0.13	–	0.30	0.005	–	0.012
S	0.20	–	–	0.008	–	–
Y	–	–	0.10	–	–	0.004
θ	0°	–	7°	0°	–	7°
θ_1	0°	–	–	0°	–	–
θ_2	9°	10°	11°	9°	10°	11°
θ_3	9°	10°	11°	9°	10°	11°

Notes:
1. Dimensions D_1 and E_1 do not include mold protrusion, but mold mismatch is included. Allowable protrusion is 0.25mm/0.010″ per side.
2. Dimension B does not include Dambar protrusion. Allowable protrusion is 0.08mm/0.003″ total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
3. Controlling dimension: millimeter.

Figure 6. PQFP Package Dimensions

present only during reset. If mcs0_n has been programmed as the chip select for the whole middle chip select address range, these pins may be used as PIOs.

2.2.25 mcs3_n/rfsh_n/pio25—Midrange Memory Chip Select (synchronous outputs with internal pullup)/Automatic Refresh (synchronous output)

The mcs3_n pin provides an indication that a memory access is in progress to the fourth region of the midrange memory block. The size of the Midrange Memory Block and its base address are programmable. The mcs3_n may be configured for either an 8- or 16-bit bus width for the IA186ES microcontroller by the Auxiliary Configuration Register (AUXCON Bit [1]) and is held high during bus hold. If mcs0_n has been programmed as the chip select for the whole middle chip select address range, this pin may be used as PIO. Furthermore, this pin has a weak pullup that is only present during reset.

The rfsh_n signal is timed for auto refresh to PSRAM or DRAM devices. The refresh pulse is only output when the PSRAM or DRAM mode bit is set (EDRAM register Bit [15]). This pulse is of 1.5 clock pulse duration with the rest of the refresh cycle made up of a deassertion period such that the overall refresh time is met. Finally this pin is not tristated during a bus hold.

2.2.26 nmi—Nonmaskable Interrupt (synchronous edge-sensitive input)

This is the highest priority interrupt signal and cannot be masked, unlike int6–int0.

Program execution is transferred to the nonmaskable interrupt vector in the interrupt vector table, upon the assertion of this interrupt (transition from low to high), and this interrupt is initiated at the next instruction boundary. For recognition to be assured, the nmi pin must be held high for at least a clkouta period.

The nmi is not involved in the priority resolution process, which deals with the maskable interrupts and does not have an associated interrupt flag. This allows for a new nmi request to interrupt an nmi service routine that is already underway. The interrupt flag IF is cleared, disabling the maskable interrupts, when an interrupt is taken by the processor. If, during the nmi service routine, the maskable interrupts are re-enabled, by use of STI instruction for example, the priority resolution of maskable interrupts will be unaffected by the servicing of the nmi. For this reason, it is strongly recommended that the nmi interrupt service routine does not enable the maskable interrupts.

2.2.27 pcs1_n–pcs0_n (pio17–pio16)—Peripheral Chip Selects 1–0 (synchronous outputs)

These pins provide an indication that a memory access is under way for the second and first regions, respectively, of the peripheral memory block (I/O or memory address space). The base address of the peripheral memory block is programmable. The pcs3_n–pcs0_n are held high

Table 10. Bus Cycle Types for s2_n, s1_n, and s0_n

s2_n	s1_n	s0_n	Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	Read data from I/O
0	1	0	Write data to I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	None (passive)

2.2.40 s6/lock_n/clkdiv2_n/pio29—Bus Cycle Status Bit [6] (synchronous output)/Bus Lock (synchronous output)/Clock Divide by 2 (input with internal pullup)

The s6 signal is high during the second and remaining cycle periods (i.e., t_2–t_4), indicating that a DMA-initiated bus cycle is under way. The s6 is tristated during bus hold or reset.

The lock_n signal is held low to indicate to other system bus masters that the system bus is being used and that no attempt should be made to try to gain control of it. This signal is only available during t_1 and is intended for emulator use.

The microcontroller enters clock divide-by-2 mode, if clkdiv2_n is held low during power-on-reset. In this mode, the PLL is disabled and the processor receives the external clock divided by 2. Sampling of this pin occurs on the rising edge of res_n.

Should this pin be used as pio29 configured as an input, care should be taken that it is not driven low during power-on-reset. This pin has an internal pullup so it is not necessary to drive the pin high even though it defaults to an input PIO.

2.2.41 srdy/pio6—Synchronous Ready (synchronous level-sensitive input)

This signal is an active high input synchronized to clkouta and indicates to the microcontroller that a data transfer will be completed by the addressed memory space or I/O device.

In contrast to the asynchronous ready (ardy), which requires internal synchronization, srdy permits easier system timing as it already synchronized. Tying srdy high will always assert this ready condition, whereas tying it low will give control to ardy.

2.2.42 tmrin0/pio11—Timer Input 0 (synchronous edge-sensitive input)

This signal may be either a clock or control signal for the internal timer 0. The timer is incremented by the microcontroller after it synchronizes a rising edge of tmrin0. When not used, tmrin0 must be tied high, or when used as pio11 it is pulled up internally.

2.2.49 uzi_n/pio26—Upper Zero Indicate (synchronous output)

This pin allows the designer to determine if an access to the interrupt vector table is in progress by ORing it with Bits [15–10] of the address and data bus (ad15–ad10 on the AI186 and ao15–ao10 on the IA188ES). The uzi_n is the logical AND of the inverted a19–a16 bits. It asserts in the first period of a bus cycle and is held throughout the cycle.

2.2.50 v_{cc}—Power Supply (input)

These pins supply power (+5V ±10%) to the microcontroller.

2.2.51 whb_n (IA186ES only)—Write High Byte (synchronous output with tristate)

This pin and wlb_n provide an indication to the system of which bytes of the data bus (upper, lower, or both) are taking part in a write cycle. The whb_n is asserted with ad15–ad8 and is the logical OR of bhe_n and wr_n. It is tristated during reset.

2.2.52 wlb_n/wb_n—Write Low Byte (IA186ES only) (synchronous output with tristate)/Write Byte (IA188ES only) (synchronous output with tristate)

The wlb_n and whb_n provide an indication to the system of which bytes of the data bus (upper, lower, or both) are taking part in a write cycle. The wlb_n is asserted with ad7–ad0 and is the logical OR of ad0 and wr_n. It is tristated during reset.

On the IA188ES microcontroller, wb_n provides an indication that a write to the bus is occurring. It shares the same early timing as that of the non-multiplexed address bus, and is associated with ad7–ad0. It is tristated during reset.

2.2.53 wr_n—Write Strobe (synchronous output)

This pin provides an indication to the system that the data currently on the bus is to be written to a memory or I/O device. It is tristated during a bus hold or reset.

2.2.54 x1—Crystal Input

This pin and x2 are the connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. An external clock source for the microcontroller is connected to x1 while the x2 pin is left unconnected.

2.2.55 x2—Crystal Input

This pin and x1 are the connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. An external clock source for the microcontroller is connected to x1 while the x2 pin is left unconnected.

Table 13. DC Characteristics Over Commercial Operating Ranges

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage (Except x1)	–	−0.5	0.8	V
V_{IL1}	Clock Input Low Voltage (x1)	–	−0.5	0.8	V
V_{IH}	Input High Voltage (Except res_n and x1)	–	2.0	v_{cc} +0.5	V
V_{IH1}	Input High Voltage (res_n)	–	2.4	v_{cc} +0.5	V
V_{IH2}	Clock Input High Voltage (x1)	–	v_{cc}–0.8	v_{cc} +0.5	V
V_{OL}	Output Low Voltages	I_{OL} = 2.5 mA (s2_n–s0_n)	–	0.45	V
		I_{OL} = 2.0 mA (other)	–	0.45	V
V_{OH}	Output High Voltages[a]	I_{OH} = −2.4 mA @ 2.4 V	2.4	v_{cc} +0.5	V
		I_{OH} = −200 µA @ v_{cc} −0.5	v_{cc} −0.5	v_{cc}	V
I_{CC}	Power Supply Current @ 0°C	v_{cc} = 5.5 V[b]	–	5.9	mA/ MHz
I_{LI}	Input Leakage Current @ 0.5 MHz	0.45 V ≤ V_{IN} ≤ v_{cc}	–	±10	µA
I_{LO}	Output Leakage Current @ 0.5 MHz	0.45 V ≤ V_{OUT} ≤ v_{cc} [c]	–	±10	µA
V_{CLO}	Clock Output Low	I_{CLO} = 4.0 mA	–	0.45	V
V_{CHO}	Clock Output High	I_{CHO} = −500 µA	v_{cc} −0.5	–	V

[a]The lcs_n/once0_n, mcs3_n–mcs0_n, ucs_n/once1_n, and rd_n pins have weak internal pullup resistors. Loading the lcs_n/once0_n and ucs_n/once1_n pins in excess of I_{OH} = −200 µA during reset can cause the device to go into ONCE mode.

[b]Current is measured with the device in reset with the x1 and x2 driven and all other non-power pins open but held high or low.

[c]Testing is performed with the pins floating, either during hold or by invoking the ONCE mode.

wait-state settings must agree with those for any overlapping chip selects as though they had been configured as chip selects. This is true regardless of whether these pins are configured as PIO and enabled (by writing to the MMCS and MPCS registers for the mcs_n chip selects and to the PACS and MPCS registers for the pcs_n chip selects).

Even though pcs4_n is not available as an external pin, it has ready- and wait-state logic and must therefore follow the rules for overlapping chip selects. By contrast, the pcs6_n and pcs5_n have ready and wait-state logic that is disabled when they are configured as address bits a2 and a1, respectively.

If the chip-select-configuration rules are not followed, the processor may hang with the appearance of waiting for a ready signal—even in a system where ready (ardy or srdy) is always set to "1."

4.11 Upper-Memory Chip Select

The ucs_n chip select is for the top of memory. On reset, the microcontroller begins fetching and executing instructions at memory location FFFF0h, so upper memory is usually used for instruction. To this end, ucs_n is active on reset and has a memory range of 64 Kbytes (F0000h to FFFFFh) as default, along with external ready required and three wait states automatically inserted. The lower boundary of ucs_n is programmable to provide ranges of 64 to 512 Kbytes.

4.12 Low-Memory Chip Select

The lcs_n chip select is for lower memory and may be configured for 8- or 16-bit accesses by the AUXCON register. Because the interrupt vector table is at the bottom of memory beginning at 00000h, this pin is usually used for control data memory. Unlike ucs_n, this pin is inactive on reset.

4.13 Midrange-Memory Chip Selects

There are four midrange chip selects, mcs3_n–mcs0_n, which may be used in a user-located memory block. With some exceptions, the base address of the memory block may be located anywhere in the 1-Mbyte memory address space. The memory spaces used by the ucs_n and lcs_n chip selects are excluded, as are pcs6_n, pcs5_n, and pcs3_n–pcs0_n. If the pcs_n chip selects are mapped to I/O space, the MCS address range can overlap the PCS address range.

The mcs0_n chip select may be programmed to be active over the entire MCS range, leaving the mcs3_n–mcs1_n free for use as PIO pins.

The MCS may be configured for 8- or 16-bit accesses by the AUXCON register. The width of the non-UCS/non-LCS memory ranges determines the MCS range bus width. The assertion of the MCS outputs occurs with the same timing as the multiplexed AD address bus.

input or output with or without a weak pull-up or pull-down. A PIO pin can be also programmed as an open-drain output. Each PIO pin regains default status after a POR.

Table 15. Default Status of PIO Pins at Reset

PIO No.	Associated Pin	Power-On Reset Status
0	tmrin1	Input with pullup
1	tmrout1	Input with pulldown
2	pcs6_n/a2	Input with pullup
3	pcs5_n/a1	Normal operation[a]
4	dt/r_n	Normal operation[a]
5	den_n/ds_n	Normal operation[a]
6	srdy	Normal operation[a]
7[b]	a17	Normal operation[a]
8[b]	a18	Normal operation[a]
9[b]	a19	Normal operation[a]
10	tmrout0	Input with pulldown
11	tmrin0	Input with pullup
12	drq0/int5	Input with pullup
13	drq1/int6	Input with pullup
14	mcs0_n	Input with pullup
15	mcs1_n	Input with pullup
16	pcs0_n	Input with pullup
17	pcs1_n	Input with pullup
18	pcs2_n/cts1_n/enrx1_n	Input with pullup
19	pcs3_n/rts1_n/rtr1_n	Input with pullup
20	rts0_n/rtr0_n	Input with pullup
21	cts0_n/enrx0_n	Input with pullup
22	txd0	Input with pullup
23	rxd0	Input with pullup
24	mcs2_n	Input with pullup
25	mcs3_n/rfsh_n	Input with pullup
26[b,c]	uzi_n	Input with pullup
27	txd1	Input with pullup
28	rxd1	Input with pullup
29[b,c]	s6/lock_n/clkdiv2	Input with pullup
30	int4	Input with pullup
31	int2/inta0_n/pwd	Input with pullup

Associated Pin	A	Power-On Reset Status
a17	7	Normal operation[a]
a18	8	Normal operation[a]
a19	9	Normal operation[a]
cts0_n/enrx0_n	21	Input with pullup
den_n/ds_n	5	Normal operation[a]
drq0/int5	12	Input with pullup
drq1/int6	13	Input with pullup
dt/r_n	4	Normal operation[a]
int2/inta0_n/pwd	31	Input with pullup
int4	30	Input with pullup
mcs0_n	14	Input with pullup
mcs1_n	16	Input with pullup
mcs2_n	24	Input with pullup
mcs3_n/rfsh_n	25	Input with pullup
pcs0_n	16	Input with pullup
pcs1_n	17	Input with pullup
pcs2_n/cts1_n/enrx1_n	18	Input with pullup
pcs3_n/rts1_n/rtr1_n	19	Input with pullup
pcs5_n/a1	3	Input with pullup
pcs6_n/a2	2	Input with pullup
rts0_n/rtr0_n	20	Input with pullup
rxd0	23	Input with pullup
rxd1	28	Input with pullup
s6/lock_n/clkdiv2	29	Input with pullup
srdy	6	Normal operation[d]
timrin0	11	Input with pullup
tmrin1	0	Input with pullup
tmrout0	10	Input with pulldown
tmrout1	1	Input with pulldown
txd0	22	Input with pullup
txd1	27	Input with pullup
uzi_n	26	Input with pullup

[a]Input with pullup when used as PIO.
[b]Emulators use these pins and also s2_n–s0_n, res_n, nmi, clkouta, bhe_n, ale, ad15–ad0, and a16–a0.
[c]If bhe_n/aden_n (IA186ES) or rfsh_n/aden_n (IA188ES) is held low during POR, these pins will revert to normal operation.
[d]Input with pulldown option available when used as PIO.

Table 16. Peripheral Control Registers

Register Name	Offset
Peripheral Control Block Registers	
PCB Relocation Register	FEh
Reset Configuration Register	F6h
Processor Release Level Register	F4h
Auxiliary Configuration Register	F2h
System Configuration Register	F0h
Watchdog Timer Control Register	E6h
Enable RCU Register	E4h
Clock Prescaler Register	E2h
Memory Partition Register	E0h
DMA Registers	
DMA1 Control Register	DAh
DMA1 Transfer Count Register	D8h
DMA1 Destination Address High Register	D6h
DMA1 Destination Address Low Register	D4h
DMA1 Source Address High Register	D2h
DMA1 Source Address Low Register	D0h
DMA0 Control Register	CAh
DMA0 Transfer Count Register	C8h
DMA0 Destination Address High Register	C6h
DMA0 Destination Address Low Register	C4h
DMA0 Source Address High Register	C2h
DMA0 Source Address Low Register	C0h
Chip-Select Registers	
pcs_n and mcs_n Auxiliary Register	A8h
Mid-Range Memory Chip-Select Register	A6h
Peripheral Chip-Select Register	A4h
Low-Memory Chip-Select Register	A2h
Upper-Memory Chip-Select Register	A0h
Serial Port 0 Registers	
Serial Port 0 Baud Rate Divisor Register	88h
Serial Port 0 Receive Register	86h
Serial Port 0 Transmit Register	84h
Serial Port 0 Status Register	82h
Serial Port 0 Control Register	80h
PIO Registers	
PIO Data 1 Register	7Ah
PIO Direction Register	78h
PIO Mode 1 Register	76h
PIO Data 0 Register	74h
PIO Direction 0 Register	72h
PIO Mode 0 Register	70h

Register Name	Offset
Timer Registers	
Timer2 Mode and Control Register	66h
Timer2 Max Count Compare A Register	62h
Timer2 Count Register	60h
Timer1 Mode and Control Register	5Eh
Timer1 Max Count Compare B Register	5Ch
Timer1 Max Count Compare A Register	5Ah
Timer1 Count Register	58h
Timer0 Mode and Control Register	56h
Timer0 Max Count Compare B Register	54h
Timer0 Max Count Compare A Register	52h
Timer0 Count Register	50h
Interrupt Registers	
Serial Port 0 Interrupt Control Register	44h
Serial Port 1 Interrupt Control Register	42h
INT4 Interrupt Control Register	40h
INT3 Interrupt Control Register	3Eh
INT2 Interrupt Control Register	3Ch
INT1 Interrupt Control Register	3Ah
INT0 Interrupt Control Register	38h
DMA1/INT6 Interrupt Control Register	36h
DMA0/INT5 Interrupt Control Register	34h
Timer Interrupt Control Register	32h
Interrupt Status Register	30h
Interrupt Request Register	2Eh
Interrupt In-Service Register	2Ch
Interrupt Priority Mask Register	2Ah
Interrupt Mask Register	28h
Interrupt Poll Status Register	26h
Interrupt Poll Register	24h
End-of-Interrupt (EOI) Register	22h
Interrupt Vector Register	20h
Serial Port 1 Registers	
Serial Port 1 Baud Rate Divisor Register	18h
Serial Port 1 Receive Register	16h
Serial Port 1 Transmit Register	14h
Serial Port 1 Status Register	12h
Serial Port 1 Control Register	10h

- Bit [1]—MSIZ (IA186ES only) → When set to 1, 8-bit data accesses are performed in middle chip-select (mcs_n) space and peripheral chip-select space (psc_n—but only if pcs_n is mapped to memory). When 0, 16-bit data accesses are performed.

- Bit [0]—IOSIZ (IA186ES only) → When set to 1, 8-bit data accesses are performed in all I/O space. When 0, 16-bit data accesses are performed.

5.1.5 SYSCON (0f0h)

The SYStem CONfiguration Register controls several miscellaneous system I/O and timing functions. The SYSCON contains 0000h at reset (see Table 21).

Table 21. System Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSEN	MCSBIT	DSDEN	PWD	CBF	CBD	CAF	CAD	RES					F2	F1	F0

- Bit [15]—PSEN → When set to 1, enables the power-save mode causing the internal operating clock to be divided by the value in F2–F0. External or internal interrupts clear PSEN automatically. Software interrupts and exceptions do not.

  Note: The value of PSEN is not restored upon execution of an IRET instruction.

- Bit [14]—MCSBIT → When set to 1, mcs0_n is active over the entire MCS range, thus freeing msc2 _n and mcs1_n to be used as PIO. When 0, it behaves normally.

- Bit [13]—DSDEN → When set to 1, the ds_n/den_n pin functions as ds_n. When 0, it functions as den_n. See the individual pin descriptions for details of data strobe (ds_n) mode versus data enable (den_n) mode.

- Bit [12]—PWD → When set to 1, the pulse width demodulator is enabled. When 0, it is disabled.

- Bit [11]—CBF → When set to 1, the clkoutb output follows the input crystal (PLL) frequency. When 0, it follows the internal clock frequency after the clock divider.

- Bit [10]—CBD → When set to 1, the clkoutb output is driven low. When 0, it is driven as an output per the CBF bit.

- Bit [9]—CAF → When set to 1, the clkouta output follows the input crystal (PLL) frequency. When 0, it follows the internal clock frequency after the clock divider.

- Bit [8]—CAD → When set to 1, the clkouta output is driven low. When 0, it is driven as an output per the CBF bit.
- Bits [7–3]—Reserved → The bits read back as zeros.
- Bits [2–0]—F2–F0 → These bits control the clock divider as shown below.

Note: PSEN must be 1 for the clock divider to function.

F2	F1	F0	Divider Factor
0	0	0	Divide by 1 (2^0)
0	0	1	Divide by 2 (2^1)
0	1	0	Divide by 4 (2^2)
0	1	1	Divide by 8 (2^3)
1	0	0	Divide by 16 (2^4)
1	0	1	Divide by 32 (2^5)
1	1	0	Divide by 64 (2^6)
1	1	1	Divide by 128 (2^7)

5.1.6 WDTCON (0e6h)

The WatchDog Timer CONtrol Register provides control and status for the WDT. The WDTCON contains c080h at reset (see Table 22).

Table 22. Watchdog Timer Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	WRST	RSTFLAG	NMIFLAG	TEST	RES			COUNT							

- Bit [15]—ENA → When set to 1, the WDT is enabled. When 0, it is disabled.
- Bit [14]—WRST → When set to 1, an internal WDT reset is generated when the WDT timeout count (COUNT) is reached. When 0, an NMI will be generated once WDT timeout count is reached and the NMIFLAG bit is 0. If the NMIFLAG bit is 1, an internal WDT reset is generated when the WDT timeout count is reached.
- Bit [13]—RSTFLAG → When set to 1, a WDT timeout event has occurred. This bit may be cleared by software or by an external reset.
- Bit [12]—NMIFLAG → When set to 1, a WDT NMI event has occurred. This bit may be cleared by software or by an external reset. If this bit is 1 when WDT timeout occurs, an internal WDT reset is generated regardless of the state of WRST.
- Bit [11]—TEST → This bit is reserved for chip test and should be always set to 0.

- Bit [15]—DM/IOn → Destination Address Space Select selects memory or I/O space for the destination address. When DM/IO is set to 1, the destination address is in memory space. When 0, it is in I/O space.

- Bit [14]—DDEC → Destination Decrement when set to 1, automatically decrements the destination address after each transfer. The address is decremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [13]—DINC → Destination Increment when set to 1, automatically increments the destination address after each transfer. The address is incremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [12]—SM/IOn → Source Address Space Select selects memory or I/O space for the source address. When set to 1, the source address is in memory space. When 0, it is in I/O space.

- Bit [11]—SDEC → Source Decrement when set to 1, automatically decrements the destination address after each transfer. The address is decremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [10]—SINC → Source Increment when set to 1, automatically increments the destination address after each transfer. The address is incremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [9]—TC → Terminal Count. The DMA decrements the transfer count for each DMA transfer. When set to 1, the source or destination synchronized DMA transfers terminate when the count reaches 0. When 0, they do not terminate when the count reaches 0. Unsynchronized DMA transfers always end when the count reaches 0, regardless of the setting of this bit.

- Bit [8]—INT → Interrupt. When this bit is set to 1, the DMA channel generates an interrupt request on completion of the transfer count. However, for an interrupt to be generated, the TC bit must also be set to 1.

- Bits [7–6]—SYN1–SYN0 → Synchronization Type bits each select channel synchronization types as shown below. The value of these bits is ignored if TDRQ (Bit [4]) is set to 1. A processor reset causes these bits to be set to 11b.

- Bit [6]—THRE Transmit Holding Register Empty → When this bit is 1, it indicates that the corresponding transmit holding register is ready to accept data. This is a read-only bit.

- Bit [5]—FER Framing Error Detected → When the receiver samples the rxd line as low when a stop bit is expected (line high), a framing error is generated setting this bit.

Note: This bit should be reset by software.

- Bit [4]—OER Overrun Error Detected → When new data overwrites valid data in the receive register (because it has not been read), an overrun error is detected setting this bit.

Note: This bit should be reset by software.

- Bit [3]—PER Parity Error Detected → When a parity error is detected in either mode 1 or 3, this bit is set.

Note: This bit should be reset by software.

- Bit [2]—TEMT Transmitter Empty → When both the transmit shift register and the transmit register are empty, this bit is set indicating to software that it is safe to disable the transmitter. This bit is read-only.

- Bit [1]—HS0 Handshake Signal 0 → This bit is the inverted value of cts_n and is read only.

- Bit [0]—RES Reserved.

5.1.26 SP0CT (080h) and SP1CT (010h)

Serial Port ConTrol Registers. These registers control both transmit and receive parts of the respective serial ports. The value of the SP0CT and SP1CT registers is 0000h at reset (see Table 42).

Table 42. Serial Port Control Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA			RSIE	BRK	TB8	FC	TXIE	RXIE	TMODE	RMODE	EVN	PE	MODE		

- Bits [15–13]—DMA DMA Control Field → These bits set up the respective ports for use with DMA transfers as shown below.

- Bit [10]—TB8 Transmit Bit 8 → This is the ninth data bit transmitted when in modes 2 and 3. This bit is cleared at each transmitted word and is not buffered. To transmit data with this bit set high, the following procedure is recommended.

  1. The TEMT bit in the serial port status register must go high.
  2. Set the TB8 bit by writing it to the serial port control register.
  3. Write the transmit character to the serial port transmit register.

- Bit [9]—FC Flow Control Enable → This bit controls the hardware handshake (flow control) by enabling it when set to 1, and vice versa. The type of flow control depends on the value of the ENRX0/ENRX1 and RTS0/RTS1 bits in the AUXCON register.

  – Serial Port 0 is a special case in that, if this bit is 1, the associated pins are used for flow control overriding the Peripheral Chip Select signals.

  – This bit is 0 at reset.

- Bit [8]—TXIE Transmitter Ready Interrupt Enable → This bit enables the generation of an interrupt request whenever the transmit holding register is empty (THRE Bit [1]). The respective port does not generate interrupts when this bit is 0. Interrupts continue to be generated as long as THRE and the TXIE are 1.

- Bit [7]—RXIE Receive Data Ready Interrupt Enable → This bit enables the generation of an interrupt request whenever the receive register contains valid data (RDR Bit [1]). The respective port does not generate interrupts when this bit is 0. Interrupts continue to be generated as long as RDR and the RXIE are 1.

- Bit [6]—TMODE Transmit Mode → The transmit section of the serial port is enabled when this bit is 1. Conversely, the transmit section of the serial port is disabled when this bit is 0.

- Bit [5]—RMODE Receive Mode → The receive section of the serial port is enabled when this bit is 1. Conversely, the receive section of the serial port is disabled when this bit is 0.

- Bit [4]—EVN Even Parity → When this bit is 1, even parity protocol is established. Conversely, odd parity is established when this bit is 0. This bit is valid only when parity is enabled (PE).

- Bit [3]—PE Parity Enable → Parity is enabled when this bit is 1 and disabled when this bit is 0.

- Bit [2–0]—MODE Mode of Operation → These three bits establish the mode of operation of the respective serial port. The valid modes and their functions are shown below.

- Bit [5]—MC Maximum Count → When the timer reaches its maximum count, this bit is set to 1 regardless of the interrupt enable bit. This bit may be used by software polling to monitor timer status rather than through interrupts if desired.

- Bits [4–1]—Reserved. Set to 0.

- Bit [0]—CONT Continuous Mode Bit → The timer will run continuously when this bit is set to 1. The timer will stop after each count run and EN will be cleared if this bit is set to 0.

5.1.32 T2COMPA (062h), T1COMPB (05ch), T1COMPA (05ah), T0COMPB (054h), and T0COMPA (052h)

Timer Maxcount COMpare Registers. These registers contain the maximum count value that is compared to the respective count register. Timer0 and Timer1 have two of these compare registers each.

If Timer0 and/or Timer1 is/are configured to count and compare firstly to register A and then register B, the TMROUT0 or TMROUT1 signals may be used to generate various duty-cycle wave forms.

Timer2 has only one compare register, T2COMPA.

If one of these timer maxcount compare registers is set to 0000h, the respective timer will count from 0000h to FFFFh before generating an interrupt request. For example, a timer configured in this manner with a 40-MHz clock will interrupt every 6.5536 µS.

The value of these registers is 0000h at reset (see Table 53).

Table 53. Timer Maxcount Compare Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15–TC0															

- Bits [15–0]—TC [15–0] Timer Compare Value → The timer will count to the value in the respective register before resetting the count value to 0.

5.1.33 T2CNT (060h), T1CNT (058h), and T0CNT (050h)

Timer CouNT Registers. These registers are incremented by one every four internal clock cycles if the relevant timer is enabled.

The Increment of Timer0 and Timer1 may also be controlled by external signals tmrin0 and tmrin1 respectively, or prescaled by Timer2.

- Bit [15]—DHLT DMA Halt → DMA activity is halted when this bit is 1. It is set to 1 automatically when any non-maskable interrupt occurs and is cleared to 0 when an IRET instruction is executed. Interrupt handlers and other time critical software may modify this bit directly to disable DMA transfers. However, the DHLT bit should not be modified by software if the timer interrupts are enabled as the function of this register as an interrupt request register for the timers would be compromised.

- Bits [14–3]—Reserved.

- Bit [2–0]—TMR [2–0] Timer Interrupt Request → A pending interrupt request is indicated by the respective timer, when any of these bits is 1.

Note: The TMR bit in the REQST register is a logical OR of these timer interrupt requests.

5.1.44 REQST (02eh) (Master Mode)

Interrupt REQueST Register. This is a read-only register and such a read results in the status of the interrupt request bits presented to the interrupt controller. The REQST register is undefined on reset (see Table 65).

Table 65. Interrupt Request Register (Master Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	I4	I3	I2	I1	IO	D1/I6	D0/I5	Res	TMR

- Bits [15–11]—Reserved.

- Bit [10]—SP0 Serial Port 0 Interrupt Request → This is the serial port 0 interrupt state and when enabled is the logical OR of all the serial port 0 interrupt sources, THRE, RDR, BRK1, BRK0, FER, PER, and OER.

- Bit [9]—SP1 Serial Port 1 Interrupt Request → This is the serial port 1 interrupt state and when enabled is the logical OR of all the serial port 1 interrupt sources, THRE, RDR, BRK1, BRK0, FER, PER, and OER.

- Bits [8–4]—I [4–0] Interrupt Requests → When any of these bits is set to 1, it indicates that the relevant interrupt has a pending interrupt.

- Bit [3]—D1/I6 DMA Channel 1/Interrupt 6 Request → When set to 1, it indicates that either the DMA channel 1 or int6 has a pending interrupt.

- Bit [2]—D0/I5 DMA Channel 0/Interrupt 5 Request → When set to 1, it indicates that either the DMA channel 0 or int5 has a pending interrupt.

Table 70. Interrupt MASK Register (Master Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	I4	I3	I2	I1	IO	D1/I6	D0/I5	Res	TMR

- Bits [15–11]—Reserved.
- Bit [10]—SP0 Serial Port 0 Interrupt Mask → Setting this bit to 1 is an indication that the serial port 0 interrupt is masked.
- Bit [9]—SP1 Serial Port 1 Interrupt Mask → Setting this bit to 1 is an indication that the serial port 0 interrupt is masked.
- Bits [8–4]—I [4–0] Interrupt Mask → When any of these bits is set to 1, it is an indication that the relevant interrupt is masked.
- Bit [3]—D1/I6 DMA Channel 1/Interrupt 6 Mask → Setting this bit to 1, is an indication that either the DMA channel 1 or int6 interrupt is masked.
- Bit [2]—D0/I5 DMA Channel 0/Interrupt 5 Mask → When set to 1, it indicates that either the DMA channel 0 or int5 interrupt is masked.
- Bit [1]—Reserved.
- Bit [0]—TMR Timer Interrupt Mask → When set to 1, it indicates that the timer control unit interrupt is masked.

5.1.50 IMASK (028h) (Slave Mode)

The interrupt mask register is read/write. Setting a bit in this register has the effect of setting the MSK bit in the corresponding interrupt control register. Setting a bit to 1, masks the interrupt request. The interrupt request is enabled when the corresponding bit is set to 0. The IMASK register contains 003dh on reset (see Table 71).

Table 71. Interrupt MASK Register (Slave Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/I6	D0/I5	Res	TMR0

- Bits [15–6]—Reserved.
- Bit [5]—TMR2 Timer2 Interrupt Mask → This bit provides the state of the mask bit in the Timer Interrupt Control register. When set to 1, it indicates that the interrupt request is masked.

Table 89. Instruction Set Summary *(Continued)*

Instruction		Opcode – Hex			Clock Cycles		Flags Affected								
Mnemonic	Description	Byte 1	Byte 2	Byte 3–6	IA186ES	IA188ES	O	D	I	T	S	Z	A	P	C
SUB	Subtract imm8 from AL	2C	ib	–	3	3	R	–	–	–	R	R	R	R	R
	Subtract imm16 from AX	2D	iw	–	4	4									
	Subtract imm8 from r/m8	80	/5 ib	–	4/16	4/16									
	Subtract imm16 from r/m16	81	/5 iw	–	4/16	4/20									
	Subtract sign-extended imm8 from r/m16	83	/5 ib	–	4/16	4/20									
	Subtract byte reg from r/m8	28	/r	–	3/10	3/10									
	Subtract word reg from r/m16	29	/r	–	3/10	3/14									
	Subtract r/m8 from byte reg	2A	/r	–	3/10	3/10									
	Subtract r/m16 from word reg	2B	/r	–	3/10	3/14									
TEST	AND imm8 with AL	A8	ib	–	3	3	0	–	–	–	R	R	U	R	0
	AND imm16 with AX	A9	iw	–	4	4									
	AND imm8 with r/m8	F6	/0 ib	data 8	4/10	4/10									
	AND imm16 with r/m16	F7	/0 iw	–	4/10	4/14									
	AND byte reg with r/m8	84	/r	–	3/10	3/10									
	AND word reg with r/m16	85	/r	data 8	3/10	3/14									
WAIT	Performs a NOP	9B	–	–	–	–	–	–	–	–	–	–	–	–	–
XCHG	Exchange word reg with AX	90 +rw	–	–	3	3	–	–	–	–	–	–	–	–	–
	Exchange AX with word reg		–	–	3	3									
	Exchange byte reg with r/byte	86 /r	–	–	4/17	4/17									
	Exchange r/m8 with byte reg		–	–	4/17	4/17									
	Exchange word reg with r/m16	87 /r	–	–	4/17	4/21									
	Exchange r/m16 with word reg		–	–	4/17	4/21									
XLAT	Set AL to memory byte segment:[BX+unsigned AL]	D7	–	–	11	15	–	–	–	–	–	–	–	–	–
XLATB	Set AL to memory byte DS:[BX+unsigned AL]	D7	–	–	11	15									
XOR	XOR imm8 with AL	34	ib	–	3	3	0	–	–	–	R	R	U	R	0
	XOR imm16 with AX	35	iw	–	4	4									
	XOR imm8 with r/m8	80	/6 ib	–	4/16	4/16									
	XOR imm16 with r/m16	81	/6 iw	–	4/16	4/20									
	XOR sign-extended imm8 with r/m16	83	/6 ib	–	4/16	4/20									
	XOR byte reg with r/m8	30	/r	–	3/10	3/10									
	XOR word reg with r/m16	31	/r	–	3/10	3/14									
	XOR r/m8 with byte reg	32	/r	–	3/10	3/10									
	XOR r/m16 with word reg	33	/r	–	3/10	3/14									