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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | 8/16-Bit |
| Speed | 40MHz |
| Connectivity | EBI/EMI, UART/USART |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/ia188esptq100ir03 |

# ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| AMD® | Advanced Micro Devices |
| BIC | Bus Interface and Control |
| CDRAM | Count for Dynamic RAM |
| CSC | Chip Selects and Control |
| DA | Disable Address |
| DMA | Direct Memory Access |
| EOI | End of Interrupt |
| INSERV | In-Service |
| ISR | Interrupt Service Routine |
| LMCS | Low-Memory Chip Select |
| MC | Maximum Count |
| MDRAM | Memory Partition for Dynamic RAM |
| MILES™ | Managed IC Lifetime Extension System |
| MMCS | Midrange Memory Chip Select |
| NMI | nonmaskable interrupt |
| PCB | peripheral control block |
| PIO | programmable I/O |
| PLL | phase-lock-loop |
| POR | power-on reset |
| PQFP | Plastic Quad Flat Package |
| PSRAM | Pseudo-Static RAM |
| RCU | Refresh Control Unit |
| RoHS | Restriction of Hazardous Substances |
| SFNM | Special Fully Nested mode |
| SYSCON | System Configuration Register |
| TQFP | Thin Quad Flat Package |
| UART | Universal Asynchronous Receiver-Transmitter |
| UMCS | Upper Memory Chip Select |
| WDT | Watchdog Timer |

- +5-VDC power supply

# 2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186ES and the IA188ES is provided separately. Refer to sections, figures, and tables for information on the device of interest.

## 2.1 Packages and Pinouts

The Innovasic Semiconductor IA186ES and IA188ES microcontroller is available in the following packages:

- 100-Pin Thin Quad Flat Package (TQFP), equivalent to original SQFP package
- 100-Plastic Quad Flat Package (PQFP), equivalent to original PQFP package

## Table 3. IA188ES TQFP Numeric Pin Listing

| Pin | Name |
|---|---|
| 1 | ad0 |
| 2 | ao8 |
| 3 | ad1 |
| 4 | ao9 |
| 5 | ad2 |
| 6 | ao10 |
| 7 | ad3 |
| 8 | ao11 |
| 9 | ad4 |
| 10 | ao12 |
| 11 | ad5 |
| 12 | gnd |
| 13 | ao13 |
| 14 | ad6 |
| 15 | $v_{CC}$ |
| 16 | ao14 |
| 17 | ad7 |
| 18 | ao15 |
| 19 | s6/lock_n/clkdiv2_n/pio29 |
| 20 | uzi_n/pio26 |
| 21 | txd1/pio27 |
| 22 | rxd1/pio28 |
| 23 | cts0_n/enrx0_n/pio21 |
| 24 | rxd0/pio23 |
| 25 | txd0/pio22 |
| 26 | rts0_n/rtr0_n/pio20 |
| 27 | rfsh2_n/aden_n |
| 28 | wr_n |
| 29 | rd_n |
| 30 | ale |
| 31 | ardy |
| 32 | s2_n |
| 33 | s1_n |
| 34 | s0_n |

| Pin | Name |
|---|---|
| 35 | gnd |
| 36 | x1 |
| 37 | x2 |
| 38 | $v_{CC}$ |
| 39 | clkouta |
| 40 | clkoutb |
| 41 | gnd |
| 42 | a19/pio9 |
| 43 | a18/pio8 |
| 44 | $v_{CC}$ |
| 45 | a17/pio7 |
| 46 | a16 |
| 47 | a15 |
| 48 | a14 |
| 49 | a13 |
| 50 | a12 |
| 51 | a11 |
| 52 | a10 |
| 53 | a9 |
| 54 | a8 |
| 55 | a7 |
| 56 | a6 |
| 57 | a5 |
| 58 | a4 |
| 59 | a3 |
| 60 | a2 |
| 61 | $v_{CC}$ |
| 62 | a1 |
| 63 | a0 |
| 64 | gnd |
| 65 | gnd |
| 66 | wb_n |
| 67 | hlda |

| Pin | Name |
|---|---|
| 68 | hold |
| 69 | srdy/pio6 |
| 70 | nmi |
| 71 | dt/r_n/pio4 |
| 72 | den_n/ds_n/pio5 |
| 73 | mcs0_n/pio14 |
| 74 | mcs1_n/pio15 |
| 75 | int4/pio30 |
| 76 | int3/inta1_n/irq |
| 77 | int2/inta0_n/pwd/pio31 |
| 78 | int1/select_n |
| 79 | int0 |
| 80 | ucs_n/once1_n |
| 81 | lcs_n/once0_n |
| 82 | pcs6_n/a2/pio2 |
| 83 | pcs5_n/a1/pio3 |
| 84 | $v_{CC}$ |
| 85 | pcs3_n/rts1_n/rtr1_n/pio19 |
| 86 | pcs2_n/cts1_n/enrx1_n/pio18 |
| 87 | gnd |
| 88 | pcs1_n/pio17 |
| 89 | pcs0_n/pio16 |
| 90 | $v_{CC}$ |
| 91 | mcs2_n/pio24 |
| 92 | mcs3_n/rfsh_n/pio25 |
| 93 | gnd |
| 94 | res_n |
| 95 | tmrin1/pio0 |
| 96 | tmrout1/pio1 |
| 97 | tmrout0/pio10 |
| 98 | tmrin0/pio11 |
| 99 | drq1/int6/pio13 |
| 100 | drq0/int5/pio12 |

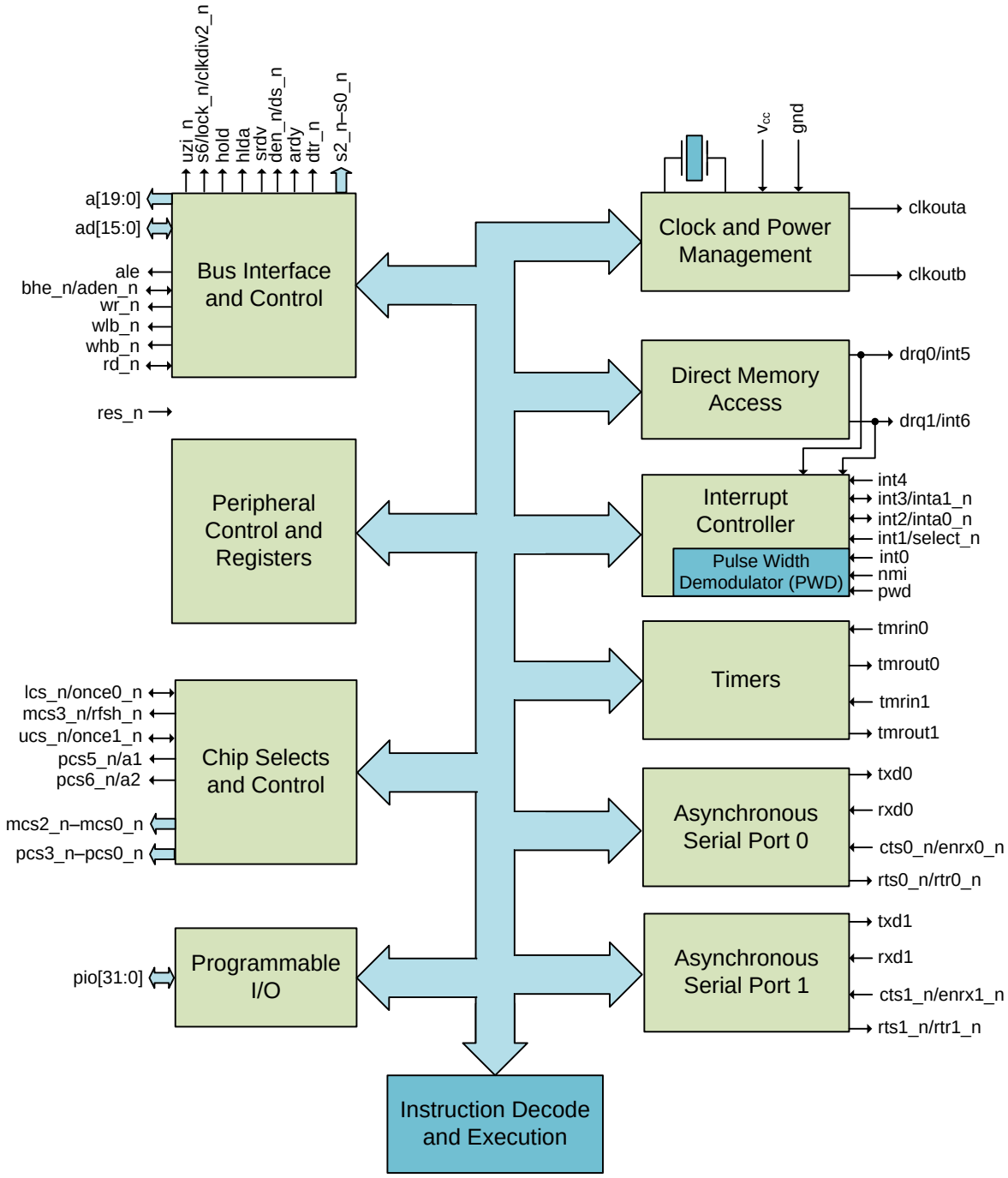


**Figure 7. Functional Block Diagram**

*Note: See pin descriptions for pins that share other functions with PIO pins. Pins pwd, int5, int6, rts1_n/rtr1_n, and cts1_n/enrx1_n are multiplexed with int2_n/inta0_n, drq0, drq0, pcs3_n, and pcs2_n, respectively.*

The current count of timer1 for INT2 and timer0 for INT4 should be inspected by the ISR to determine the pulse width. The timer count register should then be reset by the ISR in readiness for the next pulse.

The timer count rate (one-fourth of the processor clock rate) determines the maximum resolution of the timers. To avoid the delay in servicing a timer interrupt in cases where the pulse width is short, the INT2 and INT4 request bits in the Interrupt Request register may be polled. In cases where the pulse width is greater than the maximum count of the timer, detection is achieved either by monitoring the Maximum Count (MC) bit of the respective timer or by enabling the timer interrupt requests by setting the INT bit in the respective Timer Mode and Control Register.

## 4.25 Asynchronous Serial Ports

There are two independent asynchronous serial ports that employ standard industry communication protocols in their implementation of full duplex, bi-directional data transfers. Functioning independently, either port may be the source or destination of DMA transfers.

The following features are supported:

- Full-duplex data transfers
- 7-, 8-, or 9-bit data transfers
- Odd, even, or no parity
- One or two stop bits
- Break characters of two lengths
- Error detection provided by parity, framing, or overrun errors
- Hardware handshaking achieved with the following selectable control signals:
  - Clear to send (cts_n)
  - Enable receiver request (enrx_n)
  - Ready to send (rts_n)
  - Ready to receive (rtr_n)

- DMA to and from the ports
- Each port has its own maskable interrupts
- 9-bit multidrop protocol
- Each port has an independent baud-rate generator
- Maximum baud rate is 1/16 of the processor clock
- Transmit and receive lines are double buffered

## 4.26 Programmable I/O

Thirty-two pins are programmable as I/O signals (PIO). Table 15 presents them in both numeric and alphabetic order. Because programming a pin as a PIO disables its normal function, it should be done only if the normal function is not required. A PIO pin can be programmed as an

input or output with or without a weak pull-up or pull-down. A PIO pin can be also programmed as an open-drain output. Each PIO pin regains default status after a POR.

### Table 15. Default Status of PIO Pins at Reset

| PIO No. | Associated Pin | Power-On Reset Status |
|---|---|---|
| 0 | tmrin1 | Input with pullup |
| 1 | tmrout1 | Input with pulldown |
| 2 | pcs6_n/a2 | Input with pullup |
| 3 | pcs5_n/a1 | Normal operation[a] |
| 4 | dt/r_n | Normal operation[a] |
| 5 | den_n/ds_n | Normal operation[a] |
| 6 | srdy | Normal operation[a] |
| 7[b] | a17 | Normal operation[a] |
| 8[b] | a18 | Normal operation[a] |
| 9[b] | a19 | Normal operation[a] |
| 10 | tmrout0 | Input with pulldown |
| 11 | tmrin0 | Input with pullup |
| 12 | drq0/int5 | Input with pullup |
| 13 | drq1/int6 | Input with pullup |
| 14 | mcs0_n | Input with pullup |
| 15 | mcs1_n | Input with pullup |
| 16 | pcs0_n | Input with pullup |
| 17 | pcs1_n | Input with pullup |
| 18 | pcs2_n/cts1_n/enrx1_n | Input with pullup |
| 19 | pcs3_n/rts1_n/rtr1_n | Input with pullup |
| 20 | rts0_n/rtr0_n | Input with pullup |
| 21 | cts0_n/enrx0_n | Input with pullup |
| 22 | txd0 | Input with pullup |
| 23 | rxd0 | Input with pullup |
| 24 | mcs2_n | Input with pullup |
| 25 | mcs3_n/rfsh_n | Input with pullup |
| 26[b,c] | uzi_n | Input with pullup |
| 27 | txd1 | Input with pullup |
| 28 | rxd1 | Input with pullup |
| 29[b,c] | s6/lock_n/clkdiv2 | Input with pullup |
| 30 | int4 | Input with pullup |
| 31 | int2/inta0_n/pwd | Input with pullup |

| Associated Pin | A | Power-On Reset Status |
|---|---|---|
| a17 | 7 | Normal operation[a] |
| a18 | 8 | Normal operation[a] |
| a19 | 9 | Normal operation[a] |
| cts0_n/enrx0_n | 21 | Input with pullup |
| den_n/ds_n | 5 | Normal operation[a] |
| drq0/int5 | 12 | Input with pullup |
| drq1/int6 | 13 | Input with pullup |
| dt/r_n | 4 | Normal operation[a] |
| int2/inta0_n/pwd | 31 | Input with pullup |
| int4 | 30 | Input with pullup |
| mcs0_n | 14 | Input with pullup |
| mcs1_n | 16 | Input with pullup |
| mcs2_n | 24 | Input with pullup |
| mcs3_n/rfsh_n | 25 | Input with pullup |
| pcs0_n | 16 | Input with pullup |
| pcs1_n | 17 | Input with pullup |
| pcs2_n/cts1_n/enrx1_n | 18 | Input with pullup |
| pcs3_n/rts1_n/rtr1_n | 19 | Input with pullup |
| pcs5_n/a1 | 3 | Input with pullup |
| pcs6_n/a2 | 2 | Input with pullup |
| rts0_n/rtr0_n | 20 | Input with pullup |
| rxd0 | 23 | Input with pullup |
| rxd1 | 28 | Input with pullup |
| s6/lock_n/clkdiv2 | 29 | Input with pullup |
| srdy | 6 | Normal operation[d] |
| timrin0 | 11 | Input with pullup |
| tmrin1 | 0 | Input with pullup |
| tmrout0 | 10 | Input with pulldown |
| tmrout1 | 1 | Input with pulldown |
| txd0 | 22 | Input with pullup |
| txd1 | 27 | Input with pullup |
| uzi_n | 26 | Input with pullup |

[a]Input with pullup when used as PIO.
[b]Emulators use these pins and also s2_n–s0_n, res_n, nmi, clkouta, bhe_n, ale, ad15–ad0, and a16–a0.
[c]If bhe_n/aden_n (IA186ES) or rfsh_n/aden_n (IA188ES) is held low during POR, these pins will revert to normal operation.
[d]Input with pulldown option available when used as PIO.

- Bit [1]—MSIZ (IA186ES only) → When set to 1, 8-bit data accesses are performed in middle chip-select (mcs_n) space and peripheral chip-select space (psc_n—but only if pcs_n is mapped to memory). When 0, 16-bit data accesses are performed.

- Bit [0]—IOSIZ (IA186ES only) → When set to 1, 8-bit data accesses are performed in all I/O space. When 0, 16-bit data accesses are performed.

### 5.1.5 SYSCON (0f0h)

The SYStem CONfiguration Register controls several miscellaneous system I/O and timing functions. The SYSCON contains 0000h at reset (see Table 21).

**Table 21. System Configuration Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PSEN | MCSBIT | DSDEN | PWD | CBF | CBD | CAF | CAD | RES | | | | | F2 | F1 | F0 |

- Bit [15]—PSEN → When set to 1, enables the power-save mode causing the internal operating clock to be divided by the value in F2–F0. External or internal interrupts clear PSEN automatically. Software interrupts and exceptions do not.

  *Note: The value of PSEN is not restored upon execution of an IRET instruction.*

- Bit [14]—MCSBIT → When set to 1, mcs0_n is active over the entire MCS range, thus freeing msc2 _n and mcs1_n to be used as PIO. When 0, it behaves normally.

- Bit [13]—DSDEN → When set to 1, the ds_n/den_n pin functions as ds_n. When 0, it functions as den_n. See the individual pin descriptions for details of data strobe (ds_n) mode versus data enable (den_n) mode.

- Bit [12]—PWD → When set to 1, the pulse width demodulator is enabled. When 0, it is disabled.

- Bit [11]—CBF → When set to 1, the clkoutb output follows the input crystal (PLL) frequency. When 0, it follows the internal clock frequency after the clock divider.

- Bit [10]—CBD → When set to 1, the clkoutb output is driven low. When 0, it is driven as an output per the CBF bit.

- Bit [9]—CAF → When set to 1, the clkouta output follows the input crystal (PLL) frequency. When 0, it follows the internal clock frequency after the clock divider.

- Bit [15]—DM/IOn → Destination Address Space Select selects memory or I/O space for the destination address. When DM/IO is set to 1, the destination address is in memory space. When 0, it is in I/O space.

- Bit [14]—DDEC → Destination Decrement when set to 1, automatically decrements the destination address after each transfer. The address is decremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [13]—DINC → Destination Increment when set to 1, automatically increments the destination address after each transfer. The address is incremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [12]—SM/IOn → Source Address Space Select selects memory or I/O space for the source address. When set to 1, the source address is in memory space. When 0, it is in I/O space.

- Bit [11]—SDEC → Source Decrement when set to 1, automatically decrements the destination address after each transfer. The address is decremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [10]—SINC → Source Increment when set to 1, automatically increments the destination address after each transfer. The address is incremented by 1 or 2, depending on the byte/word bit (Bn/W, Bit [0]). The address does not change if the increment and decrement bits are set to the same value (00b or 11b).

- Bit [9]—TC → Terminal Count. The DMA decrements the transfer count for each DMA transfer. When set to 1, the source or destination synchronized DMA transfers terminate when the count reaches 0. When 0, they do not terminate when the count reaches 0. Unsynchronized DMA transfers always end when the count reaches 0, regardless of the setting of this bit.

- Bit [8]—INT → Interrupt. When this bit is set to 1, the DMA channel generates an interrupt request on completion of the transfer count. However, for an interrupt to be generated, the TC bit must also be set to 1.

- Bits [7–6]—SYN1–SYN0 → Synchronization Type bits each select channel synchronization types as shown below. The value of these bits is ignored if TDRQ (Bit [4]) is set to 1. A processor reset causes these bits to be set to 11b.

- Bit [5–3]—Reserved. Set to 1.
- Bit [2]—R2 Ready Mode → When set to 1, the external ready is ignored. When 0, an external ready is required. The value of these bits determines the number of wait states inserted.
- Bits [1–0]—R [1–0] Wait-State Value → The value of these bits determines the number of wait states inserted into an access to the lcs_n memory area. This number ranges from 0 to 3 (R1–R0 = 00b to 11b).

### 5.1.21 SP0BAUD (088h)

Serial Port BAUD Rate Divisor Registers.

### 5.1.22 SP1BAUD (018h)

Two baud-rate divisor registers, one for each port, allow the two ports to operate at different baud rates. The value in these registers determines the number of internal processor cycles in one phase (one half period) of the 16x serial clock.

The contents of these registers must be adjusted to reflect the new processor clock frequency if power-save mode is in effect.

The baud rate divisor may be calculated from:

BAUDDIV = (Processor Frequency/(16 x baud rate)) (Equation 2)

By setting the BAUDDIV to 0001h, the maximum baud rate of 1/16 of the internal processor frequency clock is set. This provides a baud rate of 2500 Kbytes at 40 MHz. If the BAUDDIV is set to zero, transmission or reception of data does not occur. The baud rate tolerance is +3.0% and −2.5% with respect to the actual serial port baud rate, not the target baud rate (see Table 37).

If handshaking is employed, the control signals cts_n/enrx_n are deasserted while the receive register has valid unread data. The cts_n/enrx_n signal is reasserted after the data in the receive register is read. The value of the SP0RD and SP1RD registers is undefined at reset (see Table 39).

**Table 39. Serial Port Receive Registers**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | RDATA | | | | | | | |

- Bits [15–8]—Reserved.
- Bits [7–0]—RDATA → Holds valid data while the RDR bit of the respective status register is set.

### 5.1.24 SP0TD (084h) and SP1TD (014h)

Serial Port Transmit Registers. Data is written to these registers by software with the values to be transmitted by the serial port. Double buffering of these transmitters allows for the transmission of data from the transmit shift registers (no software access), while the next data are written into the transmit registers.

The TEMT and THRE bits in the respective Serial Port Status registers indicate the status of these two pairs of registers.

Invoking handshaking requires that rts_n/rtr_n inputs be asserted before the transmitters can send any data which remain held in the transmit and shift registers without affecting the transmit pin. The value of the SPTD registers is undefined at reset (see Table 40).

**Table 40. Serial Port Transmit Registers**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | TDATA | | | | | | | |

- Bits [15–8]—Reserved.
- Bits [7–0]—TDATA → Holds the data to be transmitted.

### 5.1.25 SP0STS (082h) and SP1STS (012h)

Serial Port Status Register. These registers store information concerning the current status of the respective ports. The value of the SP0STS and SP1STS registers is undefined at reset (see Table 41).

DMA Control Bits

| DMA Bits | Receive | Transmit |
|---|---|---|
| 000b | No DMA | No DMA |
| 001b | DMA0 | DMA1 |
| 010b | DMA1 | DMA0 |
| 011b | Reserved | Reserved |
| 100b | DMA0 | No DMA |
| 101b | DMA1 | No DMA |
| 110b | No DMA | DMA0 |
| 111b | No DMA | DMA1 |

– DMA transfers to both serial ports are destination-synchronized operations. When the transmit holding register is empty, a new transfer is requested, corresponding with the assertion of the THRE bit in the status register in non-DMA mode. However, when configured for DMA transfers, the respective transmit interrupt is disabled without regard for the TXIE bit.

– DMA transfers from both serial ports are source-synchronized operations. When the receive holding register contains valid data, a new transfer is requested, corresponding with the assertion of the RDR bit in the status register in non-DMA mode. However, when configured for DMA receives, the respective receive interrupt is disabled without regard for the RXIE bit. This is despite the fact that the RSIE bit may still permit receive status interrupts, depending on its setting.

– DMA transfers do not preclude the use of hardware handshaking.

– If either or both serial ports are configured for DMA transfers, the DMA request is internally generated and the corresponding external DMA signals, drq0 and/or drq1 do not play a role.

- Bit [12]—RSIE Receive Status Interrupt Enable → When an exception occurs during data reception, an interrupt request is generated if enabled by this bit (RSIE = 1). Interrupt requests are made for the error conditions listed (BRK0, BRK1, OER, PER, and FER) in the serial port status register.

- Bit [11]—BRK Send Break → When this bit is set to 1, the txd pin is driven low overriding any data that may be in the course of being shifted out of the transmit shift register.

*Note: See the definitions of long and short break in the Serial Port Status register definition.*

The value of the PDIR0 register is FC0Fh at reset (see Table 48).

**Table 47. PDIR0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PDIR (15–0) | | | | | | | | | | | | | | | |

The value of the PDIR1 register is FFFFh at reset (see Table 48).

**Table 48. PDIR1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PDIR (31–16) | | | | | | | | | | | | | | | |

- Bits [15–0]—PDIR [15–0] PIO Direction 0 Bits → For each bit, if the value is 1, the pin is configured as an input. If 0, as an output. The values of these bits correspond to those in the PIO data registers and PIO mode registers.

- Bits [15–0]—PDIR [31–16] PIO Direction 1 Bits → For each bit, if the value is 1, the pin is configured as an input. If 0, as an output. The values of these bits correspond to those in the PIO data registers and PIO mode registers.

### 5.1.29 PMODE1 (076h) and PMODE0 (070h)

PIO MODE Registers. Each PIO pin is configured as an input or an output by the corresponding bit in the PIO direction register. The bit number of PMODE corresponds to the PIO number (see Table 46, PIO Mode and PIO Direction Settings). The value of the PMODE0 register is 0000h at reset (see Table 49).

**Table 49. PMODE0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMODE (15–0) | | | | | | | | | | | | | | | |

The value of the PMODE1 register is 0000h at reset (see Table 50).

**Table 50. PMODE1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMODE (31–16) | | | | | | | | | | | | | | | |

- Bits [15–0]—PMODE [15–0] PIO Mode 0 Bits → For each bit, if the value is 1, the pin is configured as an input. If 0, an output. The values of these bits correspond to those in the PIO data registers and PIO Mode registers.

- Bits [15–0]—PMODE [31–16] PIO Mode 1 Bits → For each bit, if the value is 1, the pin is configured as an input. If 0, an output. The values of these bits correspond to those in the PIO data registers and PIO Mode registers.

### 5.1.30 T1CON (05eh) and T0CON (056h)

Timer0 and Timer1 Mode and CONtrol Registers. These registers control the operation of Timer0 and Timer1, respectively. The value of the T0CON and T1CON registers is 0000h at reset (see Table 51).

**Table 51. Timer0 and Timer1 Mode and Control Registers**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EN | INHn | INT | RIU | 0 | 0 | 0 | 0 | 0 | 0 | MC | RTG | P | EXT | ALT | CONT |

- Bit [15]—EN Enable Bit → The timer is enabled when the EN bit is 1. The timer count is inhibited when the EN bit is 0. Setting this bit to 1 by writing to the T2CON register requires that the INHn bit be set to 1 during the same write. This bit is write-only and can only be written if the INHn bit (Bit [14]) is set to 1 in the same operation.

- Bit [14]—INHn Inhibit Bit → Gates the setting of the enable (EN) bit. This bit must be set to 1 in the same write operation that sets the enable (EN) bit. This bit always reads as 0.

- Bit [13]—INT Interrupt Bit → An interrupt request is generated when the Count register reaches its maximum, MC = 1, by setting the INT bit to 1. In dual maxcount mode, an interrupt request is generated when the count register reaches the value in maxcount A or maxcount B. No interrupt requests are generated if this bit is set to 0. If an interrupt request is generated and then the enable bit is cleared before said interrupt is serviced, the interrupt request will remain.

- Bit [12]—RIU Register in Use Bit → This bit is set to 1 when the maxcount register B is used to compare to the timer count value. It is set to 0 when the maxcount compare A register is used.

- Bits [11–6]—Reserved. Set to 0.

- Bit [5]—MC Maximum Count → When the timer reaches its maximum count, this bit is set to 1 regardless of the interrupt enable bit. This bit is also set every time maxcount compare register A or B is reached when in dual maxcount mode. This bit may be used by software polling to monitor timer status rather than through interrupts, if desired.

- Bit [4]—RTG Retrigger Bit.

- Bits [15–4]—Reserved. Set to 0.
- Bit [3]—MSK Mask → Any of the interrupt sources may cause an interrupt if the MSK bit is 0. The interrupt sources cannot cause an interrupt if the MSK bit is 1. The Interrupt Mask Register has a duplicate of this bit.
- Bit [2–0]—PR [2–0] Priority → These bits define the priority of the serial port interrupts in relation to other interrupt signals. The interrupt priority is the lowest at 7 upon reset. The values of PR2–PR0 are shown above.

### 5.1.40 DMA1CON/INT6CON (036h) and DMA0CON/INT5CON (034h) (Master Mode)

DMA and INTerrupt CONtrol Register. The DMA0 and DMA1 interrupts have interrupt type 0ah and 0bh, respectively. These pins are configured as external interrupts or DMA requests in the respective DMA Control register. The value of these registers is 000Fh at reset (see Table 61).

**Table 61. DMA and Interrupt Control Register (Master Mode)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | MSK | PR2–PR0 | | |

- Bits [15–4]—Reserved. Set to 0.
- Bit [3]—MSK Mask → Any of the interrupt sources may cause an interrupt if the MSK bit is 0. The interrupt sources cannot cause an interrupt if the MSK bit is 1. The Interrupt Mask Register has a duplicate of this bit.
- Bits [2–0]—PR [2–0] Priority → These bits define the priority of the serial port interrupts in relation to other interrupt signals. The interrupt priority is the lowest at 7 upon reset. The values of PR2–PR0 are shown above.

### 5.1.41 DMA1CON/INT6 (036h) and DMA0CON/INT5 (034h) (Slave Mode)

DMA and INTerrupt CONtrol Register. The two DMA control registers maintain their original functions and addressing that they possessed in Master Mode. These pins are configured as external interrupts or DMA requests in the respective DMA Control register. The value of these registers is 000Fh at reset (see Table 62).

**Table 62. DMA and Interrupt Control Register (Slave Mode)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | MSK | PR2–PR0 | | |

- Bit [1]—Reserved.

- Bit [0]—TMR Timer Interrupt Request → This is the timer interrupt state and is the logical OR of the timer interrupt requests. When set to 1, it indicates that the timer control unit has a pending interrupt.

### 5.1.45 REQST (02eh) (Slave Mode)

This read-only register results in the status of interrupt request bits being presented to the interrupt controller. The status of these bits is available when this register is read. This register is read-only.

When an internal interrupt request (D1/I6, D0/I5, TMR2, TMR1, or TMR0) occurs, the respective bit is set to 1. The internally generated interrupt acknowledge resets these bits. The REQST register contains 0000h on reset (see Table 66).

**Table 66. Interrupt Request Register (Slave Mode)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | TMR2 | TMR1 | D1/I6 | D0/I5 | Res | TMR0 |

- Bits [15–6]—Reserved.

- Bit [5]—TMR2 Interrupt Requests → When set to 1, it indicates that Timer2 has a pending interrupt.

- Bit [4]—TMR1 Interrupt Requests → When set to 1, it indicates that Timer1 has a pending interrupt.

- Bit [3]—D1/I6 DMA Channel 1/Interrupt 6 Request → When set to 1, it indicates that either the DMA channel 1 or int6 has a pending interrupt.

- Bit [2]—D0/I5 DMA Channel 0/Interrupt 5 Request → When set to 1, it indicates that either the DMA channel 0 or int5 has a pending interrupt.

- Bit [1]—Reserved.

- Bit [0]—TMR0 Timer Interrupt Request → When set to 1, it indicates that Timer0 has a pending interrupt.

### 5.1.46 INSERV (02ch) (Master Mode)

IN-SERVice Register. The interrupt controller sets the bits in this register when the interrupt is taken. The INSERV register contains 0000h on reset (see Table 67).

**Table 77. Alphabetic Key to Waveform Parameters** *(Continued)*

| No. | Name | Description | Min[a] | Max[a] |
|---|---|---|---|---|
| 1 | tDVCL | Data in Setup | 10 | – |
| 19 | tDXDL | den_n Inactive to dt/r_n Low | 0 | – |
| 58 | tHVCL | hld Setup Time | 10 | – |
| 53 | tINVCH | Peripheral Setup Time | 10 | – |
| 54 | tINVCL | drq Setup Time | 10 | – |
| 86 | tLCRF | lcs_n Inactive to rfsh_n Active Delay | 2tCLCL | – |
| 23 | tLHAV | ale High to Address Valid | 7.5 | – |
| 10 | tLHLL | ale Width | tCLCH-5 | – |
| 13 | tLLAX | *ad* Address Hold from ale Inactive | tCHCL | – |
| 61 | tLOCK | Maximum PLL Lock Time | – | 0.5 |
| 84 | tLRLL | lcs_n Precharge Pulse Width | tCLCL+tCLCHH | – |
| 57 | tRESIN | res_n Setup Time | 10 | – |
| 85 | tRFCY | rfsh_n Cycle Time | 6tCLCL | – |
| 29 | tRHAV | rd_n Inactive to *ad* Address Active | tCLCL | – |
| 59 | tRHDX | rd_n High to Data Hold on *ad* Bus | 0 | – |
| 28 | tRHLH | rd_n Inactive to ale High | tCLCH | – |
| 26 | tRLRH | rd_n Pulse Width | tCLCL | – |
| 47 | tSRYCL | srdy Transition Setup Time | 10 | – |
| 35 | tWHDEX | wr_n Inactive to den_n Inactive | tCLCH | – |
| 34 | tWHDX | Data Hold after wr_n | tCLCL | – |
| 33 | tWHLH | wr_n Inactive to ale High | tCLCH | – |
| 32 | tWLWH | wr_n Pulse Width | 2tCLCL | – |

[a]In nanoseconds.

**Table 78. Numeric Key to Waveform Parameters**

| No. | Name | Description | Min[a] | Max[a] |
|---|---|---|---|---|
| 1 | tDVCL | Data in Setup | 10 | – |
| 2 | tCLDX | Data in Hold | 0 | – |
| 3 | tCHSV | Status Active Delay | 0 | 6 |
| 4 | tCLSH | Status Inactive Delay | 0 | 6 |
| 5 | tCLAV | *ad* Address Valid Delay | 0 | 12 |
| 6 | tCLAX | Address Hold | 0 | 12 |
| 7 | tCLDV | Data Valid Delay | 0 | 12 |
| 8 | tCHDX | Status Hold Time | 0 | – |
| 9 | tCHLH | ale Active Delay | 0 | 8 |
| 10 | tLHLL | ale Width | tCLCH-5 | – |
| 11 | tCHLL | ale Inactive Delay | 0 | 8 |
| 12 | tAVLL | *ad* Address Valid to ale Low | tCLCH | – |
| 13 | tLLAX | *ad* Address Hold from ale Inactive | tCHCL | – |

[a]In nanoseconds.

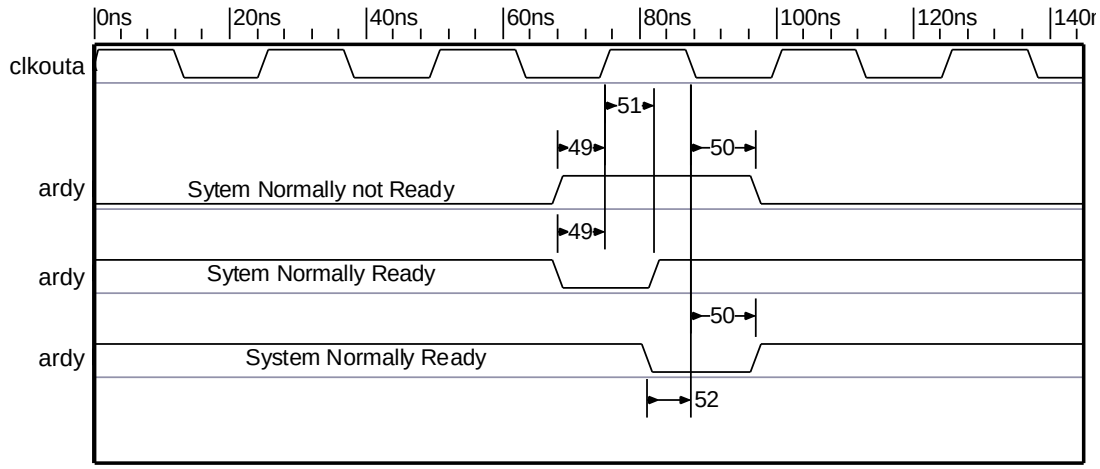


**Figure 24. ardy—Asynchronous Ready**

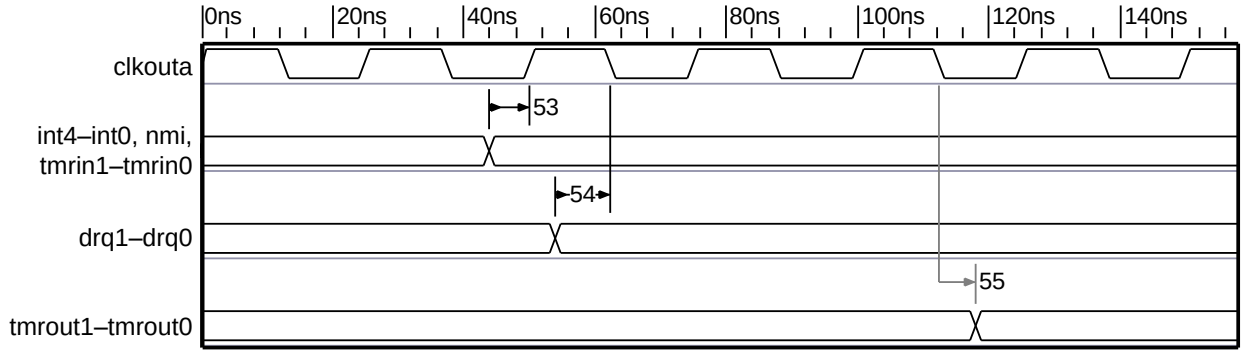


**Figure 25. Peripherals**

## Table 88. Reset and Bus Hold Timing

| No. | Name | Description | Min[a] | Max[a] |
|---|---|---|---|---|
| **Reset and Bus Hold Timing Requirements** | | | | |
| 5 | tCLAV | *ad* Address Valid Delay | 0 | 12 |
| 15 | tCLAZ | *ad* Address Float Delay | 0 | 12 |
| 57 | tRESIN | res_n Setup Time | 10 | – |
| 58 | tHVCL | hld Setup Time | 10 | – |
| **Reset and Bus Hold Timing Responses** | | | | |
| 62 | tCLHAV | hlda Valid Delay | 0 | 7 |
| 63 | tCHCZ | Command Lines Float Delay | 0 | 12 |
| 64 | tCHCV | Command Lines Valid Delay (after Float) | 0 | 12 |

[a]In nanoseconds.

## Table 91. Innovasic/AMD Part Number Cross-Reference for the PQFP

| Innovasic Part Number | AMD Part Number | Package Type | Temperature Grade |
|---|---|---|---|
| IA186ES-PQF100I-R-03 lead free (RoHS-compliant) | AM186ES-20KC\W<br>AM186ES-25KC\W<br>AM186ES-33KC\W<br>AM186ES-40KC\W<br>AM186ES-20KI\W<br>AM186ES-25KI\W<br>AM186ES-33KI\W<br>AM186ES-40KI\W | 100-Pin Plastic Quad Flat Package (PQFP) | Industrial |
| IA188ES-PQF100I-R-03 lead free (RoHS-compliant) | AM188ES-20KC\W<br>AM188ES-25KC\W<br>AM188ES-33KC\W<br>AM188ES-40KC\W<br>AM188ES-20KI\W<br>AM188ES-25KI\W<br>AM188ES-33KI\W<br>AM188ES-40KI\W | | |

# 10. Revision History

Table 93 presents the sequence of revisions to document IA211050902.

**Table 93. Revision History**

| Date | Revision | Description | Page(s) |
|---|---|---|---|
| August 17, 2007 | 11 | Edition released. | NA |
| January 31, 2008 | 12 | Errata 6 and 7 added. | 136 |
| February 19, 2008 | 13 | Errata 7 clarified. | 136 |
| August 7, 2008 | 14 | Column 2 of Peripheral Control Registers table changed from “Serial Port 0” to “Serial Port 1” in 6 bottom rows. | 9 |
| December 24, 2008 | 15 | Document reformatted and elements added to meet publication standards. Improved figures and tables. Added Conventions, Acronyms and Abbreviations, and Summary of Errata table. | All |
| January 25, 2010 | 16 | Corrected PQFP Package Dimensions table. | 30 |
| February 25, 2011 | 17 | Updated section 2.2.50 to clarify that power rating is ±10%; Removed packaging options to support the elimination of SnPb lead plating options. | 44, 148, 149 |
| July 22, 2011 | 18 | Corrected pin names for various pins. | 17-29 |
| November 15, 2011 | 19 | Corrected pin names for pins 42, 43 | 29 |
| May 2, 2014 | 20 | Corrected the address for the DMA1 Source Address Low Register. | 63 |
| January 9, 2015 | 21 | Modified the chip compatibility claim. | 15 |