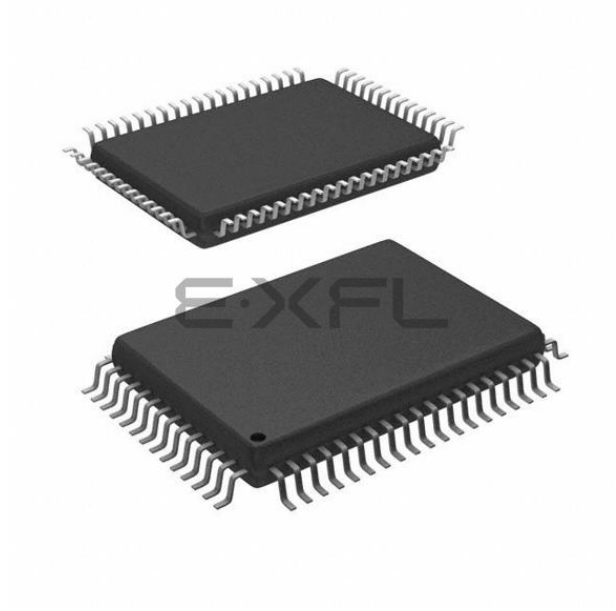
Infineon Technologies - MB89635RPF-G-1447E1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1447e1

(Continued)

- UART
  CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  Start by an external input capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Bus interface function
  With hold and ready function

- Other specifications
  Both MB89630 series and MB89635R/636R/637R is the same.
- Electrical specifications/electrical characteristics
  Electrical specifications of the MB89635R/636R/637R series are the same as that of the MB89630 series.
  Electrical characteristics of both the series are much the same.

■ CORRESPONDENCE BETWEEN THE MB89630 AND MB89630R SERIES

- The MB89630R series is the reduction version of the MB89630 series.
- The the MB89630 and MB89630R series consist of the following products:

MB89630 series	MB89635	MB89636	MB89637	MB89P637	MB89PV630
MB89630R series	MB89635R	MB89636R	MB89637R		

■ PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
30	22	23	X0	A	Main clock crystal oscillator pins
31	23	24	X1		
28	20	21	MOD0	D	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
29	21	22	MOD1		
27	19	20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
56 to 49	48 to 41	49 to 42	P00/AD0 to P07/AD7	F	General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.
48 to 41	40 to 33	41 to 34	P10/A08 to P17/A157	F	General-purpose I/O ports When an external bus is used, these ports function as an upper address output.
40	32	33	P20/BUFC	H	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	31	32	P21/$\overline{HAK}$	H	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.
38	30	31	P22/HRQ	F	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	29	30	P23/RDY	F	General-purpose output port When an external bus is used, this port functions as a ready input.
36	28	29	P24/CLK	H	General-purpose output port When an external bus is used, this port functions as a clock output.
35	27	28	P25/$\overline{WR}$	H	General-purpose output port When an external bus is used, this port functions as a write signal output.
34	26	27	P26/$\overline{RD}$	H	General-purpose output port When an external bus is used, this port functions as a read signal output.

*1: DIP-64P-M01
*2: MDP-64C-P02
*3: FPT-64P-M23
*4: FPT-64P-M06
*5: MQP-M64C-P01

(Continued)

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

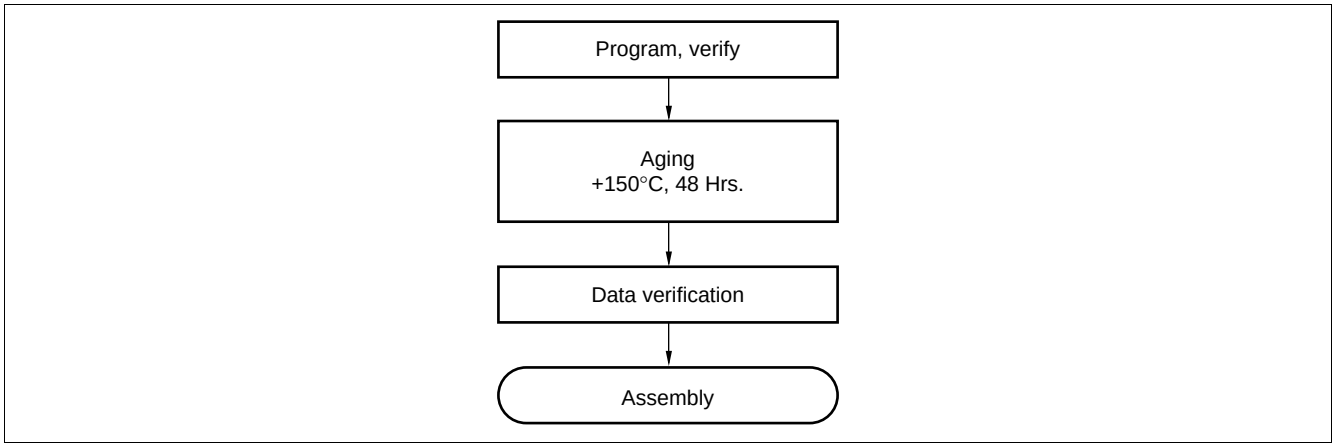
(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$. (Note that addresses 8000_H to $FFFF_H$ in the operating mode assign to 0000_H to $7FFF_H$ in EPROM mode).

(3) Load option data into addresses 0000_H to 0006_H of the EPROM programmer.
(For information about each corresponding option, see “8. OTPROM Option Bit Map”.)

(4) Program with the EPROM programmer.

4. Recommended Screening Conditions

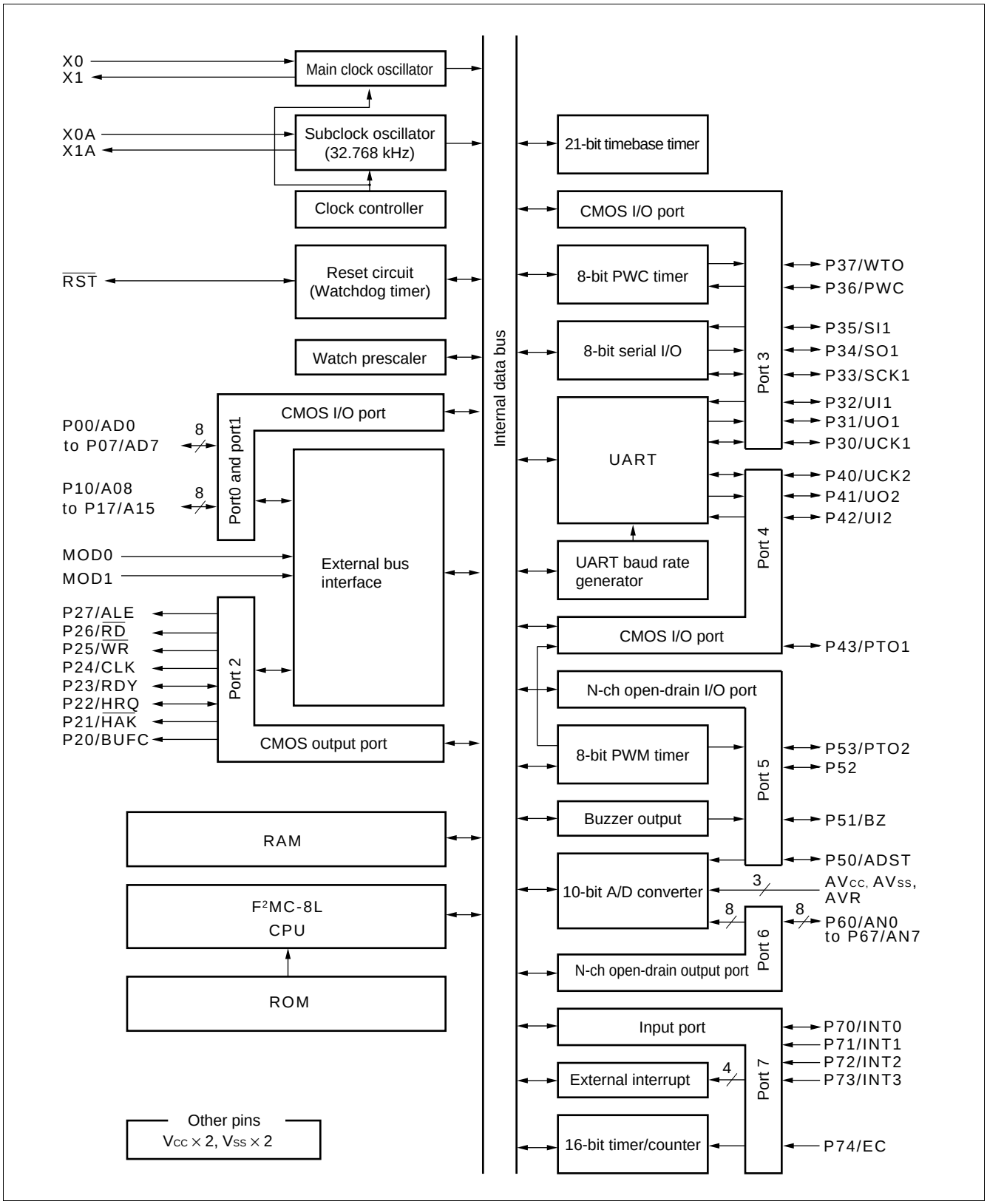
High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ BLOCK DIAGRAM

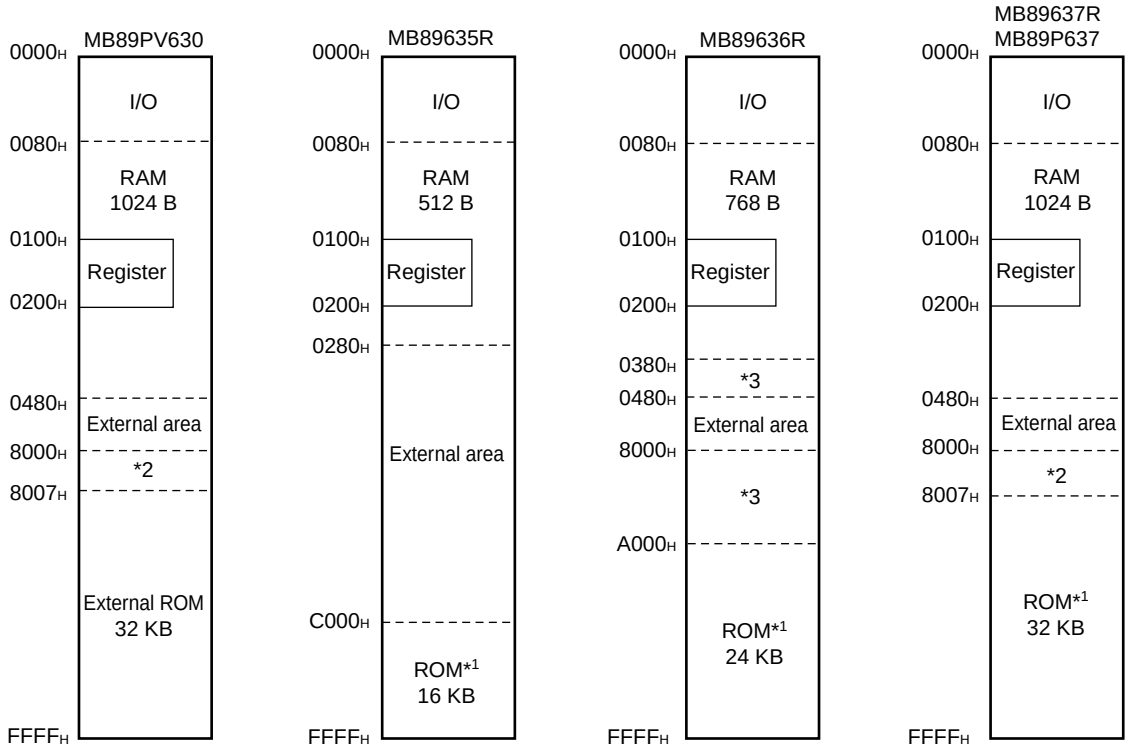


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89630R series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89630R series is structured as illustrated below.

• Memory space



*1: The ROM area is an external area depending on the mode.

*2: Addresses 8000H to 8006H for the MB89P637 comprise an option area, do not use this area for the MB89PV630 and MB89637R.

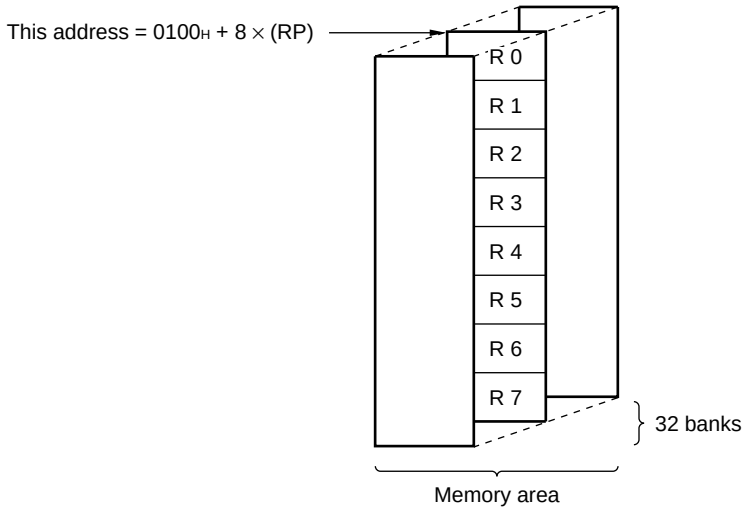
*3: The access is forbidden in the external bus mode.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).

• Register bank configuration



(Continued)

Address	Read/write	Register name	Register description
20H	(R/W)	ADC1	A/D converter control register 1
21H	(R/W)	ADC2	A/D converter control register 2
22H	(R/W)	ADDH	A/D converter data register (H)
23H	(R/W)	ADDL	A/D converter data register (L)
24H	(R/W)	EIC1	External interrupt control register 1
25H	(R/W)	EIC2	External interrupt control register 2
26H	Vacancy		
27H	Vacancy		
28H	(R/W)	CNTR1	PWM timer control register 1
29H	(R/W)	CNTR2	PWM timer control register 2
2AH	(R/W)	CNTR3	PWM timer control register 3
2BH	(W)	COMR1	PWM timer compare register 1
2CH	(W)	COMR2	PWM timer compare register 2
2DH	(R/W)	SMC	UART serial mode control register
2EH	(R/W)	SRC	UART serial rate control register
2FH	(R/W)	SSD	UART serial status/data register
30H	(R) (W)	SIDR SODR	UART serial input data control register UART serial output data control register
31H to 7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacancy		

Note: Do not use vacancies.

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89635R/ 636R/637R/ PV630
				—	1.5	2.5	mA	MB89P637
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89635R/ 636R/637R/ PV630
				—	500	700	µA	MB89P637
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	

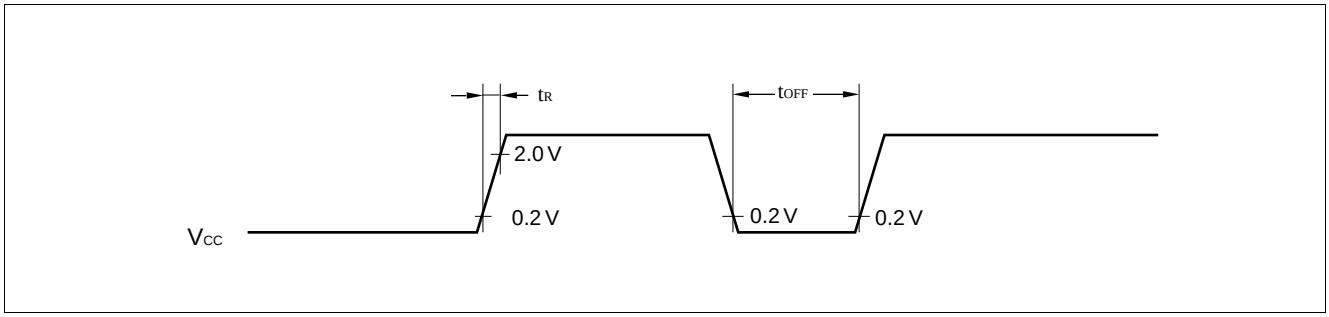
(Continued)

(2) Specification for Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Min. interval time for the next power-on reset

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



(3) Clock Timing

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	External clock
Input clock rising/ falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

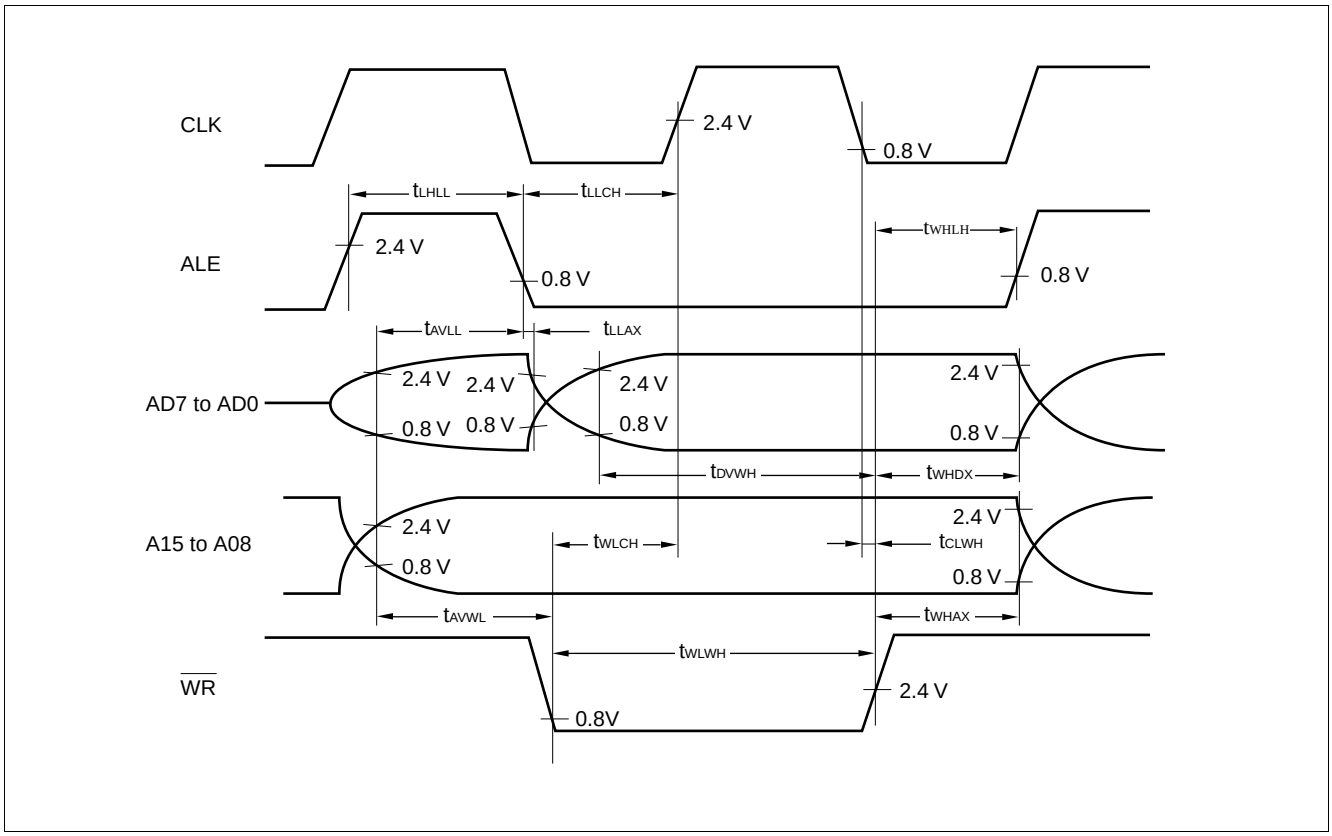
(7) Bus Write Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to AD0, ALE A15 to A08	—	1/4 t_{inst}*1 – 64 ns*2	—	µs	
ALE ↓ time → address loss time	t_{LLAX}			5	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 60 ns*2	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*1 – 20 ns*2	—	µs	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to AD0, $\overline{WR}$		1/2 t_{inst}*1 – 60 ns*2	—	µs	
$\overline{WR}$ ↑ → address loss time	t_{WHAX}	$\overline{WR}$, A15 to A08		1/4 t_{inst}*1 – 40 ns*2	—	µs	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to AD0, $\overline{WR}$		1/4 t_{inst}*1 – 40 ns*2	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 40 ns*2	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*1 – 40 ns*2	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}			0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*1 – 35 ns*2	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE,CLK		1/4 t_{inst}*1 – 30 ns*2	—	µs	

*1: For information on t_{inst}, see “(4) Instruction Cycle”.

*2: This characteristics are also applicable to the bus read timing.



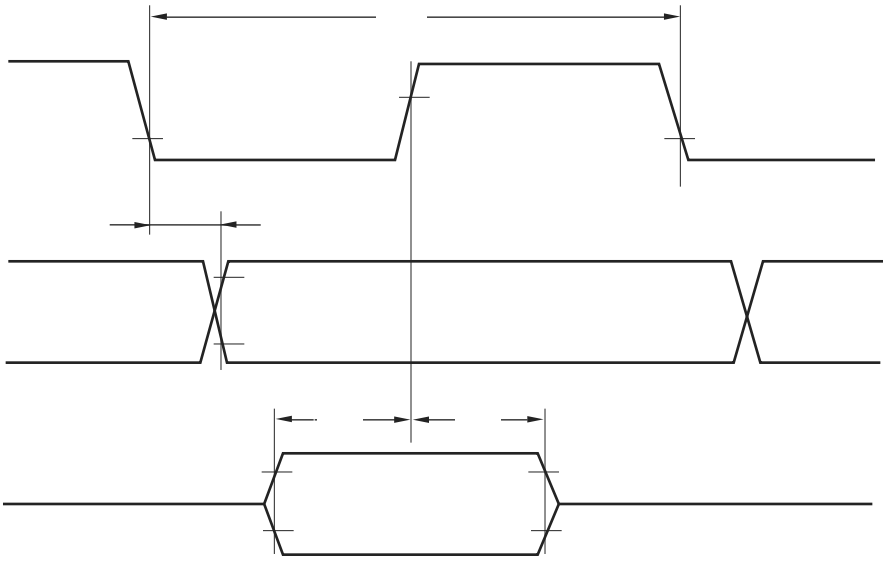
(9) Serial I/O Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

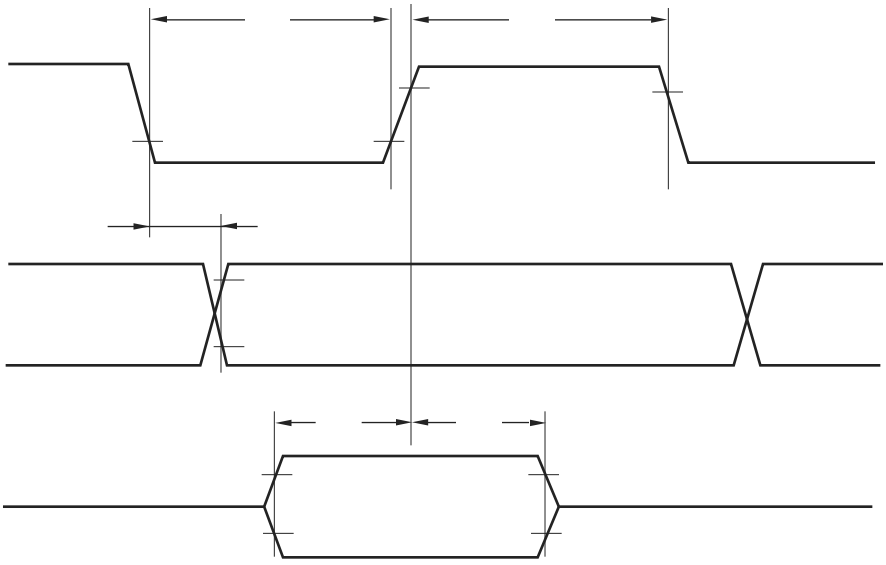
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, UCK1, UCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time UCK1 ↑ → valid UI1 hold time UCK2 ↑ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, UCK1, UCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, UCK1, UCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↓ → valid SI1 hold time UCK1 ↓ → valid UI1 hold time UCK2 ↓ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

• **Internal shift clock mode**



• **External shift clock mode**

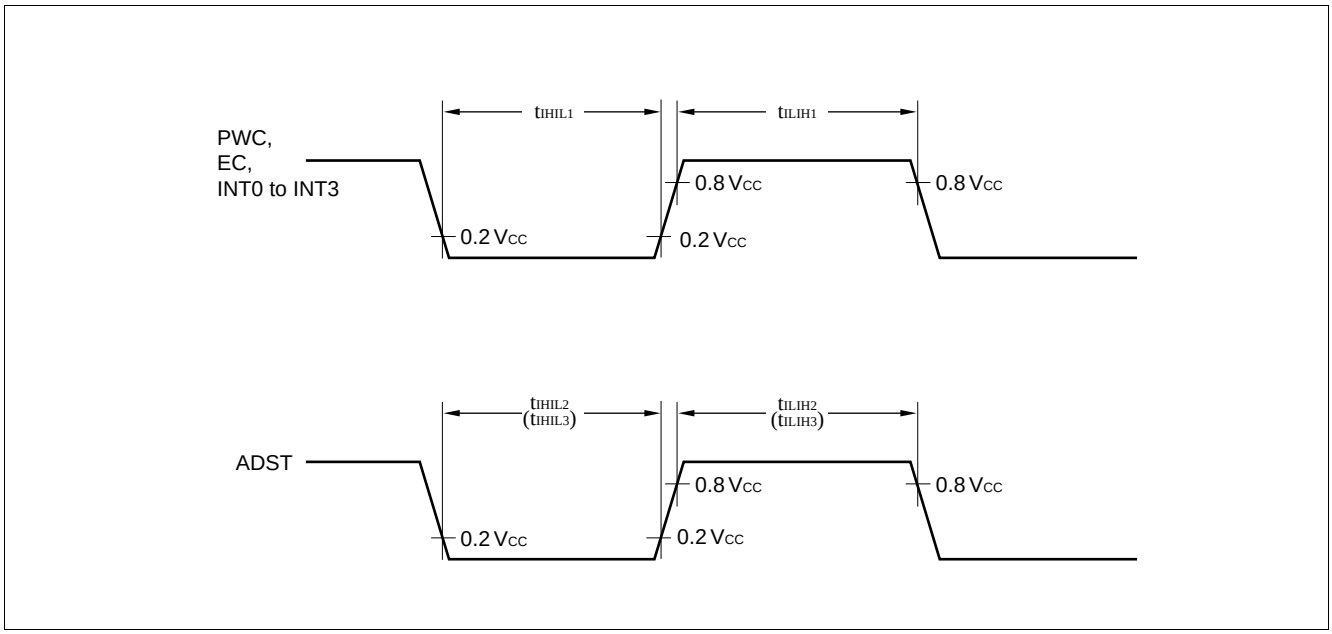


(10) Peripheral Input Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	PWC, INT0 to INT3,EC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	ADST	2^8 t_{inst}*	—	µs	A/D mode
Peripheral input “L” pulse width 2	t_{IHIL2}		2^8 t_{inst}*	—	µs	A/D mode
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	2^8 t_{inst}*	—	µs	Sense mode
Peripheral input “L” pulse width 3	t_{IHIL3}		2^8 t_{inst}*	—	µs	Sense mode

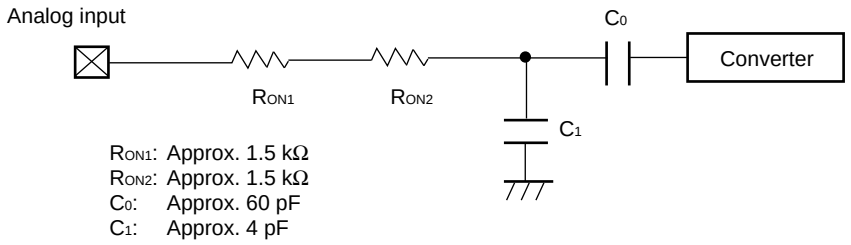
* : For information on t_{inst}, see “(4) Instruction Cycle”.



7. Notes on Using A/D Converter

- **Input impedance of the analog input pins**
  The output impedance of the external circuit for the analog input must satisfy the following conditions.
  If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 kΩ.

- **Analog input circuit model**



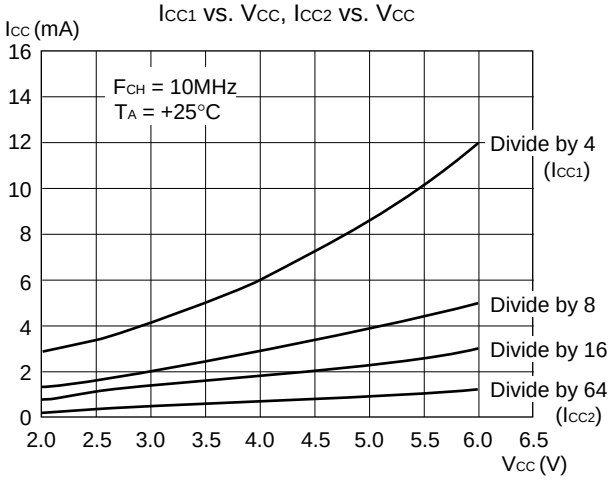
R_{ON1}: Approx. 1.5 kΩ
R_{ON2}: Approx. 1.5 kΩ
C_0: Approx. 60 pF
C_1: Approx. 4 pF

Note: The values mentioned here should be used as a guideline.

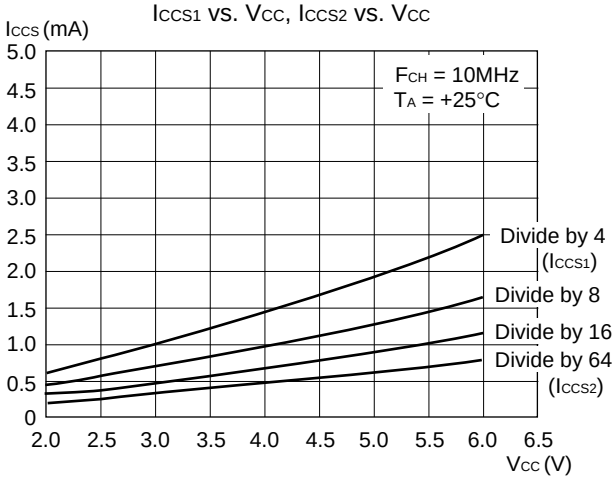
- **Error**
  The smaller the | AVR–AVss |, the greater the error would become relatively.

(5) Power Supply Current (External Clock)

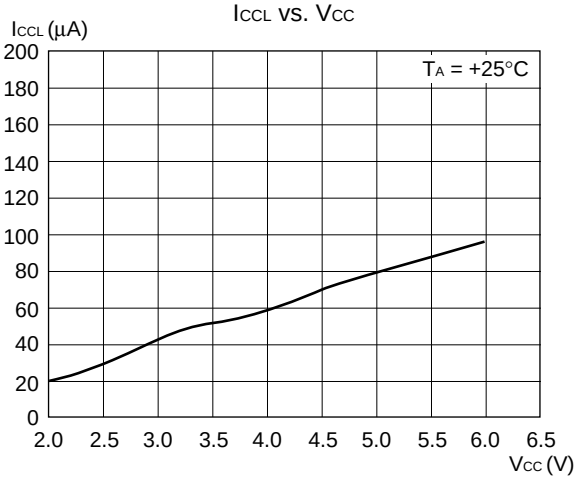
I_{CC1} vs. V_{CC}, I_{CC2} vs. V_{CC}



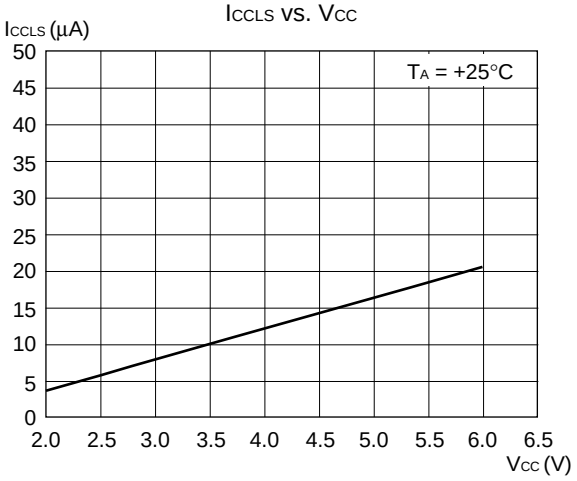
I_{CCS1} vs. V_{CC}, I_{CCS2} vs. V_{CC}



I_{CCL} vs. V_{CC}



I_{CCLS} vs. V_{CC}



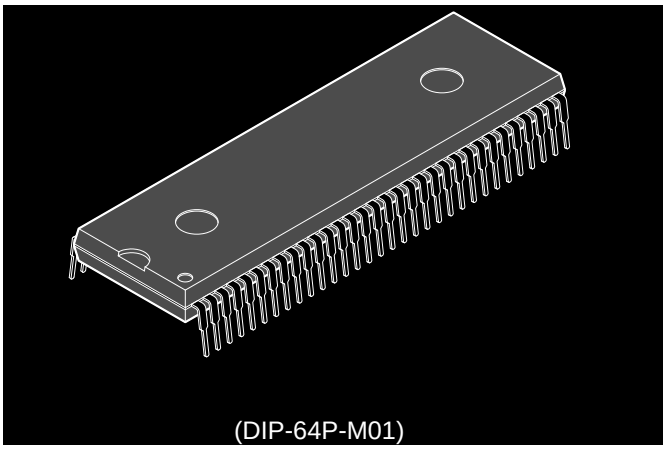
(Continued)

■ MASK OPTIONS

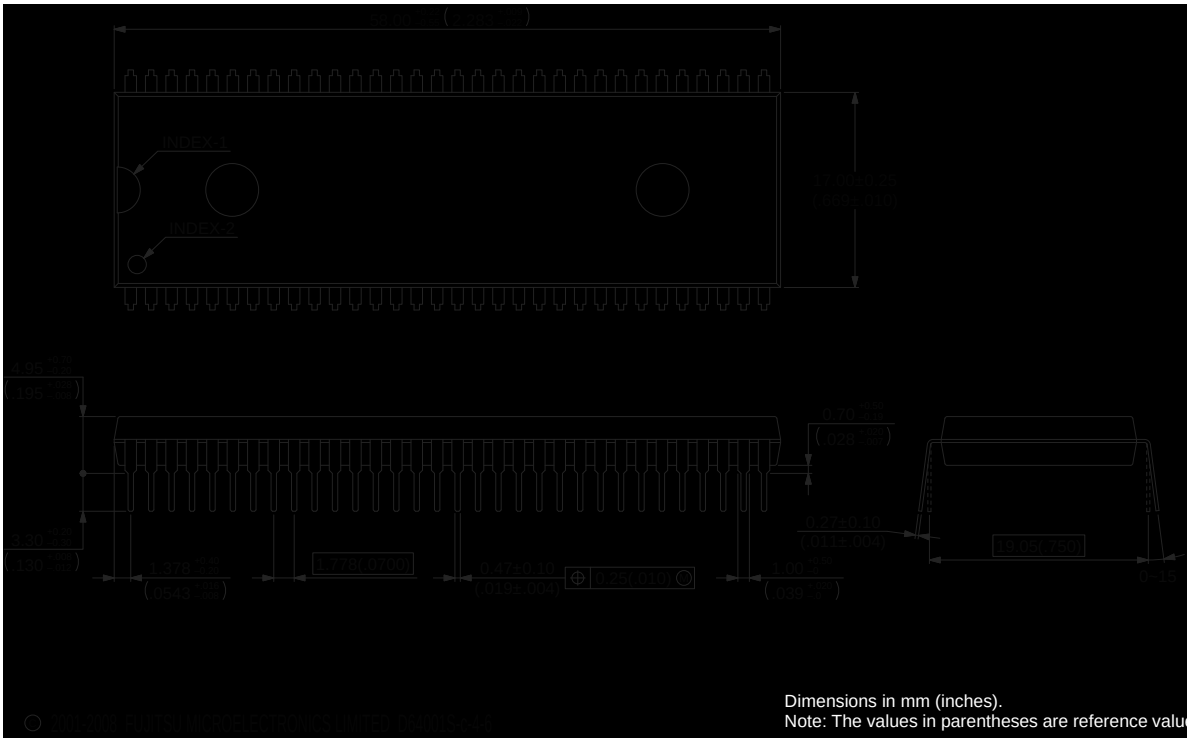
No.	Part number	MB89635R MB89636R MB89637R	MB89P637	MB89PV630
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors 〈 P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Selectable by pin	Can be set per pin*	Fixed to “without pull-up resistor”
2	Power-on reset selection 〈 With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to “with power-on reset”
3	Selection of the main clock oscillation stabilization time (at 10 MHz) 〈 $2^{18}/F_{CH}$ (Approx. 26.2 ms) $2^{17}/F_{CH}$ (Approx. 13.1 ms) $2^{14}/F_{CH}$ (Approx. 1.6 ms) $2^{4}/F_{CH}$ (Approx. 1.6 µs) F_{CH} : Main clock frequency	Selectable	Setting possible	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)
4	Reset pin output 〈 Reset output provided No reset output	Selectable	Setting possible	Fixed to “with reset output”
5	Single/dual-clock system option 〈 Single clock Dual clock	Selectable	Setting possible	MB89PV630-101 Single-clock system MB89PV630-102 Dual-clock systems

* : For P50 to P53, fixed to "Without pull-up resistor."

■ PACKAGE DIMENSIONS



(DIP-64P-M01)



Dimensions in mm (inches).
Note: The values in parentheses are reference valu

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

(Continued)

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
49	■ MASK OPTIONS	Changed the explanation for "*" in "■ MASK OPTIONS".

The vertical lines marked in the left side of the page show the changes.

MEMO