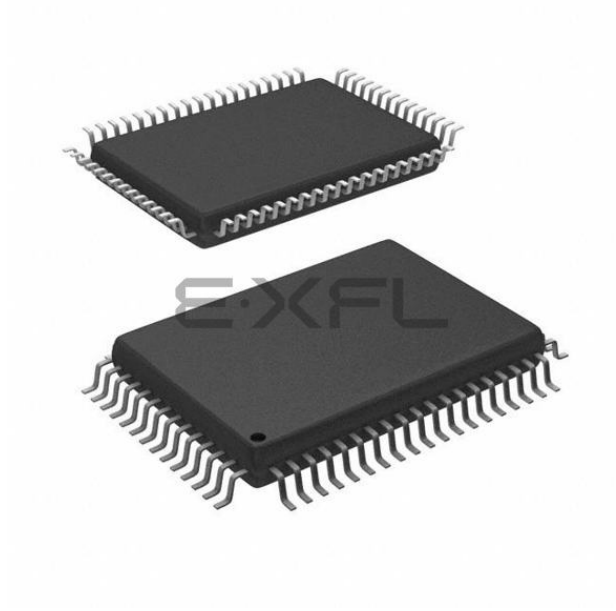
Infineon Technologies - MB89635RPF-G-1460 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1460

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12531-4E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89630R Series

MB89635R/636R/637R/P637/PV630

■ OUTLINE

The MB89630R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

* : F²MC is the abbreviation for Fujitsu Flexible Microcontroller.

■ FEATURES

- High-speed operating capability at low voltage
- Minimum execution time: 0.4 µs@3.5 V, 0.8 µs@2.7 V
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Five types of timers
  8-bit PWM timer: 2 channels (Also usable as a reload timer)
  8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
  16-bit timer/counter
  21-bit timebase timer

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2009.5

(Continued)

- UART
  CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  Start by an external input capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Bus interface function
  With hold and ready function

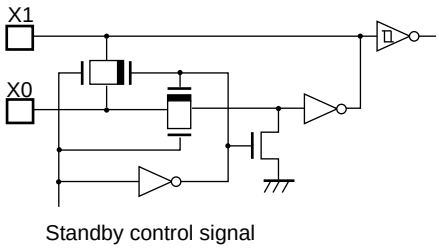
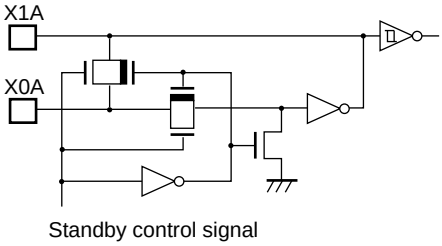
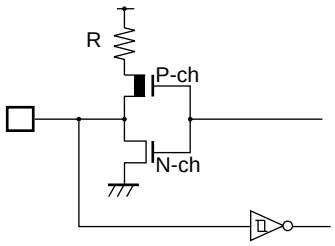
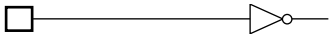
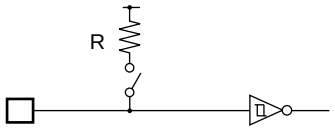
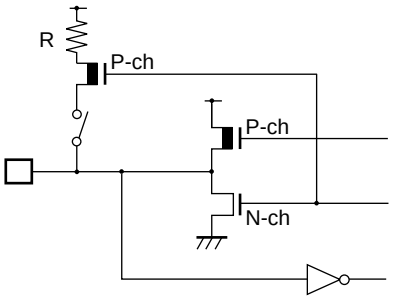
- Other specifications
  Both MB89630 series and MB89635R/636R/637R is the same.
- Electrical specifications/electrical characteristics
  Electrical specifications of the MB89635R/636R/637R series are the same as that of the MB89630 series.
  Electrical characteristics of both the series are much the same.

■ CORRESPONDENCE BETWEEN THE MB89630 AND MB89630R SERIES

- The MB89630R series is the reduction version of the MB89630 series.
- The the MB89630 and MB89630R series consist of the following products:

MB89630 series	MB89635	MB89636	MB89637	MB89P637	MB89PV630
MB89630R series	MB89635R	MB89636R	MB89637R		

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) External clock input selection versions of MB89PV630, MB89P637, MB89635R, MB89636R, and MB89637R At an oscillation feedback resistor of approximately 1 MΩ@5.0 V
B		• Crystal or ceramic oscillation type (subclock) MB89PV630, MB89P637, MB89635R, MB89636R, and MB89637R with dual-clock system At an oscillation feedback resistor of approximately 4.5 MΩ@5.0 V
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ@5.0 V • Hysteresis input
D		
E		• Hysteresis input • Pull-up resistor optional (except P70 and P71)
F		• CMOS output • CMOS input • Pull-up resistor optional (except P22 and P23)

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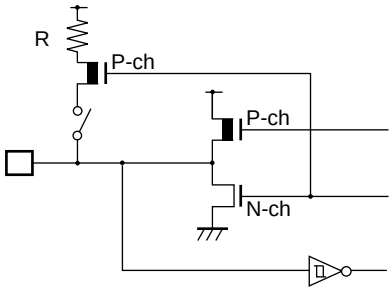
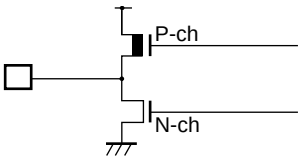
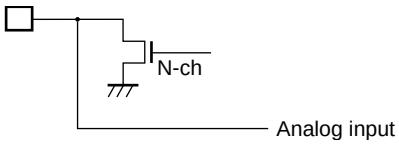
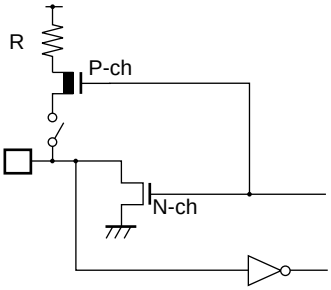
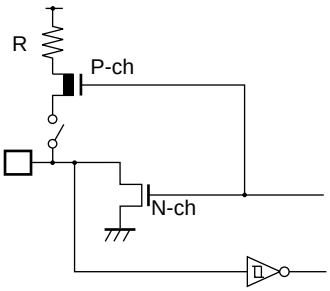
Type	Circuit	Remarks
G		• CMOS output • Hysteresis input • Pull-up resistor optional
H		CMOS output
I		Analog input
J		• CMOS input • Pull-up resistor optional
K		• Hysteresis input • Pull-up resistor optional

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

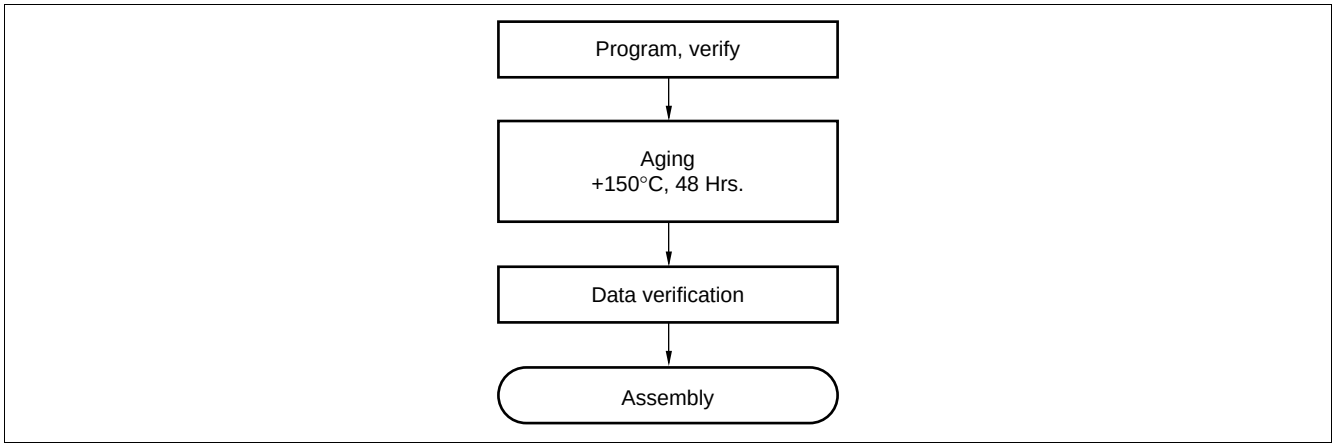
(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$. (Note that addresses 8000_H to $FFFF_H$ in the operating mode assign to 0000_H to $7FFF_H$ in EPROM mode).

(3) Load option data into addresses 0000_H to 0006_H of the EPROM programmer.
(For information about each corresponding option, see “8. OTPROM Option Bit Map”.)

(4) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

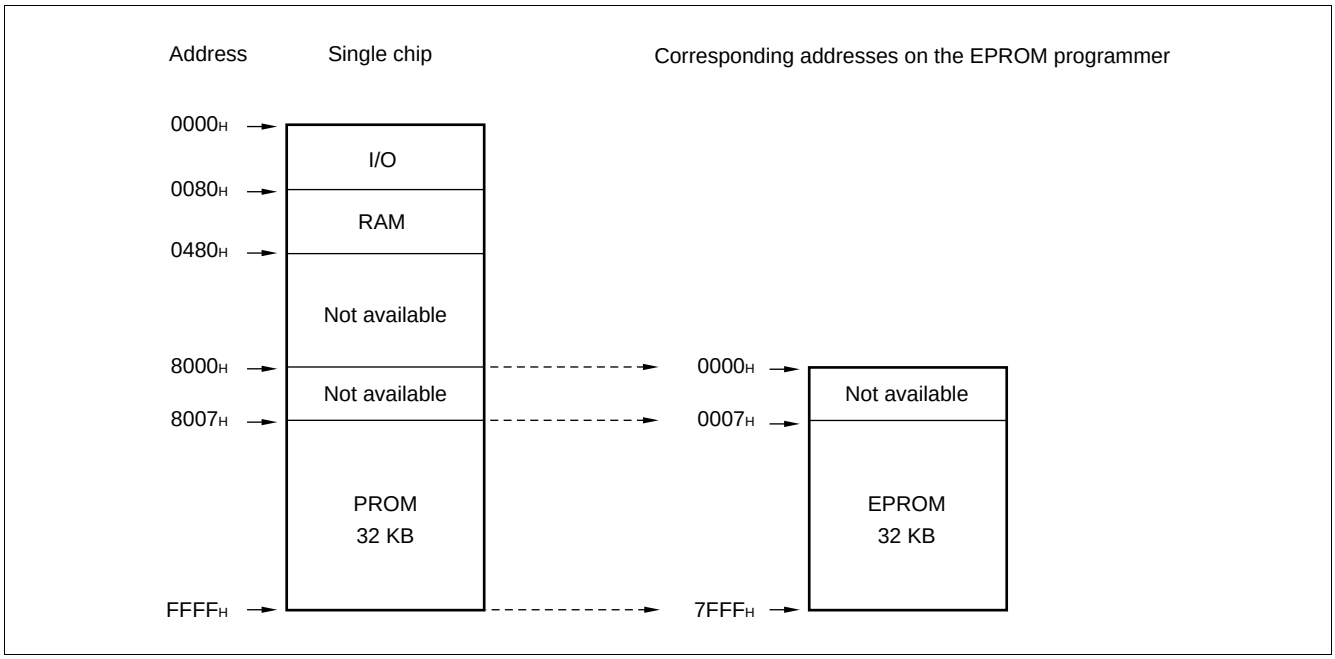
■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20CZ, MBM27C256A-20TV

2. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

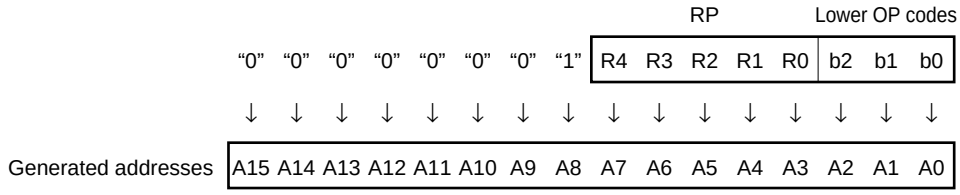
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• Rule for conversion of actual addresses of the general-purpose register area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

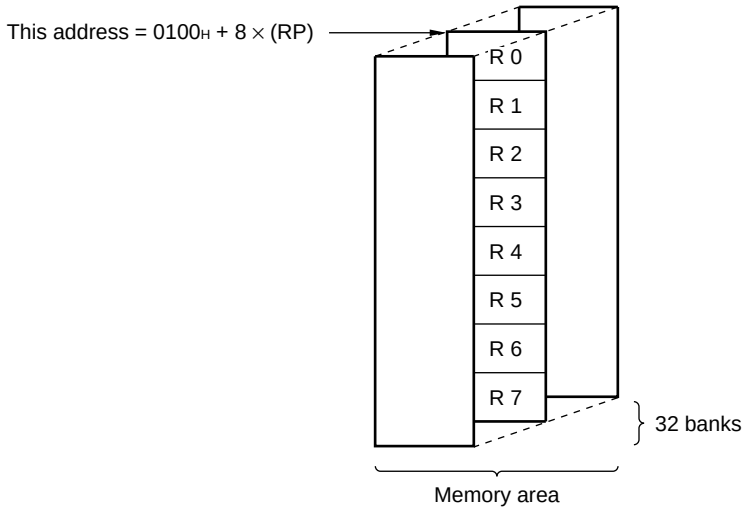
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).

• Register bank configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus pin control register
06H	Vacancy		
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	System clock control register
09H	(R/W)	WDTE	Watchdog timer control register
0AH	(R/W)	TBCR	Timebase timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	CHG3	Port 3 switching register
0DH	(R/W)	PDR3	Port 3 data register
0EH	(W)	DDR3	Port 3 data direction register
0FH	(R/W)	PDR4	Port 4 data register
10H	(W)	DDR4	Port 4 data direction register
11H	(R/W)	BUZR	Buzzer register
12H	(R/W)	PDR5	Port 5 data register
13H	(R/W)	PDR6	Port 6 data register
14H	(R)	PDR7	Port 7 data register
15H	(R/W)	PCR1	PWC pulse width control register 1
16H	(R/W)	PCR2	PWC pulse width control register 2
17H	(R/W)	RLBR	PWC reload buffer register
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH	Vacancy		
1CH	(R/W)	SMR1	Serial mode register
1DH	(R/W)	SDR1	Serial data register
1EH	Vacancy		
1FH	Vacancy		

(Continued)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89635R/ 636R/637R/ PV630
				—	1.5	2.5	mA	MB89P637
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89635R/ 636R/637R/ PV630
				—	500	700	µA	MB89P637
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	

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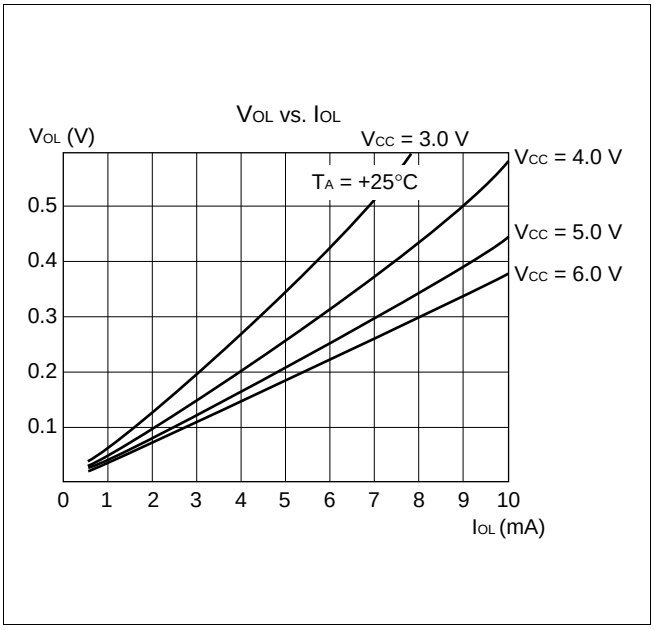
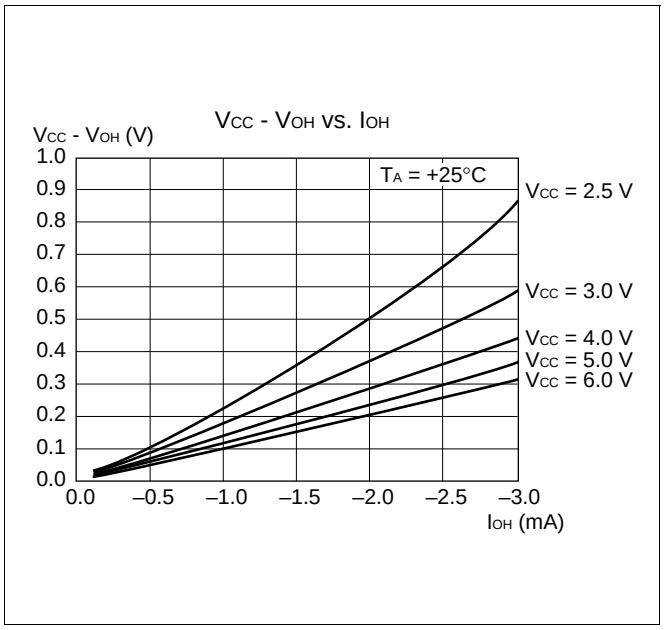
■ CHARACTERISTICS EXAMPLE

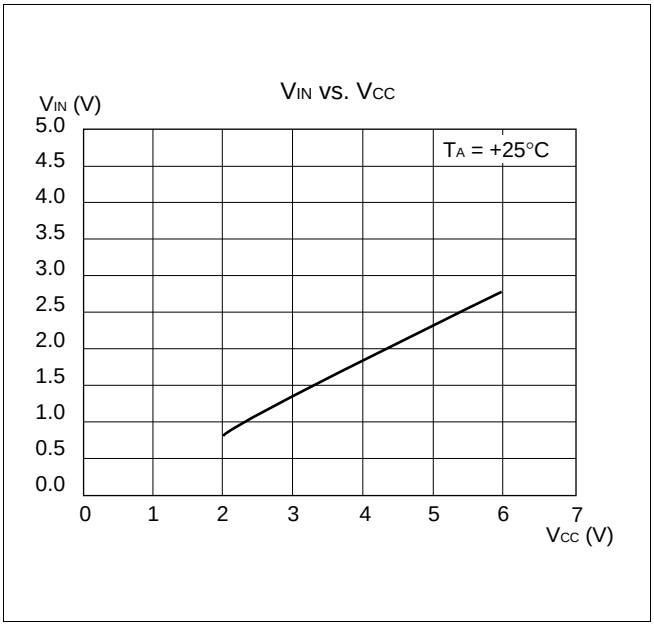
(1) “L” Level Output Voltage



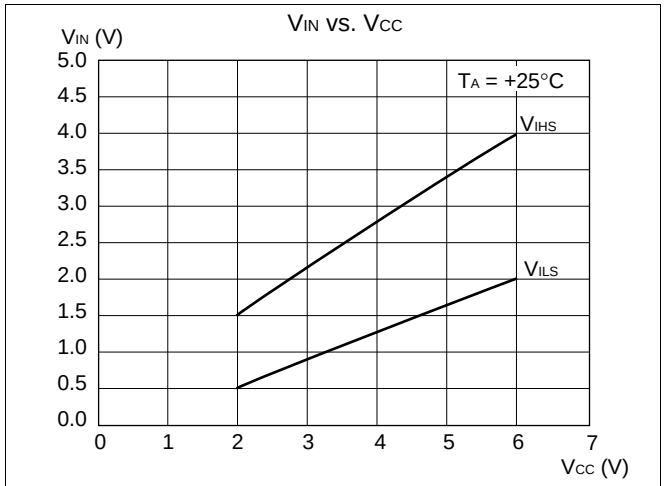
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

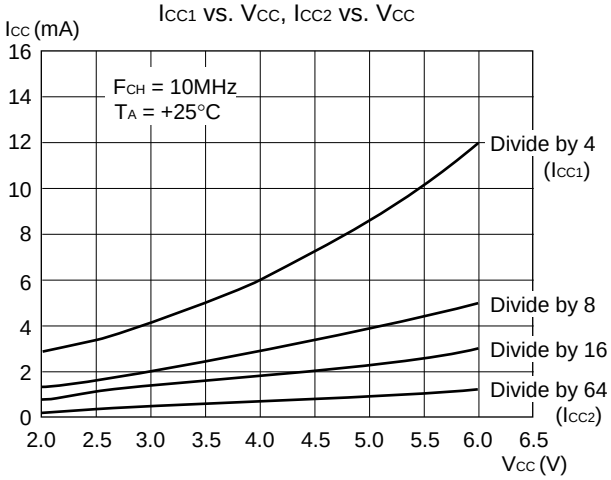


V_{IHS}: Threshold as the input voltage in hysteresis characteristics is set to “H” level

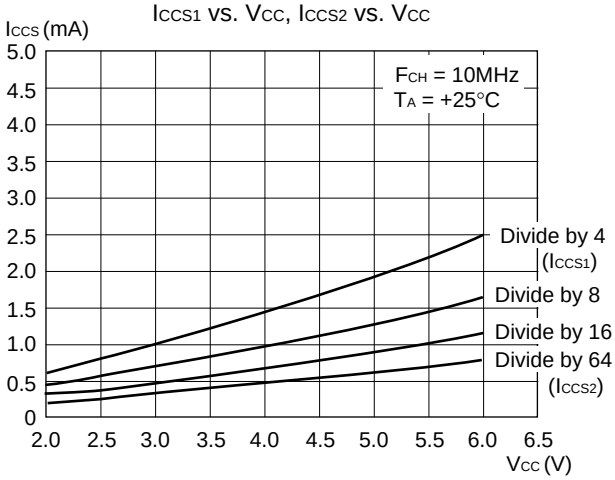
V_{ILS}: Threshold as the input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)

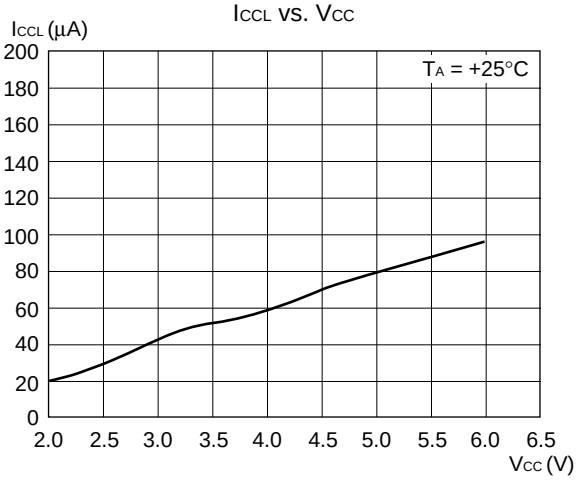
I_{CC1} vs. V_{CC}, I_{CC2} vs. V_{CC}



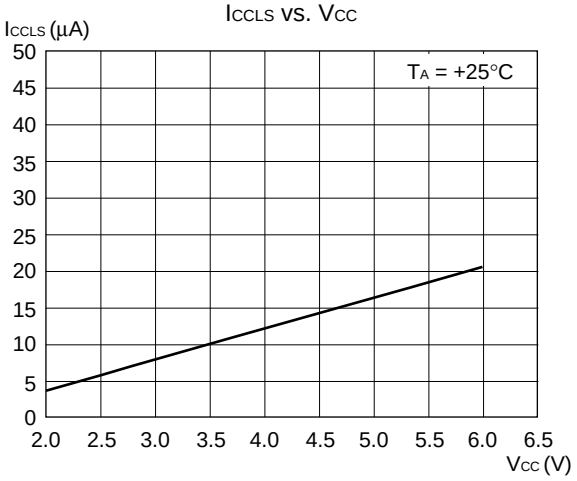
I_{CCS1} vs. V_{CC}, I_{CCS2} vs. V_{CC}



I_{CCL} vs. V_{CC}



I_{CCLS} vs. V_{CC}



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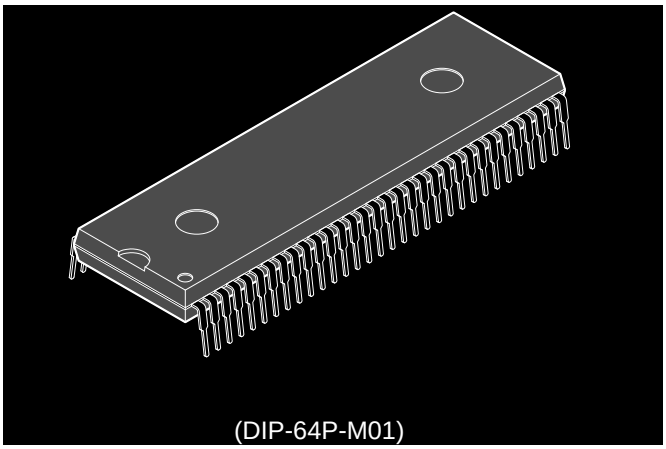
■ MASK OPTIONS

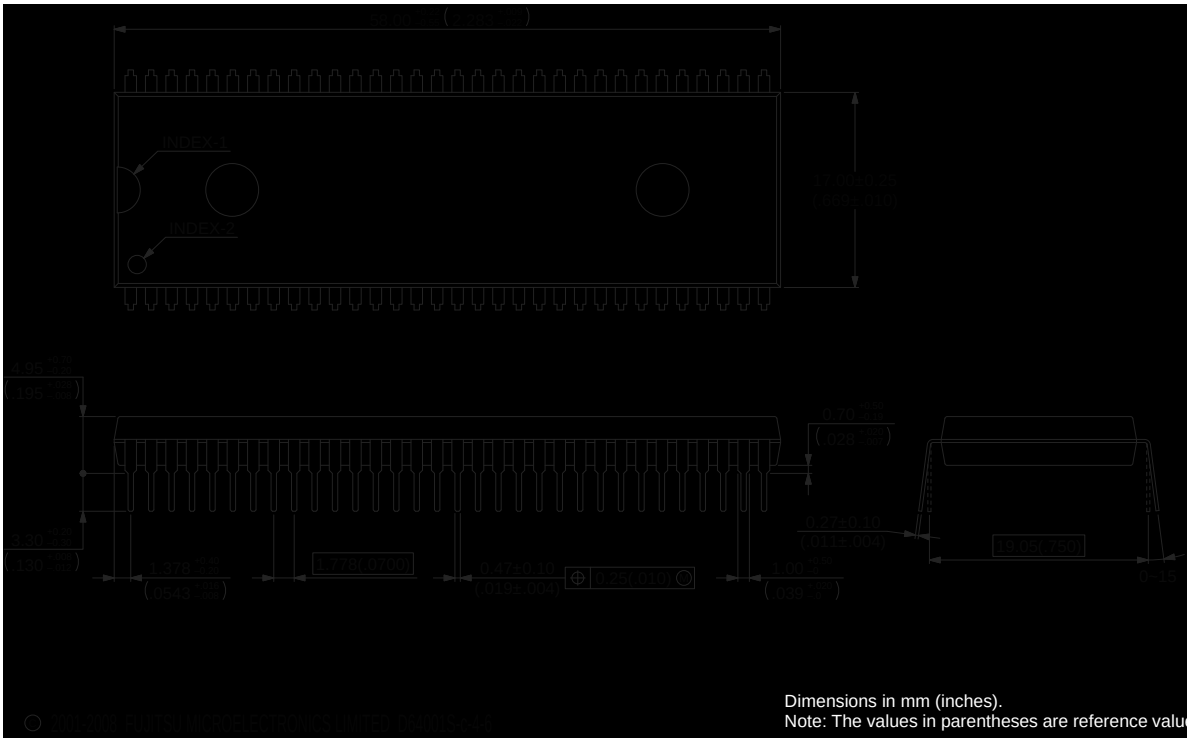
No.	Part number	MB89635R MB89636R MB89637R	MB89P637	MB89PV630
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors 〈 P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Selectable by pin	Can be set per pin*	Fixed to “without pull-up resistor”
2	Power-on reset selection 〈 With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to “with power-on reset”
3	Selection of the main clock oscillation stabilization time (at 10 MHz) 〈 $2^{18}/F_{CH}$ (Approx. 26.2 ms) $2^{17}/F_{CH}$ (Approx. 13.1 ms) $2^{14}/F_{CH}$ (Approx. 1.6 ms) $2^{4}/F_{CH}$ (Approx. 1.6 µs) F_{CH} : Main clock frequency	Selectable	Setting possible	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)
4	Reset pin output 〈 Reset output provided No reset output	Selectable	Setting possible	Fixed to “with reset output”
5	Single/dual-clock system option 〈 Single clock Dual clock	Selectable	Setting possible	MB89PV630-101 Single-clock system MB89PV630-102 Dual-clock systems

* : For P50 to P53, fixed to "Without pull-up resistor."

■ PACKAGE DIMENSIONS



(DIP-64P-M01)



Dimensions in mm (inches).
Note: The values in parentheses are reference valu

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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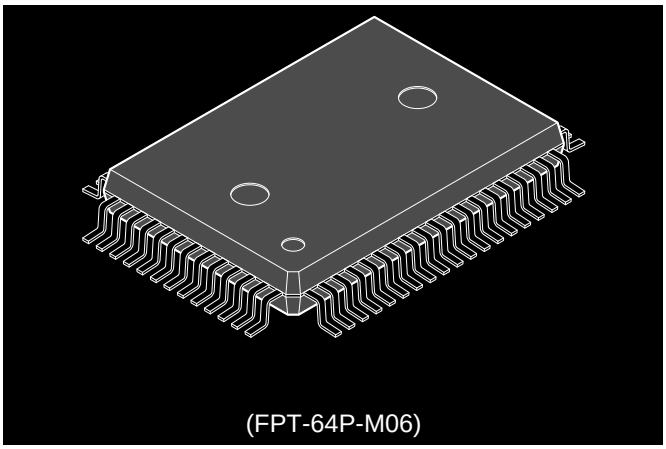
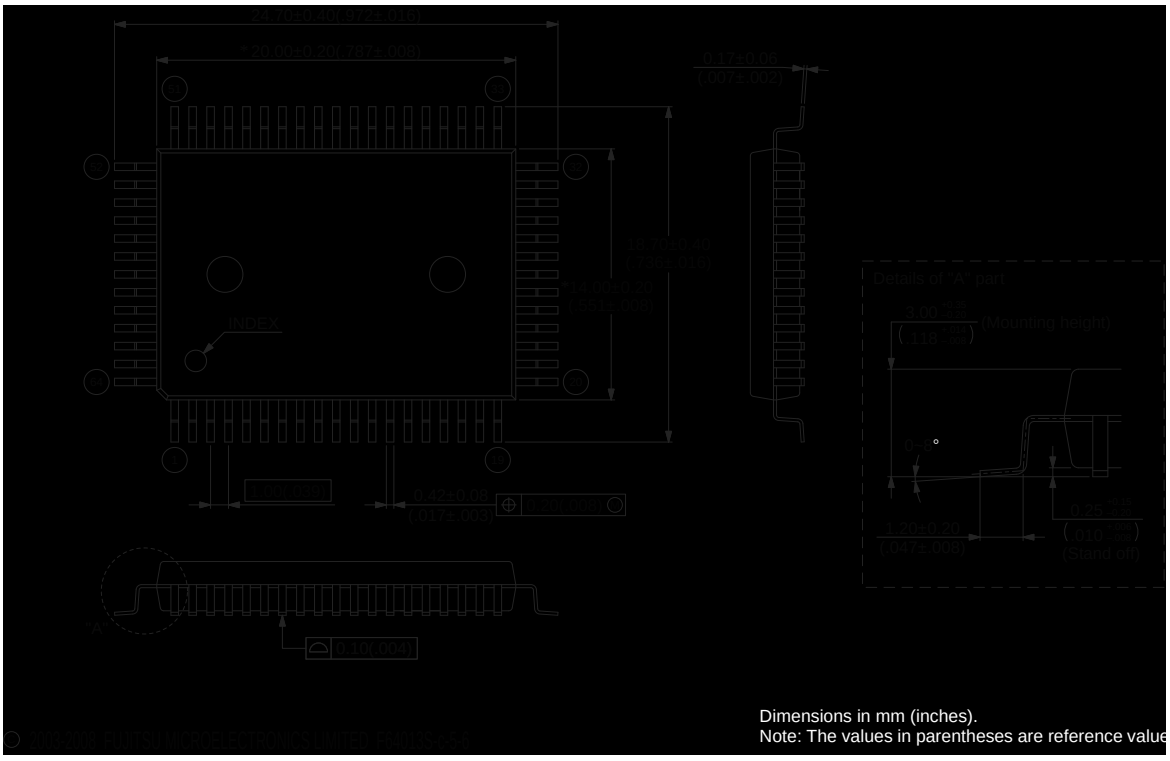


(FPT-64P-M06)



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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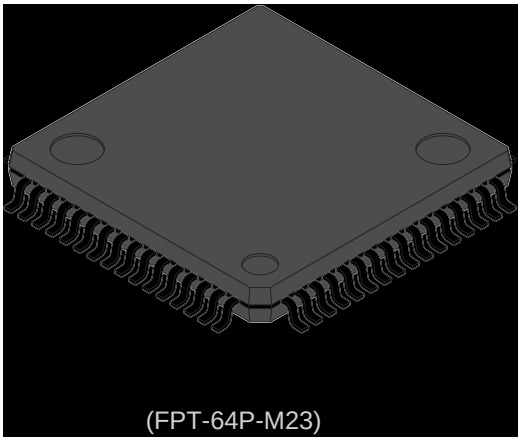
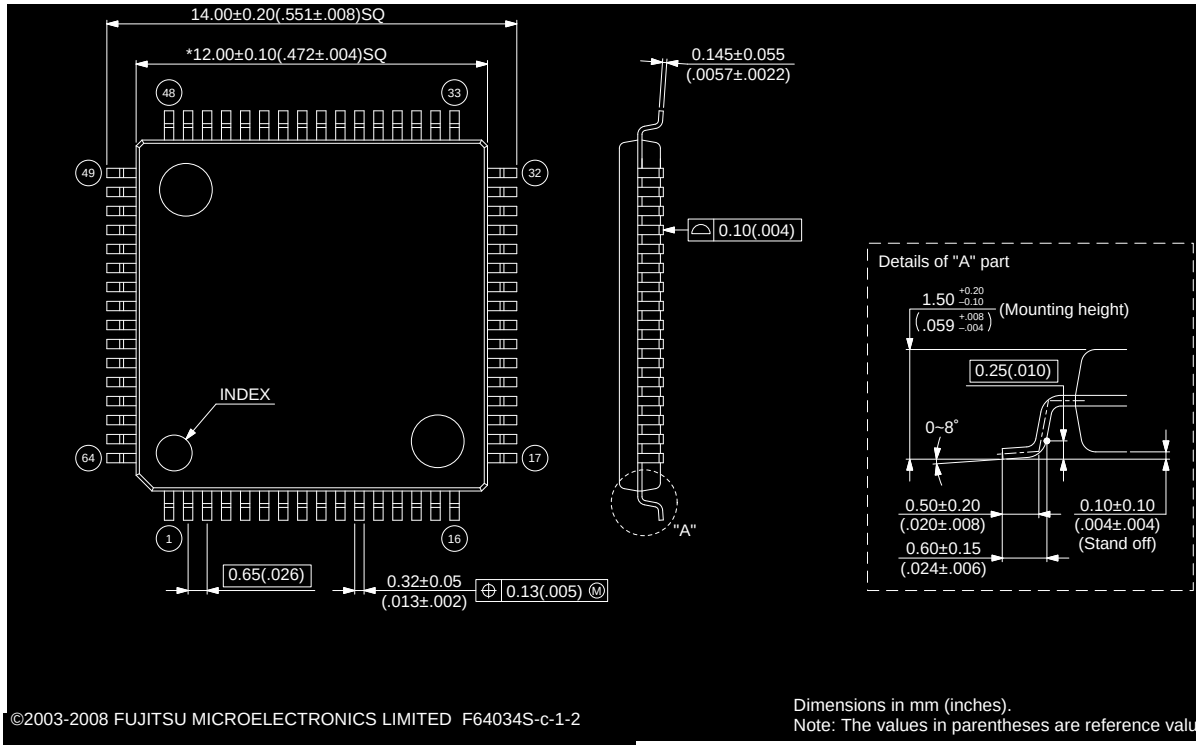


(FPT-64P-M23)



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FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3329
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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