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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	F ² MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1461

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89630R Series

MB89635R/636R/637R/P637/PV630

The MB89630R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

* : F²MC is the abbreviation for Fujitsu Flexible Microcontroller.

■ FEATURES

- · High-speed operating capability at low voltage
- Minimum execution time: 0.4 $\mu s@3.5$ V, 0.8 $\mu s@2.7$ V
- F²MC-8L family CPU core

Instruction set optimized for controllers

Multiplication and division instructions 16-bit arithmetic operations Test and branch instructions Bit manipulation instructions, etc.

Five types of timers
8-bit PWM timer: 2 channels (Also usable as a reload timer)
8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
16-bit timer/counter
21-bit timebase timer

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/



■ PRODUCT LINEUP

Part number								
Item	MB89635R	MB89636R	MB89637R	MB89P637	MB89PV630			
Classification		ass-produced produ mask ROM product	One-time PROM product	Piggyback/ evaluation product (for evaluation and development)				
ROM size	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	nal mask (internal mask		32 K × 8 bits (external ROM)			
RAM size	512×8 bits	768 × 8 bits	1024 × 8 bits	1024×8 bits	1024×8 bits			
CPU functions	Instruction bit le Instruction lengt Data bit length: Minimum execu	The number of instruction ns:136Instruction bit length:8 bitsInstruction length:1 to 3 bytes						
Ports	Input ports: Output ports (N- I/O ports (N-ch o Output ports (C I/O ports (CMO Total:	as peripherals.) as peripherals.) as peripherals.) as bus control.) o serve as bus pins	and peripherals.)					
Watch timer		21 bits \times 1 (in m	ain clock)/15 bits \times	1 (at 32.768 kHz)				
8-bit PWM timer		8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 μs to 3.3 ms) × 2 channels 7/8-bit resolution PWM operation (conversion cycle: 51.2 μs to 839 ms) × 2 channels						
8-bit pulse width count timer	 8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 μs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 μs) 8-bit pulse width measurement operation (capable of continuous measurement, and measurement of "H" pulse width/ "L" pulse width/ from ↑ to ↑/from ↓ to ↓) 							
16-bit timer/ counter	16-bit timer operation (operating clock cycle: 0.4 μs) 16-bit event counter operation (rising edge/falling edge/both edge selectable)							
8-bit serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs)							
UART		Capable of switching two I/O systems by software Transfer data length (6, 7, and 8 bits) Transfer rate (300 to 62500 bps. at 10 MHz oscillation)						
10-bit A/D converter	Capable	A/D conversio Sense m	it resolution × 8 cha n mode (conversior ode (conversion tim ation by an external	n time: 13.2 μs)	ernal timer			

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(Continued)

Part number Item			35R MB89636R MB89637R MB89P637						
External interrupt input		4 independent channels (edge selection, interrupt vector, source flag). Rising edge/falling edge selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)							
Standby mode	Sleep mode, stop mode, watch mode, and subclock mode								
Process	CMOS								
Operating voltage*	2.2 V to 6.0 V 2.7 V to 6.0 V								
EPROM for use	EPROM for use								

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.") In the case of the MB89PV630, the voltage varies with the restrictions of the EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89635R	MB89636R MB89637R		
DIP-64P-M01	0	0	0	×
FPT-64P-M06	0	0	0	×
FPT-64P-M23	0	0	×	×
MQP-64C-P01	×	×	×	0
MDP-64C-P02	×	×	×	0

 \bigcirc : Available \times : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ PIN DESCRIPTION

	Pin no.			a :	
SH-DIP ^{*1} MDIP ^{*2}	QFP2 ^{*3}	QFP1 ^{*4} MQFP ^{*5}	Pin name	Circuit type	Function
30	22	23	X0	А	Main clock crystal oscillator pins
31	23	24	X1		
28	20	21	MOD0	D	Operating mode selection pins
29	21	22	MOD1		Connect directly to Vcc or Vss.
27	19	20	RST	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
56 to 49	48 to 41	49 to 42	P00/AD0 to P07/AD7	F	General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.
48 to 41	40 to 33	41 to 34	P10/A08 to P17/A157	F	General-purpose I/O ports When an external bus is used, these ports function as an upper address output.
40	32	33	P20/BUFC	Н	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	31	32	P21/HAK	Н	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.
38	30	31	P22/HRQ	F	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	29	30	P23/RDY	F	General-purpose output port When an external bus is used, this port functions as a ready input.
36	28	29	P24/CLK	Н	General-purpose output port When an external bus is used, this port functions as a clock output.
35	27	28	P25/WR	Н	General-purpose output port When an external bus is used, this port functions as a write signal output.
34	26	27	P26/RD	Н	General-purpose output port When an external bus is used, this port functions as a read signal output.

*1: DIP-64P-M01

*2: MDP-64C-P02 *3: FPT-64P-M23 *4: FPT-64P-M06 *5: MQP-M64C-P01 (Continued)

DS07-12531-4E

■ I/O CIRCUIT TYPE

Туре	Circuit	Remarks
A	X1 X0 X0 X0 X0 X0 X0 X0 X0 X0 X0	 Crystal or ceramic oscillation type (main clock) External clock input selection versions of MB89PV630, MB89P637, MB89635R, MB89636R, and MB89637R At an oscillation feedback resistor of approximately 1 MΩ@5.0 V
В	X1A X0A X0A T X0 X0 X0 X0 X0 X0 X0 X0 X0 X0	 Crystal or ceramic oscillation type (subclock) MB89PV630, MB89P637, MB89635R, MB89636R, and MB89637R with dual-clock system At an oscillation feedback resistor of approximately 4.5 MΩ@5.0 V
C	R P-ch N-ch 7/7	 At an output pull-up resistor (P-ch) of approximately 50 kΩ@5.0 V Hysteresis input
D		
E		 Hysteresis input Pull-up resistor optional (except P70 and P71)
F	R P-ch P-ch N-ch N-ch	 CMOS output CMOS input Pull-up resistor optional (except P22 and P23)

(Continued)

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than Vcc or lower than Vss is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between Vcc and Vss.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AVcc and AVR) and analog input from exceeding the digital power supply (Vcc) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AVcc = DAVC = Vcc and AVss = AVR = Vss even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

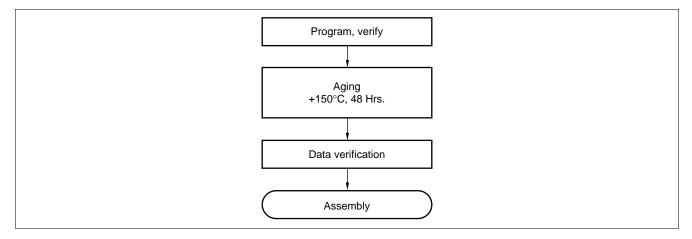
When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.

• Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007^H to 7FFF^H. (Note that addresses 8000^H to FFFF^H in the operating mode assign to 0000^H to 7FFF^H in EPROM mode).
- (3) Load option data into addresses 0000H to 0006H of the EPROM programmer. (For information about each corresponding option, see "8. OTPROM Option Bit Map".)
- (4) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

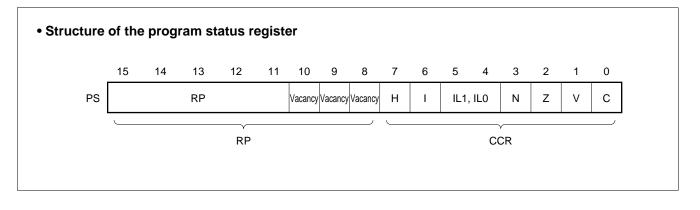
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A16-bit register for index modification
Extra pointer (EP):	A16-bit pointer for indicating a memory address
Stack pointer (SP):	A16-bit register for indicating a stack area
Program status (PS):	A16-bit register for storing a register pointer, a condition code

◄ 16 bits	Initial value
PC	: Program counter FFFDH
A	: Accumulator Indeterminate
Т	: Temporary accumulator Indeterminate
IX	: Index register Indeterminate
EP	: Extra pointer Indeterminate
SP	: Stack pointer Indeterminate
PS	: Program status I-flag = 0, IL1, IL0 = 11 The other bit values are indeterminate

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AVss = Vss = 0.0 V)

Devenetor	Symbol	Va	lue	Unit	Remarks
Parameter	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	Vcc	Vss-0.3	Vss + 7.0	V	*
rower supply voltage	AVcc	Vss-0.3	Vss + 7.0	V	*
A/D converter reference input voltage	AVR	Vss-0.3	Vss + 7.0	V	AVR must not exceed "AVcc + 0.3 V".
	Vı	Vss-0.3	Vcc + 0.3	V	Except P50 to P53
Input voltage	Vı2	Vss-0.3	Vss + 7.0	V	P50 to P53
Output voltage	Vo	Vss-0.3	Vcc + 0.3	V	Except P50 to P53
Output voltage	V ₀₂	Vss-0.3	Vss + 7.0	V	P50 to P53
"L" level maximum output current	Iol		20	mA	
"L" level average output current	IOLAV		4	mA	Average value (operating current \times operating rate)
"L" level total maximum output current	ΣΙοι		100	mA	
"L" level total average output current	ΣΙοιαν		40	mA	Average value (operating current \times operating rate)
"H" level maximum output current	Іон		-20	mA	
"H" level average output current	Іонач		-4	mA	Average value (operating current \times operating rate)
"H" level total maximum output current	ΣІон		-50	mA	
"H" level total average output current	ΣΙοήαν		-20	mA	Average value (operating current × operating rate)
Power consumption	PD		500	mW	
Operating temperature	TA	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

 * : Use AVcc and Vcc set at the same voltage.

Take care so that AV $_{CC}$ does not exceed V $_{CC}$, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

3. DC Characteristics

			(AVcc = Vcc = 5.0 V, AVss = Vss = 0.0					= −40°C to +85°C)
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
i arameter	Cymbol	r in name	Condition	Min.	Тур.	Max.	0	Remarks
	VIH1	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53		0.7 Vcc	_	Vcc + 0.3	V	P51 to P53 with pull-up resistor
"H" level input	VIH2	P51 to P53		0.7 Vcc		Vss + 6.0	V	Without pull-up resistor
voltage V⊮	Viнs	RST, MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42,P50, P72 to P74		0.8 Vcc	_	Vcc + 0.3	V	P50 with pull-up resistor
	VIHS2	P50, P70, P71		0.8 Vcc		Vss + 6.0	V	Without pull-up resistor
	VIL	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43		Vss-0.3		0.3 Vcc	V	
"L" level input voltage	Vils	P30, P32, P33, P35, P36, P40, P42, P50 to P53, <u>P70</u> to P74, RST, MOD0, MOD1		Vss-0.3		0.2 Vcc	V	
Open-drain output pin application voltage	Vd	P50 to P53	-	Vss-0.3	_	Vss + 6.0	V	
"H" level output voltage	Vон	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43	Іон = -2.0 mA	4.0			V	
"L" level output voltage	Vol	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, P50 to P53, P60 to P67, RST	lo∟= 4.0 mA			0.4	V	
Input leakage current (Hi-z output leakage current)	lu	P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1	0.0 V < Vı < Vcc		_	±5	μΑ	Without pull-up resistor

 $(AV_{CC} = V_{CC} = 5.0 \text{ V}, \text{ AV}_{SS} = V_{SS} = 0.0 \text{ V}, \text{ T}_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C})$

(Continued)

MB89630R Series

(Continued)

 $(AVcc = Vcc = 5.0 \text{ V}, \text{ AVss} = Vss = 0.0 \text{ V}, \text{ T}_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C})$

Parameter	Symbol	Pin name	Condition		Value		Unit	Remarks
Farameter	Symbol	Finnanie	Condition	Min.	Тур.	Max.	Unit	Nemarks
Power supply current ^{*1}	la		$F_{CH} = 10 \text{ MHz},$ when A/D conversion operates.	_	6		mA	
	Іан	AVcc	$F_{CH} = 10 \text{ MHz},$ $T_A = +25^{\circ}C,$ when A/D conversion in a stop.	_		1	μΑ	
Input capacitance	CIN	Other than AVcc, AVss, Vcc, and Vss	f = 1 MHz	_	10		pF	

*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not counted.

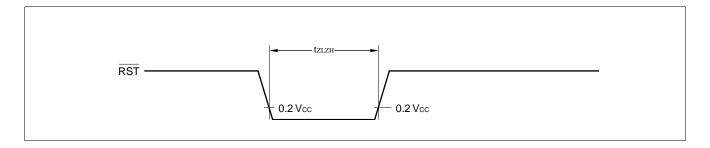
*2: For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics".

4. AC Characteristics

(1) Reset Timing

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = \text{V}_{SS} = 0.0 \text{ V}, \text{ } T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C})$

Parameter	Svmbol	Condition	ndition Value Min. Max.		Unit	Remarks
Farameter	Symbol	Condition				
RST "L" pulse width	t zlzh		48 t нсү∟		ns	



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	tinst	4/Fсн, 8/Fсн, 16/Fсн, 64/Fсн	μs	(4/F _{CH}) t _{inst} = 0.4 μ s, operating at F _{CH} = 10 MHz
		2/FcL	μs	$t_{inst} = 61.036 \ \mu s$, operating at $F_{CL} = 32.768 \ kHz$

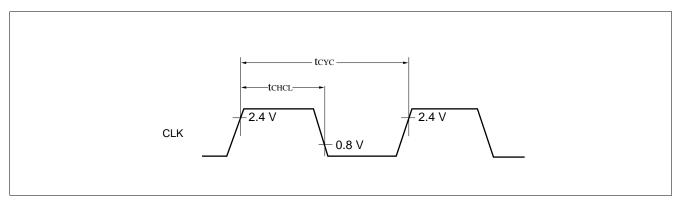
Note: Operating at 10 MHz, the cycle varies with the set execution time.

(5) Clock Output Timing

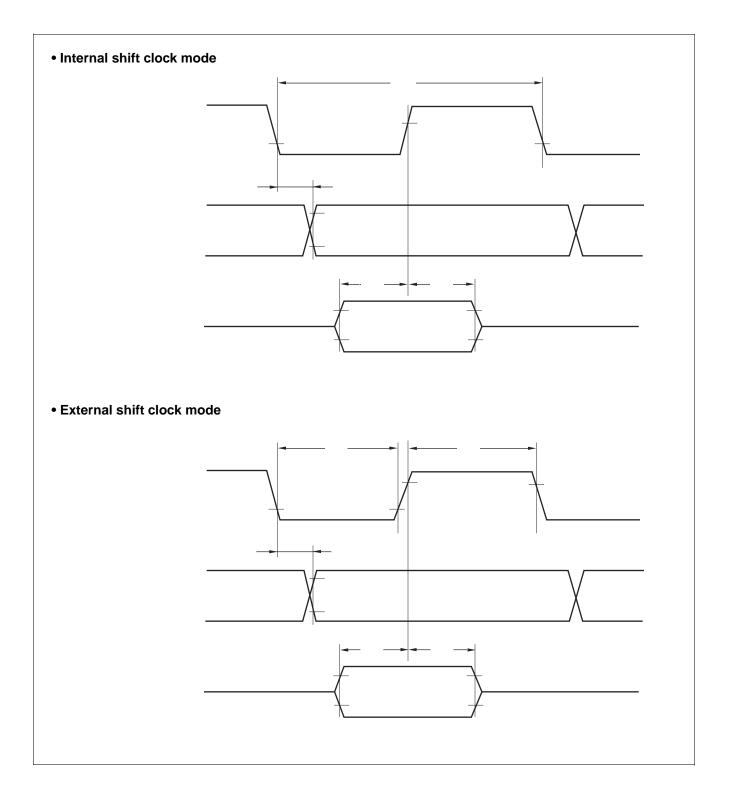
 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = \text{V}_{SS} = 0.0 \text{ V}, \text{ T}_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C})$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.	Unit	itemaiks
Cycle time	tcyc	CLK		1/2 tinst*	—	μs	
$CLK \uparrow \to CLK \downarrow$	t CHCL	CLK		1/4 t _{inst} * – 70 ns	1/4 t _{inst} *	μs	

* : For information on tinst, see "(4) Instruction Cycle".



MB89630R Series



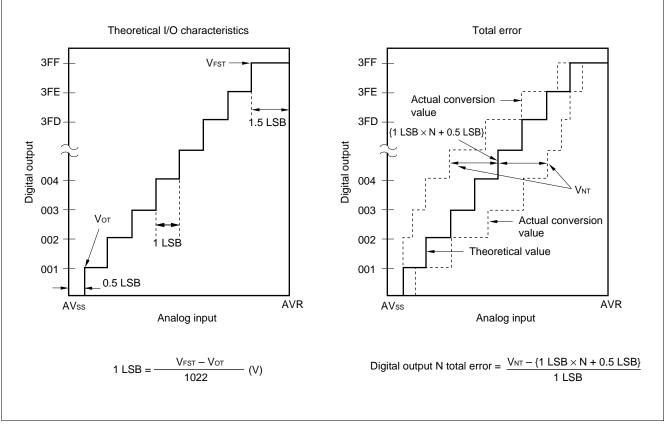
6. A/D Converter Glossary

Resolution

Analog changes that are identifiable with the A/D converter

- Linearity error
 The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with
 the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics
 - Differential linearity error The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
 - Total error (unit: LSB)

The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise

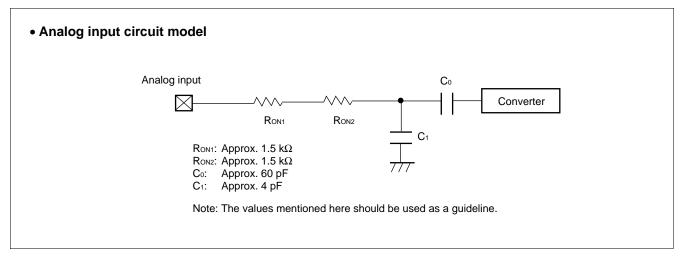


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7. Notes on Using A/D Converter

· Input impedance of the analog input pins

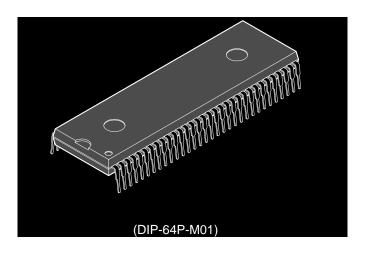
The output impedance of the external circuit for the analog input must satisfy the following conditions. If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 μ s at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 k Ω .

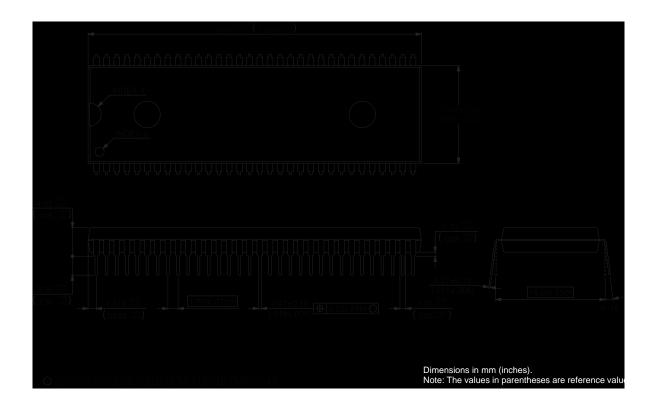


• Error

The smaller the | AVR-AVss |, the greater the error would become relatively.

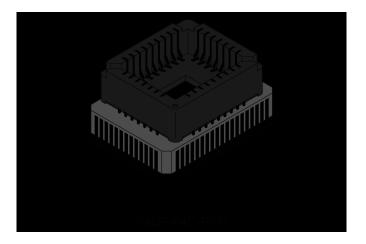
■ PACKAGE DIMENSIONS

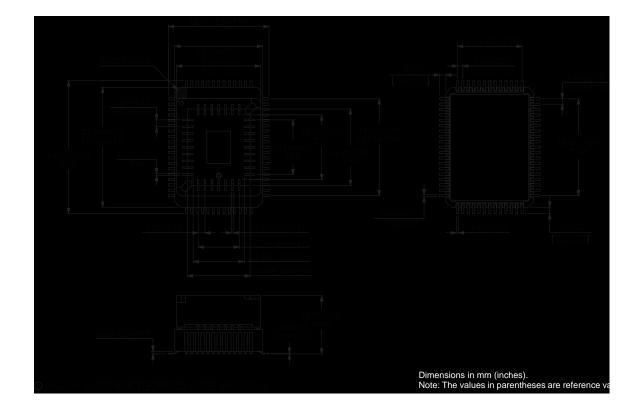




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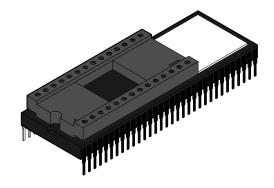


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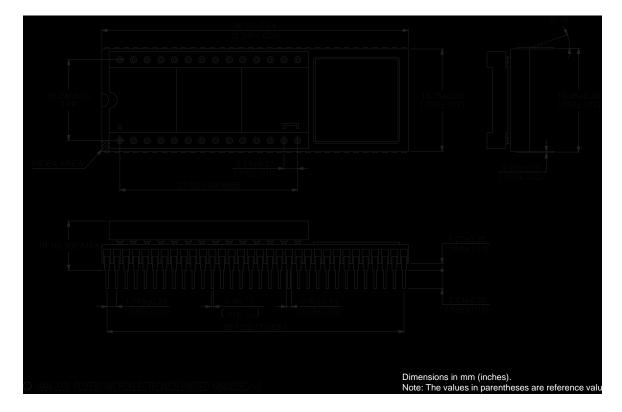
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(MDP-64C-P02)



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MB89630R Series

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
49	■ MASK OPTIONS	Changed the explanation for "*" in "■ MASK OPTIONS".

The vertical lines marked in the left side of the page show the changes.

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