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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F ² MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1470e1

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Part number	MB89635R	MB89636R	MB89637R	MB89P637	MB89PV630			
External interrupt input		4 independent channels (edge selection, interrupt vector, source flag). Rising edge/falling edge selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)						
Standby mode		Sleep mode, stop mode, watch mode, and subclock mode						
Process		CMOS						
Operating voltage*	2.2 V to 6.0 V 2.7 V to 6.0 V							
EPROM for use		MBM27C256A-20CZ MBM27C256A-20TV						

^{* :} Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.") In the case of the MB89PV630, the voltage varies with the restrictions of the EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89635R	MB89636R MB89637R	MB89P637	MB89PV630
DIP-64P-M01	0	0	0	×
FPT-64P-M06	0	0	0	×
FPT-64P-M23	0	0	×	×
MQP-64C-P01	×	×	×	0
MDP-64C-P02	×	×	×	0

^{○ :} Available ×: Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

• On the MB89P637, the program area starts from address 8007_H but on the MB89PV630 and MB89637R starts from 8000_H.

(On the MB89P637, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637R, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637.)

- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume
 more current than the product with a mask ROM. However, the current consumption in sleep/stop modes is
 the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics".)

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options".

Take particular care on the following points:

- A pull-up resistor cannot be set for P50 to P53 on the MB89P637.
- Options are fixed on the MB89PV630.

4. Differences between the MB89630 and MB89630R Series

· Memory access area

There are no difference between the access area of MB89635/MB89635R, and that of MB89637/MB89637R. The access area of MB89636 is different from that of the MB89636R when using in external bus mode.

Address	Memory area				
Address	MB89636	MB89636R			
0000н to 007Fн	I/O area	I/O area			
0080н to 037Fн	RAM area	RAM area			
0380н to 047Fн		Access prohibited			
0480н to 7FFFн	External area	External area			
8000н to 9FFFн		Access prohibited			
A000н to FFFFн	ROM area	ROM area			

	Pin no.		Cinquit		
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5	Pin name	Circuit type	Function
33	25	26	P27/ALE	Н	General-purpose output port When an external bus is used, this port functions as an address latch signal output.
2	58	59	P30/UCK1	G	General-purpose I/O port Also serves as the clock I/O 1 for the UART. This port is a hysteresis input type.
1	57	58	P31/UO1	F	General-purpose I/O port Also serves as the data output 1 for the UART.
63	55	56	P32/UI1	G	General-purpose I/O port Also serves as the data input 1 for the UART. This port is a hysteresis input type.
62	54	55	P33/SCK1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
61	53	54	P34/SO1	F	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O.
60	52	53	P35/SI1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
59	51	52	P36/PWC	G	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type.
58	50	51	P37/WTO	F	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter.
6	62	63	P40/UCK2	G	General-purpose I/O port Also serves as the clock I/O 2 for the UART. This port is a hysteresis input type.
5	61	62	P41/UO2	F	General-purpose I/O port Also serves as the data output 2 for the UART.
4	60	61	P42/UI2	G	General-purpose I/O port Also serves as the data input 2 for the UART. This port is a hysteresis input type.
3	59	60	P43/PTO1	F	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer.
10	2	3	P50/ADST	К	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.

*1: DIP-64P-M01 *2: MDP-64C-P02 *3: FPT-64P-M23

*4: FPT-64P-M06 *5: MQP-M64C-P01

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• External EPROM pins (MB89PV630 only)

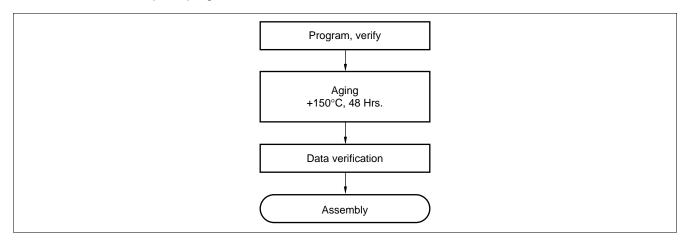
Pin	no.	B:		-	
MDIP	MQFP	Pin name	I/O	Function	
65	66	V _{PP}	0	"H" level output pin	
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	0	Address output pins	
75 76 77	77 78 79	O1 O2 O3	I	Data input pins	
78	80	Vss	0	Power supply (GND) pin	
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins	
84	87	CE	0	ROM chip enable pin Outputs "H" during standby.	
85	88	A10	0	Address output pin	
86	89	ŌĒ	0	ROM output enable pin Outputs "L" at all times.	
87 88 89	91 92 93	A11 A9 A8	0	Address output pins	
90	94	A13	0		
91	95	A14	0		
92	96	Vcc	0	EPROM power supply pin	
_	65 76 81 90	N.C.	_	Internally connected pins Be sure to leave them open.	

• Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007_H to 7FFF_H. (Note that addresses 8000_H to FFFF_H in the operating mode assign to 0000_H to 7FFF_H in EPROM mode).
- (3) Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see "8. OTPROM Option Bit Map".)
- (4) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

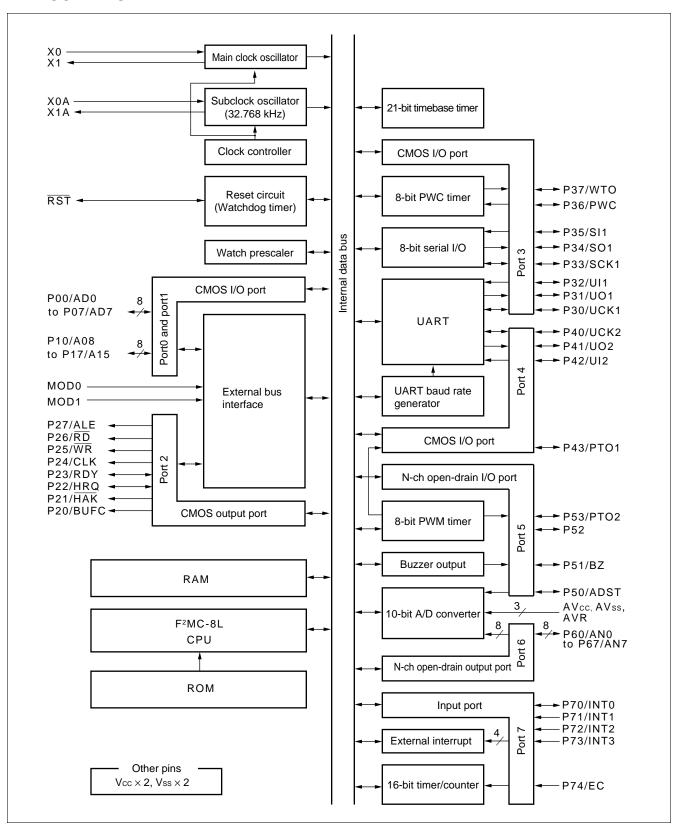
All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. OTPROM Option Bit Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000н	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single/dual- clock system 1: Dual clock 0: Single clock	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	11:2 ¹⁸ /Fc	bilization (/Fсн) н 01:2 ¹⁷ /Fсн н 00:2 ⁴ /Fсн
0001н	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002н	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0003н	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0004н	Vacancy Readable and writable	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes			
0005н	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	Vacancy Readable and writable	Vacancy Readable and writable
0006н	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Reserved bit Readable and writable			

Note: Each bit is set to '1' as the initialized value.

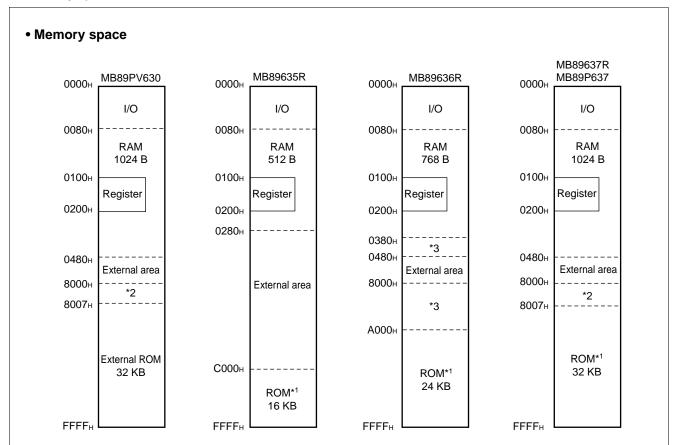
■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

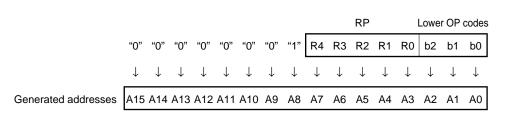
The microcontrollers of the MB89630R series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89630R series is structured as illustrated below.



- *1: The ROM area is an external area depending on the mode.
- *2: Addresses 8000н to 8006н for the MB89P637 comprise an option area, do not use this area for the MB89PV630 and MB89637R.
- *3: The access is forbidden in the external bus mode.

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• Rule for conversion of actual addresses of the general-purpose register area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1	l	†
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

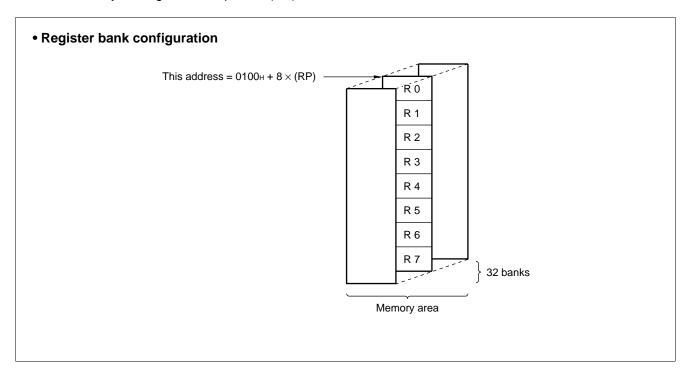
V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).



2. Recommended Operating Conditions

(AVss = Vss = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
Farameter	Symbol	Min.	Max	Onit	Nemarks
	Vcc	2.2*	6.0*	V	Normal operation assurance range* MB89635R/636R/637R
Power supply voltage	VCC	2.7*	6.0*	V	Normal operation assurance range* MB89PV630/P637
	AVcc	1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	3.0	AVcc	V	
Operating temperature	TA	-40	+85	°C	

^{*:} These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics".

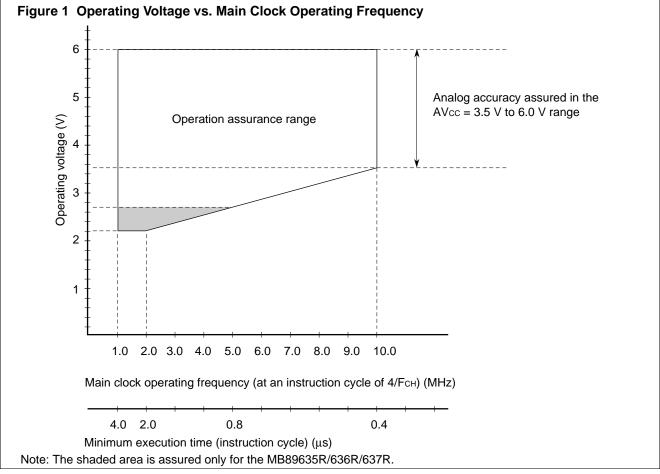


Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/FcH. Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	4	4/Fсн, 8/Fсн, 16/Fсн, 64/Fсн	μs	(4/F _{CH}) t _{inst} = 0.4 μs, operating at F _{CH} = 10 MHz
	L inst	2/FcL	μs	t _{inst} = 61.036 μs, operating at FcL = 32.768 kHz

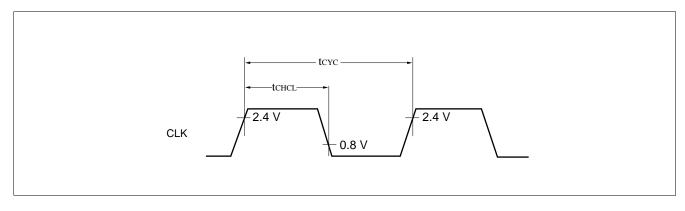
Note: Operating at 10 MHz, the cycle varies with the set execution time.

(5) Clock Output Timing

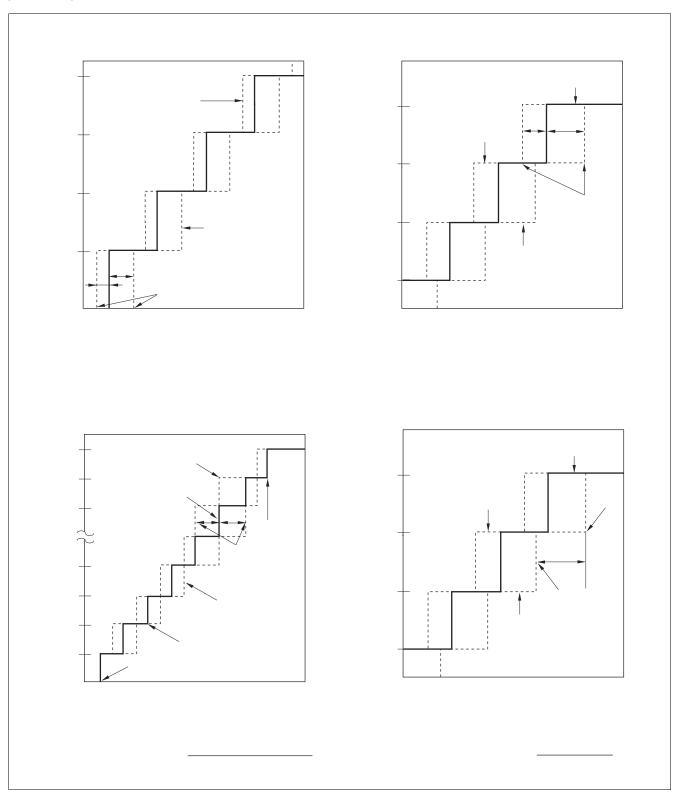
 $(Vcc = 5.0 V\pm 10\%, AVss = Vss = 0.0 V, T_A = -40^{\circ}C to +85^{\circ}C)$

Parameter	Symbol Pin		Condition	Va	Unit	Remarks	
Parameter	Symbol	name	Condition	Min.	Max.	Oilit	Remarks
Cycle time	tcyc	CLK		1/2 t _{inst} *	_	μs	
$CLK \uparrow \rightarrow CLK \downarrow$	tchcl	CLK	_	1/4 t _{inst} * - 70 ns	1/4 t _{inst} *	μs	

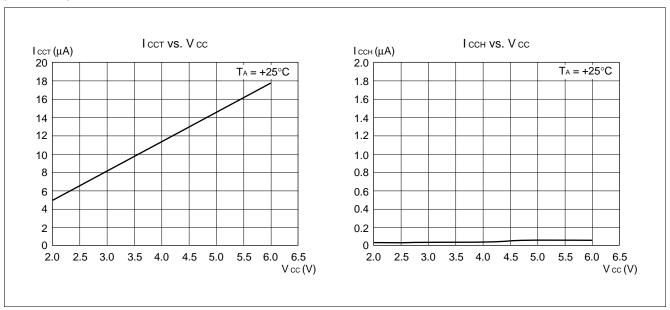
*: For information on tinst, see "(4) Instruction Cycle".



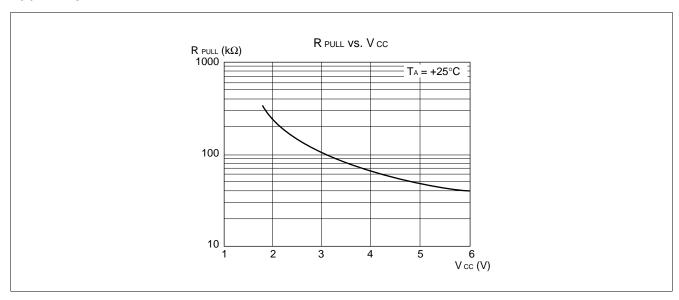
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(6) Pull-up Resistance

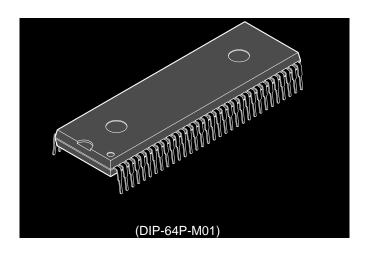


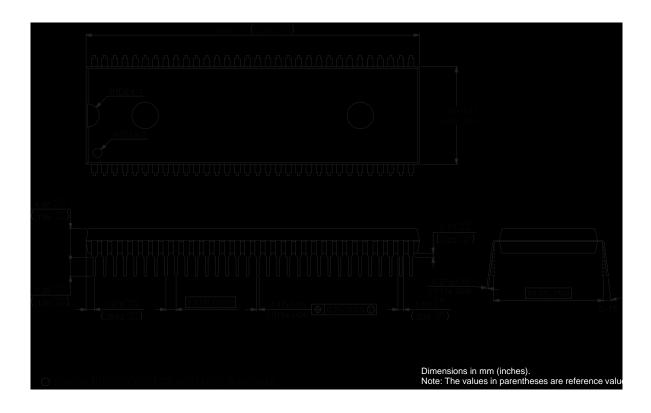
■ MASK OPTIONS

No.	Part number	MB89635R MB89636R MB89637R	MB89P637	MB89PV630
NO.	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Selectable by pin	Can be set per pin*	Fixed to "without pull-up resistor"
2	Power-on reset Selection With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to "with power-on reset"
3	Selection of the main clock oscillation stabilization time (at 10 MHz) 218/FcH (Approx. 26.2 ms) 217/FcH (Approx. 13.1 ms) 214/FcH (Approx. 1.6 ms) 24/FcH (Approx. 1.6 μs) FcH: Main clock frequency	Selectable	Setting possible	Fixed to 2 ¹⁸ /F _{CH} (Approx. 26.2 ms)
4	Reset pin output Reset output provided No reset output	Selectable	Setting possible	Fixed to "with reset output"
5	Single/dual-clock system option Single clock Dual clock	Selectable	Setting possible	MB89PV630-101 Single-clock system MB89PV630-102 Dual-clock systems

^{*:} For P50 to P53, fixed to "Without pull-up resistor."

■ PACKAGE DIMENSIONS

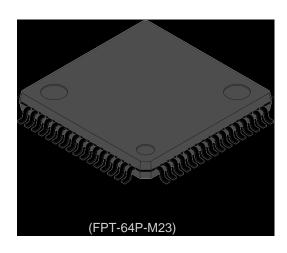


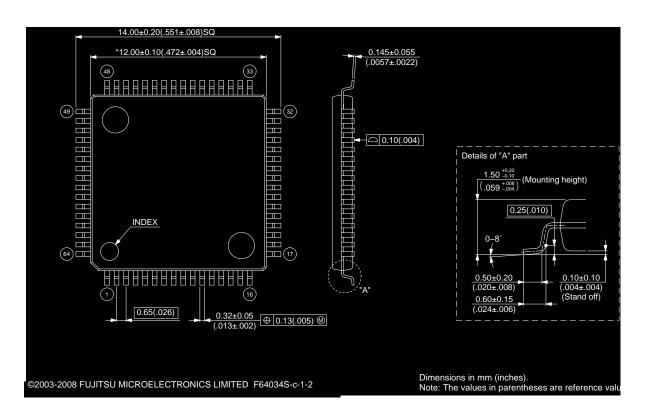


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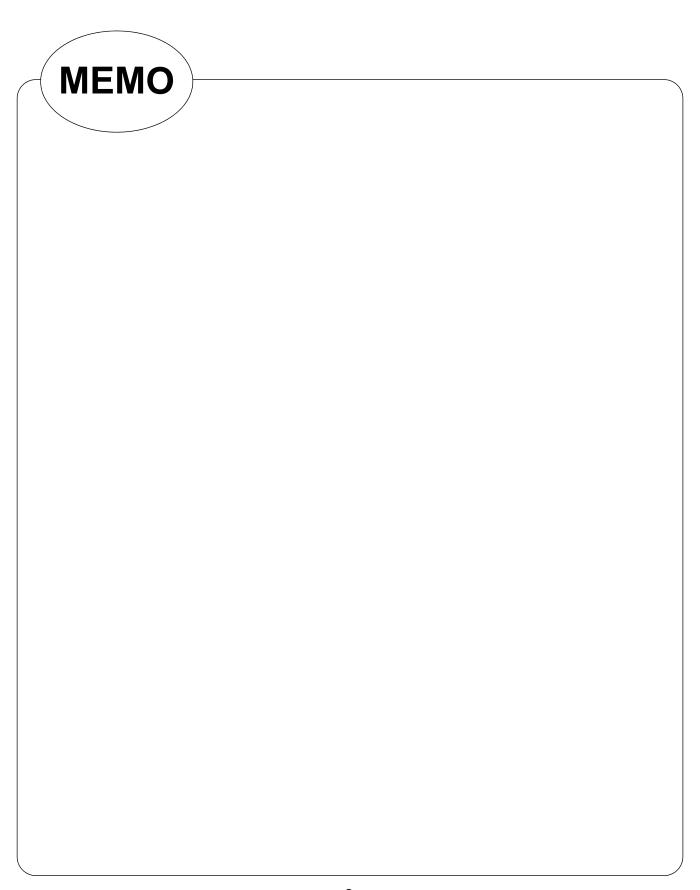


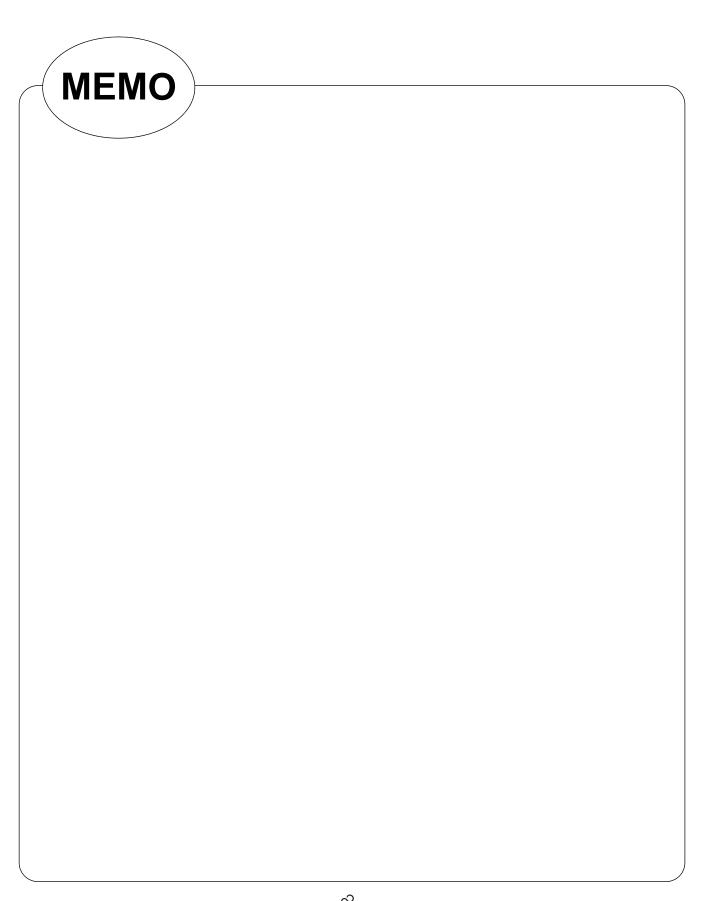


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FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0722, Japan

Tel: +81-3-5322-3329 http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC. 1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH Pittlerstrasse 47, 63225 Langen, Germany Tel: +49-6103-690-0 Fax: +49-6103-690-122 http://emea.fujitsu.com/microelectronics/

Korea

FUJITSU MICROELECTRONICS KOREA LTD. 206 Kosmo Tower Building, 1002 Daechi-Dong, Gangnam-Gu, Seoul 135-280, Republic of Korea Tel: +82-2-3484-7100 Fax: +82-2-3484-7111 http://kr.fujitsu.com/fmk/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD. 151 Lorong Chuan, #05-08 New Tech Park 556741 Singapore Tel: +65-6281-0770 Fax: +65-6281-0220 http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD. Rm. 3102, Bund Center, No.222 Yan An Road (E), Shanghai 200002, China Tel: +86-21-6146-3688 Fax: +86-21-6335-1605 http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD. 10/F., World Commerce Centre, 11 Canton Road, Tsimshatsui, Kowloon, Hong Kong

Tel: +852-2377-0226 Fax: +852-2376-3269

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