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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1480e1

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# 8-bit Proprietary Microcontroller

# CMOS

# F<sup>2</sup>MC-8L MB89630R Series

# MB89635R/636R/637R/P637/PV630

# 

The MB89630R series has been developed as a general-purpose version of the F<sup>2</sup>MC\*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

\* : F<sup>2</sup>MC is the abbreviation for Fujitsu Flexible Microcontroller.

# ■ FEATURES

- · High-speed operating capability at low voltage
- Minimum execution time: 0.4  $\mu s@3.5$  V, 0.8  $\mu s@2.7$  V
- F<sup>2</sup>MC-8L family CPU core

Instruction set optimized for controllers

Multiplication and division instructions 16-bit arithmetic operations Test and branch instructions Bit manipulation instructions, etc.

Five types of timers
8-bit PWM timer: 2 channels (Also usable as a reload timer)
8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
16-bit timer/counter
21-bit timebase timer

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/



## (Continued)

- UART
  - CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter Start by an external input capable
- External interrupt: 4 channels Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
   Stop mode (Oscillation stops to minimize the current consumption.)
   Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
   Subclock mode
   Watch mode
- Bus interface function With hold and ready function

# ■ PRODUCT LINEUP

Part number Item	MB89635R	MB89636R	MB89637R	MB89P637	MB89PV630		
Classification	M: (i	ass-produced produ mask ROM product	One-time PROM product	Piggyback/ evaluation product (for evaluation and development)			
ROM size	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	$32 \text{ K} \times 8 \text{ bits}$ (Internal PROM, to be programmed with general- purpose EPROM programmer)	32 K × 8 bits (external ROM)		
RAM size	$512 \times 8$ bits	768 × 8 bits	1024 × 8 bits	$1024 \times 8$ bits	$1024 \times 8$ bits		
CPU functions	The number of i Instruction bit le Instruction lengt Data bit length: Minimum execu Interrupt proces	nstructionns: ngth: h: tion time: sing time:	136 8 bits 1 to 3 bytes 1, 8, 16 bits 0.4 μs/10 MHz, 0 3.6 to 57.6 μs/10	61 μs@32.768 kHz ) MHz, 562.5 μs@3	2.768 kHz		
Ports	Input ports:5 (All alsoOutput ports (N-ch open-drain):8 (All alsoI/O ports (N-ch open-drain):4 (All alsoOutput ports (CMOS):8 (All alsoI/O ports (CMOS):28 (27 pcTotal:53			o serve as peripherals.) o serve as peripherals.) o serve as peripherals.) o serve as bus control.) orts also serve as bus pins and peripherals.)			
Watch timer		21 bits $\times$ 1 (in matrix	ain clock)/15 bits $\times$	1 (at 32.768 kHz)			
8-bit PWM timer	8-bit reload timer of 7/8-bit resolu	operation (toggled o channels ition PWM operation	utput capable, oper n (conversion cycle:	ating clock cycle: 0. 51.2 μs to 839 ms)	4 $\mu$ s to 3.3 ms) $\times$ 2 $\times$ 2 channels		
8-bit pulse width count timer	8-bit timer o 8-bit reload tim 8-bit pulse w mea	peration (overflow o er operation (toggle ridth measurement o surement of "H" put	utput capable, oper d output capable, o operation (capable o se width/ "L" pulse v	ating clock cycle: 0. perating clock cycle of continuous meas width/ from ↑ to ↑/fro	4 to 12.8 μs) : 0.4 to 12.8 μs) urement, and om ↓ to ↓)		
16-bit timer/ counter	16-bit eve	16-bit timer ope ent counter operatio	ration (operating clo on (rising edge/fallin	ock cycle: 0.4 μs) g edge/both edge s	electable)		
8-bit serial I/O	(one ex	8 bits LSB first/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks; 0.8 us, 3.2 us, 12.8 us)					
UART		Capable of swi Transfer Transfer rate (300	tching two I/O syste data length (6, 7, a 0 to 62500 bps. at 1	ems by software nd 8 bits) 0 MHz oscillation)			
10-bit A/D converter	Capable	10-b A/D conversio Sense m of continuous activa	it resolution × 8 cha n mode (conversior ode (conversion tim ation by an external	nnels h time: 13.2 μs) he: 7.2 μs) activation or an inte	rnal timer		

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# ■ DIFFERENCES AMONG PRODUCTS

# 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

• On the MB89P637, the program area starts from address 8007<sup>H</sup> but on the MB89PV630 and MB89637R starts from 8000<sup>H</sup>.

(On the MB89P637, addresses 8000<sup>H</sup> to 8006<sup>H</sup> comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637R, addresses 8000<sup>H</sup> to 8006<sup>H</sup> could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637.)

- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

# 2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.

## 3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options".

Take particular care on the following points:

- A pull-up resistor cannot be set for P50 to P53 on the MB89P637.
- Options are fixed on the MB89PV630.

## 4. Differences between the MB89630 and MB89630R Series

Memory access area

There are no difference between the access area of MB89635/MB89635R, and that of MB89637/MB89637R. The access area of MB89636 is different from that of the MB89636R when using in external bus mode.

Addross	Memory area				
Address	MB89636	MB89636R			
0000н to 007Fн	I/O area	I/O area			
0080н to 037Fн	RAM area	RAM area			
0380н to 047Fн		Access prohibited			
0480н to 7FFFн	External area	External area			
8000н to 9FFFн		Access prohibited			
A000н to FFFFн	ROM area	ROM area			



## • Pin assignment on package top (MB89PV630 only)

Pin no.	Pin name						
65	N.C.	73	A2	81	N.C.	89	OE
66	Vpp	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	07	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	CE	95	A14
72	A3	80	Vss	88	A10	96	Vcc

N.C.: Internally connected. Do not use.

# ■ PIN DESCRIPTION

Pin no.				Circuit				
SH-DIP <sup>*1</sup> MDIP <sup>*2</sup>	QFP2 <sup>*3</sup>	QFP1 <sup>*4</sup> MQFP <sup>*5</sup>	Pin name	type	Function			
30	22	23	X0	Α	Main clock crystal oscillator pins			
31	23	24	X1					
28	20	21	MOD0	D	Operating mode selection pins			
29	21	22	MOD1		Connect directly to Vcc or Vss.			
27	19	20	RST	С	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".			
56 to 49	48 to 41	49 to 42	P00/AD0 to P07/AD7	F	General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.			
48 to 41	40 to 33	41 to 34	P10/A08 to P17/A157	F	General-purpose I/O ports When an external bus is used, these ports function as an upper address output.			
40	32	33	P20/BUFC	Н	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.			
39	31	32	P21/HAK	Н	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.			
38	30	31	P22/HRQ	F	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.			
37	29	30	P23/RDY	F	General-purpose output port When an external bus is used, this port functions as a ready input.			
36	28	29	P24/CLK	Н	General-purpose output port When an external bus is used, this port functions as a clock output.			
35	27	28	P25/WR	Н	General-purpose output port When an external bus is used, this port functions as a write signal output.			
34	26	27	P26/RD	Н	General-purpose output port When an external bus is used, this port functions as a read signal output.			

\*1: DIP-64P-M01

\*2: MDP-64C-P02 \*3: FPT-64P-M23 \*4: FPT-64P-M06 \*5: MQP-M64C-P01 (Continued)

DS07-12531-4E

Pin no.			Circuit				
SH-DIP <sup>*1</sup> MDIP <sup>*2</sup>	QFP2 <sup>*3</sup>	QFP1 <sup>*4</sup> MQFP <sup>*5</sup>	Pin name	type	Function		
33	25	26	P27/ALE	Н	General-purpose output port When an external bus is used, this port functions as an address latch signal output.		
2	58	59	P30/UCK1	G	General-purpose I/O port Also serves as the clock I/O 1 for the UART. This port is a hysteresis input type.		
1	57	58	P31/UO1	F	General-purpose I/O port Also serves as the data output 1 for the UART.		
63	55	56	P32/UI1	G	General-purpose I/O port Also serves as the data input 1 for the UART. This port is a hysteresis input type.		
62	54	55	P33/SCK1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.		
61	53	54	P34/SO1	F	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O.		
60	52	53	P35/SI1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.		
59	51	52	P36/PWC	G	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type.		
58	50	51	P37/WTO	F	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter.		
6	62	63	P40/UCK2	G	General-purpose I/O port Also serves as the clock I/O 2 for the UART. This port is a hysteresis input type.		
5	61	62	P41/UO2	F	General-purpose I/O port Also serves as the data output 2 for the UART.		
4	60	61	P42/UI2	G	General-purpose I/O port Also serves as the data input 2 for the UART. This port is a hysteresis input type.		
3	59	60	P43/PTO1	F	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer.		
10	2	3	P50/ADST	К	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.		

\*1: DIP-64P-M01

\*2: MDP-64C-P02

\*4: FPT-64P-M06

\*5: MQP-M64C-P01

\*3: FPT-64P-M23

(Continued)

Pin	no.	Pin name I/O		Function	
MDIP	MQFP		1/0	Function	
65	66	Vpp	0	"H" level output pin	
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	0	Address output pins	
75 76 77	77 78 79	01 02 03	Ι	Data input pins	
78	80	Vss	0	Power supply (GND) pin	
79 80 81 82 83	82 83 84 85 86	04 05 06 07 08	I	Data input pins	
84	87	CE	0	ROM chip enable pin Outputs "H" during standby.	
85	88	A10	0	Address output pin	
86	89	ŌĒ	0	ROM output enable pin Outputs "L" at all times.	
87 88 89	91 92 93	A11 A9 A8	0	Address output pins	
90	94	A13	0		
91	95	A14	0		
92	96	Vcc	0	EPROM power supply pin	
	65 76 81 90	N.C.	_	Internally connected pins Be sure to leave them open.	

• External EPROM pins (MB89PV630 only)

# ■ HANDLING DEVICES

## 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than Vcc or lower than Vss is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between Vcc and Vss.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AVcc and AVR) and analog input from exceeding the digital power supply (Vcc) when the analog system power supply is turned on and off.

#### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

#### 3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AVcc = DAVC = Vcc and AVss = AVR = Vss even if the A/D and D/A converters are not in use.

#### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

#### 5. Power Supply Voltage Fluctuations

Although V<sub>CC</sub> power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V<sub>CC</sub> ripple fluctuations (P-P value) will be less than 10% of the standard V<sub>CC</sub> value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

## 6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.

# • Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007<sup>H</sup> to 7FFF<sup>H</sup>. (Note that addresses 8000<sup>H</sup> to FFFF<sup>H</sup> in the operating mode assign to 0000<sup>H</sup> to 7FFF<sup>H</sup> in EPROM mode).
- (3) Load option data into addresses 0000H to 0006H of the EPROM programmer. (For information about each corresponding option, see "8. OTPROM Option Bit Map".)
- (4) Program with the EPROM programmer.

# 4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



# 5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

# ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

# 1. EPROM for Use

MBM27C256A-20CZ, MBM27C256A-20TV

# 2. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



# 3. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (3) Program to  $0000_{H}$  to  $7FFF_{H}$  with the EPROM programmer.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(Continued)

 $(AVcc = Vcc = 5.0 \text{ V}, \text{ AVss} = Vss = 0.0 \text{ V}, \text{ T}_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C})$ 

Paramotor	Symbol	Bin namo	Condition		Value	Unit	Pomarks	
Farameter	Symbol	Fin name	Condition	Min.	Тур.	Max.	Unit	Remarks
Power cumply	IA		$F_{CH} = 10 \text{ MHz},$ when A/D conversion operates.	_	6	_	mA	
Power supply current <sup>*1</sup>	Іан	AVcc	$F_{CH} = 10 \text{ MHz},$ $T_A = +25^{\circ}\text{C},$ when A/D conversion in a stop.	_	_	1	μΑ	
Input capacitance	CIN	Other than AVcc, AVss, Vcc, and Vss	f = 1 MHz	_	10	_	pF	

\*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not counted.

\*2: For information on t<sub>inst</sub>, see "(4) Instruction Cycle" in "4. AC Characteristics".

## 4. AC Characteristics

## (1) Reset Timing

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = \text{V}_{SS} = 0.0 \text{ V}, \text{ } T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C})$ 

Parameter	Symbol Condition		Val	he	Unit	Remarks	
Falanielei	Symbol	Condition	Min.	Max.	Onit	iteritar K5	
RST "L" pulse width	<b>t</b> zlzh		<b>48 t</b> HCYL	_	ns		



## (7) Bus Write Timing

Devementer	Symbol	Din nomo	Condition	Value	Unit	Domorko	
Parameter	Symbol	Fin name	Condition	Min.	Max.	Unit	Remarks
Valid address $\rightarrow$ ALE $\downarrow$ time	<b>t</b> avll	AD7 to AD0,		1/4 t <sub>inst</sub> *1-64 ns*2		μs	
ALE $\downarrow$ time $\rightarrow$ address loss time	<b>t</b> llax	ALE A15 to A08		5	—	ns	
Valid address $\rightarrow \overline{WR} \downarrow time$	<b>t</b> avwl	WR, ALE		1/4 t <sub>inst</sub> *1-60 ns*2		μs	
WR pulse width	<b>t</b> wlwh	WR		1/2 t <sub>inst</sub> *1 – 20 ns*2		μs	
Write data $\rightarrow \overline{WR} \uparrow$ time	tovwн	AD7 to AD0, WR		1/2 t <sub>inst</sub> *1-60 ns*2		μs	
$\overline{WR} \uparrow \rightarrow address  loss time$	<b>t</b> whax	WR, A15 to A08		1/4 t <sub>inst</sub> *1-40 ns*2		μs	
$\overline{WR} \uparrow \rightarrow data  hold time$	<b>t</b> whdx	AD7 to AD0, WR		1/4 t <sub>inst</sub> *1-40 ns*2		μs	
$\overline{WR} \uparrow \rightarrow ALE \uparrow time$	twhlh	WR, ALE		1/4 t <sub>inst</sub> *1-40 ns*2		μs	
$\overline{WR} \downarrow \rightarrow CLK \uparrow time$	<b>t</b> wLCH			1/4 t <sub>inst</sub> *1-40 ns*2		μs	
$CLK \downarrow \to \overline{WR} \uparrow time$	<b>t</b> CLWH	WR, ULN		0		ns	
ALE pulse width	<b>t</b> lhll	ALE	1	1/4 t <sub>inst</sub> *1-35 ns*2		μs	
ALE $\downarrow \rightarrow$ CLK $\uparrow$ time	<b>t</b> llch	ALE,CLK		1/4 t <sub>inst</sub> *1-30 ns*2	_	μs	

#### (Vcc = 5.0 V±10%, FcH = 10 MHz, AVss = Vss= 0.0 V, TA = $-40^{\circ}C$ to $+85^{\circ}C$ )

\*1: For information on t<sub>inst</sub>, see "(4) Instruction Cycle".

\*2: This characteristics are also applicable to the bus read timing.



## 7. Notes on Using A/D Converter

#### · Input impedance of the analog input pins

The output impedance of the external circuit for the analog input must satisfy the following conditions. If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6  $\mu$ s at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 k $\Omega$ .



#### • Error

The smaller the | AVR-AVss |, the greater the error would become relatively.

# ■ CHARACTERISTICS EXAMPLE

## (1) "L" Level Output Voltage



#### (2) "H" Level Output Voltage



#### (3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



#### (4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)







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Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

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