

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1483e1

(Continued)

- UART
CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
Start by an external input capable
- External interrupt: 4 channels
Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
Stop mode (Oscillation stops to minimize the current consumption.)
Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
Subclock mode
Watch mode
- Bus interface function
With hold and ready function

MB89630R Series

■ PRODUCT LINEUP

Part number Item	MB89635R	MB89636R	MB89637R	MB89P637	MB89PV630
Classification	Mass-produced products (mask ROM products)			One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (Internal PROM, to be programmed with general- purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	512 × 8 bits	768 × 8 bits	1024 × 8 bits	1024 × 8 bits	1024 × 8 bits
CPU functions	The number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 μs/10 MHz, 61 μs@32.768 kHz Interrupt processing time: 3.6 to 57.6 μs/10 MHz, 562.5 μs@32.768 kHz				
Ports	Input ports: 5 (All also serve as peripherals.) Output ports (N-ch open-drain): 8 (All also serve as peripherals.) I/O ports (N-ch open-drain): 4 (All also serve as peripherals.) Output ports (CMOS): 8 (All also serve as bus control.) I/O ports (CMOS): 28 (27 ports also serve as bus pins and peripherals.) Total: 53				
Watch timer	21 bits × 1 (in main clock)/15 bits × 1 (at 32.768 kHz)				
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 μs to 3.3 ms) × 2 channels 7/8-bit resolution PWM operation (conversion cycle: 51.2 μs to 839 ms) × 2 channels				
8-bit pulse width count timer	8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 μs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 μs) 8-bit pulse width measurement operation (capable of continuous measurement, and measurement of "H" pulse width/ "L" pulse width/ from ↑ to ↑/from ↓ to ↓)				
16-bit timer/counter	16-bit timer operation (operating clock cycle: 0.4 μs) 16-bit event counter operation (rising edge/falling edge/both edge selectable)				
8-bit serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs)				
UART	Capable of switching two I/O systems by software Transfer data length (6, 7, and 8 bits) Transfer rate (300 to 62500 bps. at 10 MHz oscillation)				
10-bit A/D converter	10-bit resolution × 8 channels A/D conversion mode (conversion time: 13.2 μs) Sense mode (conversion time: 7.2 μs) Capable of continuous activation by an external activation or an internal timer				

(Continued)

PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP ^{*1} MDIP ^{*2}	QFP2 ^{*3}	QFP1 ^{*4} MQFP ^{*5}			
30	22	23	X0	A	Main clock crystal oscillator pins
31	23	24	X1		
28	20	21	MOD0	D	Operating mode selection pins Connect directly to V _{CC} or V _{SS} .
29	21	22	MOD1		
27	19	20	RST	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
56 to 49	48 to 41	49 to 42	P00/AD0 to P07/AD7	F	General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.
48 to 41	40 to 33	41 to 34	P10/A08 to P17/A157	F	General-purpose I/O ports When an external bus is used, these ports function as an upper address output.
40	32	33	P20/BUFC	H	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	31	32	P21/HAK	H	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.
38	30	31	P22/HRQ	F	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	29	30	P23/RDY	F	General-purpose output port When an external bus is used, this port functions as a ready input.
36	28	29	P24/CLK	H	General-purpose output port When an external bus is used, this port functions as a clock output.
35	27	28	P25/WR	H	General-purpose output port When an external bus is used, this port functions as a write signal output.
34	26	27	P26/RD	H	General-purpose output port When an external bus is used, this port functions as a read signal output.

*1: DIP-64P-M01
*2: MDP-64C-P02
*3: FPT-64P-M23

*4: FPT-64P-M06
*5: MQP-M64C-P01

(Continued)

MB89630R Series

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
33	25	26	P27/ALE	H	General-purpose output port When an external bus is used, this port functions as an address latch signal output.
2	58	59	P30/UCK1	G	General-purpose I/O port Also serves as the clock I/O 1 for the UART. This port is a hysteresis input type.
1	57	58	P31/UO1	F	General-purpose I/O port Also serves as the data output 1 for the UART.
63	55	56	P32/UI1	G	General-purpose I/O port Also serves as the data input 1 for the UART. This port is a hysteresis input type.
62	54	55	P33/SCK1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
61	53	54	P34/SO1	F	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O.
60	52	53	P35/SI1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
59	51	52	P36/PWC	G	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type.
58	50	51	P37/WTO	F	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter.
6	62	63	P40/UCK2	G	General-purpose I/O port Also serves as the clock I/O 2 for the UART. This port is a hysteresis input type.
5	61	62	P41/UO2	F	General-purpose I/O port Also serves as the data output 2 for the UART.
4	60	61	P42/UI2	G	General-purpose I/O port Also serves as the data input 2 for the UART. This port is a hysteresis input type.
3	59	60	P43/PTO1	F	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer.
10	2	3	P50/ADST	K	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.

*1: DIP-64P-M01
 *2: MDP-64C-P02
 *3: FPT-64P-M23

*4: FPT-64P-M06
 *5: MQP-M64C-P01

(Continued)

MB89630R Series

(Continued)

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up resistor optional
H		CMOS output
I		Analog input
J		<ul style="list-style-type: none"> • CMOS input • Pull-up resistor optional
K		<ul style="list-style-type: none"> • Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{CC} = DAVC = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.

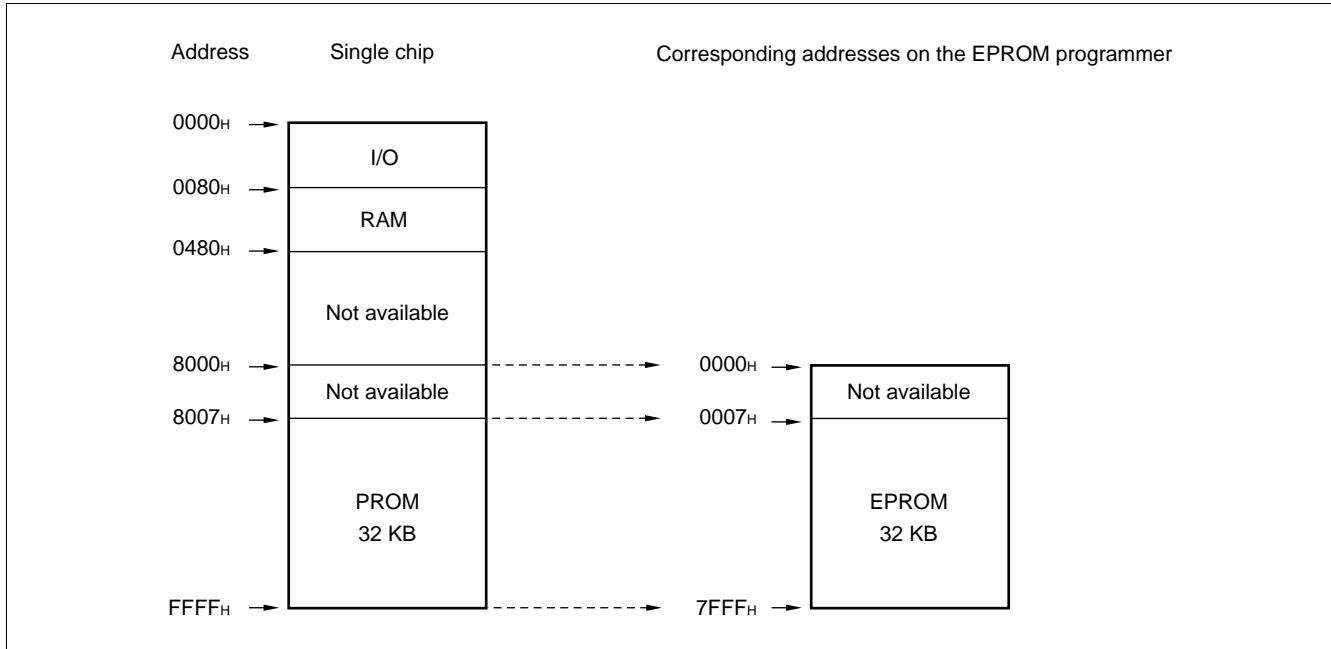
■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20CZ, MBM27C256A-20TV

2. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007H to 7FFFH.
- (3) Program to 0000H to 7FFFH with the EPROM programmer.

MB89630R Series

2. Registers

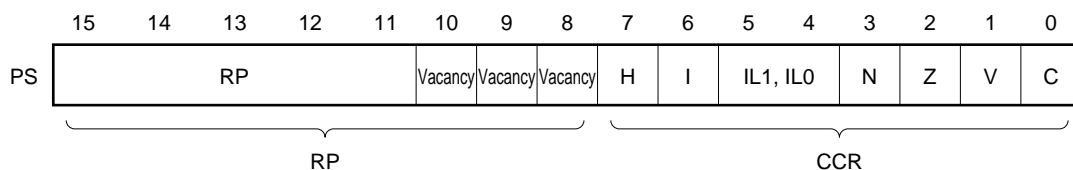
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A16-bit register for index modification
Extra pointer (EP):	A16-bit pointer for indicating a memory address
Stack pointer (SP):	A16-bit register for indicating a stack area
Program status (PS):	A16-bit register for storing a register pointer, a condition code

16 bits		Initial value
PC	: Program counter	FFFD _H
A	: Accumulator	Indeterminate
T	: Temporary accumulator	Indeterminate
IX	: Index register	Indeterminate
EP	: Extra pointer	Indeterminate
SP	: Stack pointer	Indeterminate
PS	: Program status	I-flag = 0, IL1, IL0 = 11 The other bit values are indeterminate.

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the program status register



■ I/O MAP

Address	Read/write	Register name	Register description
00 _H	(R/W)	PDR0	Port 0 data register
01 _H	(W)	DDR0	Port 0 data direction register
02 _H	(R/W)	PDR1	Port 1 data register
03 _H	(W)	DDR1	Port 1 data direction register
04 _H	(R/W)	PDR2	Port 2 data register
05 _H	(W)	BCTR	External bus pin control register
06 _H	Vacancy		
07 _H	(R/W)	SYCC	System clock control register
08 _H	(R/W)	STBC	System clock control register
09 _H	(R/W)	WDTE	Watchdog timer control register
0A _H	(R/W)	TBCR	Timebase timer control register
0B _H	(R/W)	WPCR	Watch prescaler control register
0C _H	(R/W)	CHG3	Port 3 switching register
0D _H	(R/W)	PDR3	Port 3 data register
0E _H	(W)	DDR3	Port 3 data direction register
0F _H	(R/W)	PDR4	Port 4 data register
10 _H	(W)	DDR4	Port 4 data direction register
11 _H	(R/W)	BUZR	Buzzer register
12 _H	(R/W)	PDR5	Port 5 data register
13 _H	(R/W)	PDR6	Port 6 data register
14 _H	(R)	PDR7	Port 7 data register
15 _H	(R/W)	PCR1	PWC pulse width control register 1
16 _H	(R/W)	PCR2	PWC pulse width control register 2
17 _H	(R/W)	RLBR	PWC reload buffer register
18 _H	(R/W)	TMCR	16-bit timer control register
19 _H	(R/W)	TCHR	16-bit timer count register (H)
1A _H	(R/W)	TCLR	16-bit timer count register (L)
1B _H	Vacancy		
1C _H	(R/W)	SMR1	Serial mode register
1D _H	(R/W)	SDR1	Serial data register
1E _H	Vacancy		
1F _H	Vacancy		

(Continued)

MB89630R Series

(Continued)

Address	Read/write	Register name	Register description
20 _H	(R/W)	ADC1	A/D converter control register 1
21 _H	(R/W)	ADC2	A/D converter control register 2
22 _H	(R/W)	ADDH	A/D converter data register (H)
23 _H	(R/W)	ADDL	A/D converter data register (L)
24 _H	(R/W)	EIC1	External interrupt control register 1
25 _H	(R/W)	EIC2	External interrupt control register 2
26 _H	Vacancy		
27 _H	Vacancy		
28 _H	(R/W)	CNTR1	PWM timer control register 1
29 _H	(R/W)	CNTR2	PWM timer control register 2
2A _H	(R/W)	CNTR3	PWM timer control register 3
2B _H	(W)	COMR1	PWM timer compare register 1
2C _H	(W)	COMR2	PWM timer compare register 2
2D _H	(R/W)	SMC	UART serial mode control register
2E _H	(R/W)	SRC	UART serial rate control register
2F _H	(R/W)	SSD	UART serial status/data register
30 _H	(R) (W)	SIDR SODR	UART serial input data control register UART serial output data control register
31 _H to 7B _H	Vacancy		
7C _H	(W)	ILR1	Interrupt level setting register 1
7D _H	(W)	ILR2	Interrupt level setting register 2
7E _H	(W)	ILR3	Interrupt level setting register 3
7F _H	Vacancy		

Note: Do not use vacancies.

MB89630R Series

($AV_{CC} = V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition		Value			Unit	Remarks
					Min.	Typ.	Max.		
Pull-up resistance	R _{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V _I = 0.0 V		25	50	100	kΩ	With pull-up resistor
Power supply current*1	I _{CC1}	V _{CC}	F _{CH} = 10 MHz V _{CC} = 5.0 V t _{inst} *2 = 0.4 μs		—	12	20	mA	
	I _{CC2}		F _{CH} = 10 MHz V _{CC} = 3.0 V t _{inst} *2 = 6.4 μs		—	1.0	2	mA	MB89635R/ 636R/637R/ PV630
					—	1.5	2.5	mA	MB89P637
	I _{CCS1}		Sleep mode	F _{CH} = 10 MHz V _{CC} = 5.0 V t _{inst} *2 = 0.4 μs	—	3	7	mA	
	I _{CCS2}			F _{CH} = 10 MHz V _{CC} = 3.0 V t _{inst} *2 = 6.4 μs	—	0.5	1.5	mA	
	I _{CCL}		F _{CL} = 32.768 kHz, V _{CC} = 3.0 V Subclock mode		—	50	100	μA	MB89635R/ 636R/637R/ PV630
					—	500	700	μA	MB89P637
	I _{CCLS}		F _{CL} = 32.768 kHz, V _{CC} = 3.0 V Subclock sleep mode		—	25	50	μA	
	I _{CCT}		F _{CL} = 32.768 kHz, V _{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system		—	3	15	μA	
	I _{CCH}		T _A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system		—	—	1	μA	

(Continued)

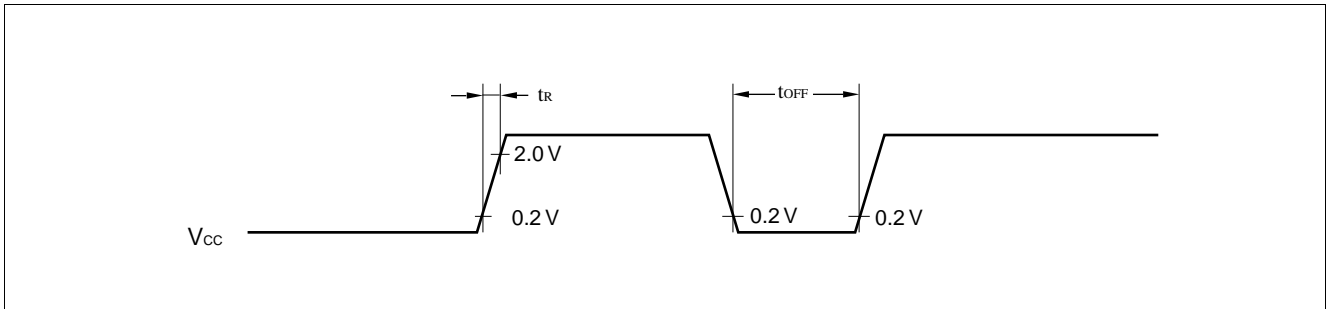
(2) Specification for Power-on Reset

($AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Min. interval time for the next power-on reset

Note: Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

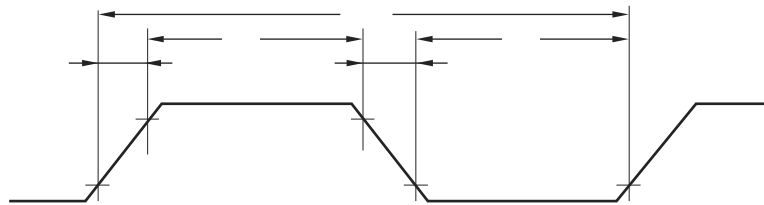


(3) Clock Timing

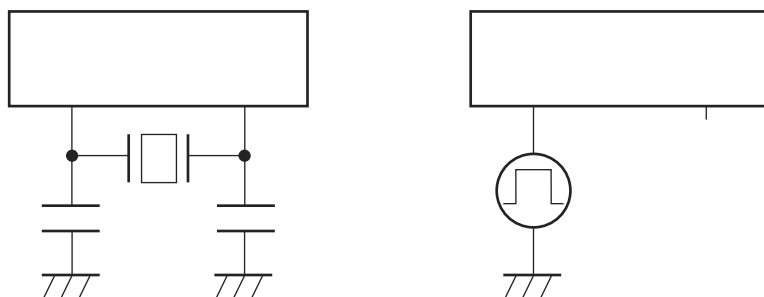
($AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	μs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WLH} P_{WLL}	X0A		—	15.2	—	μs	External clock
Input clock rising/ falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

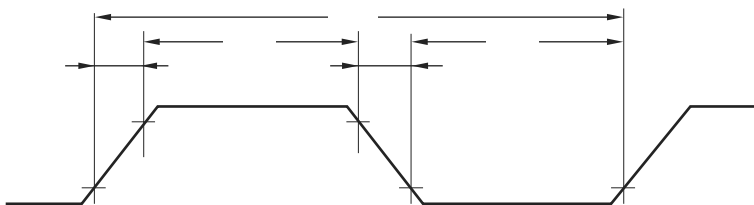
• Main clock timing condition



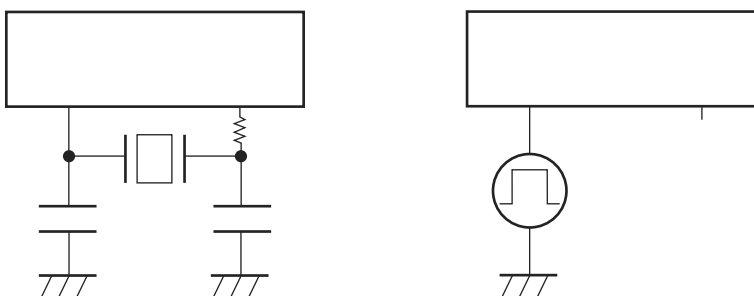
• Main clock configurations



• Subclock timing condition



• Subclock configurations



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	μs	$(4/F_{CH}) t_{inst} = 0.4 \mu s$, operating at $F_{CH} = 10 \text{ MHz}$
		$2/F_{CL}$	μs	$t_{inst} = 61.036 \mu s$, operating at $F_{CL} = 32.768 \text{ kHz}$

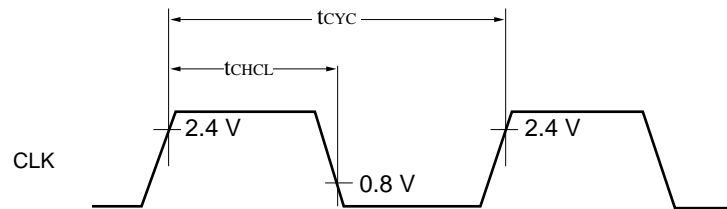
Note: Operating at 10 MHz, the cycle varies with the set execution time.

(5) Clock Output Timing

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	$1/2 t_{inst}^*$	—	μs	
CLK $\uparrow \rightarrow$ CLK \downarrow	t_{CHCL}	CLK		$1/4 t_{inst}^* - 70 \text{ ns}$	$1/4 t_{inst}^*$	μs	

* : For information on t_{inst} , see “(4) Instruction Cycle”.

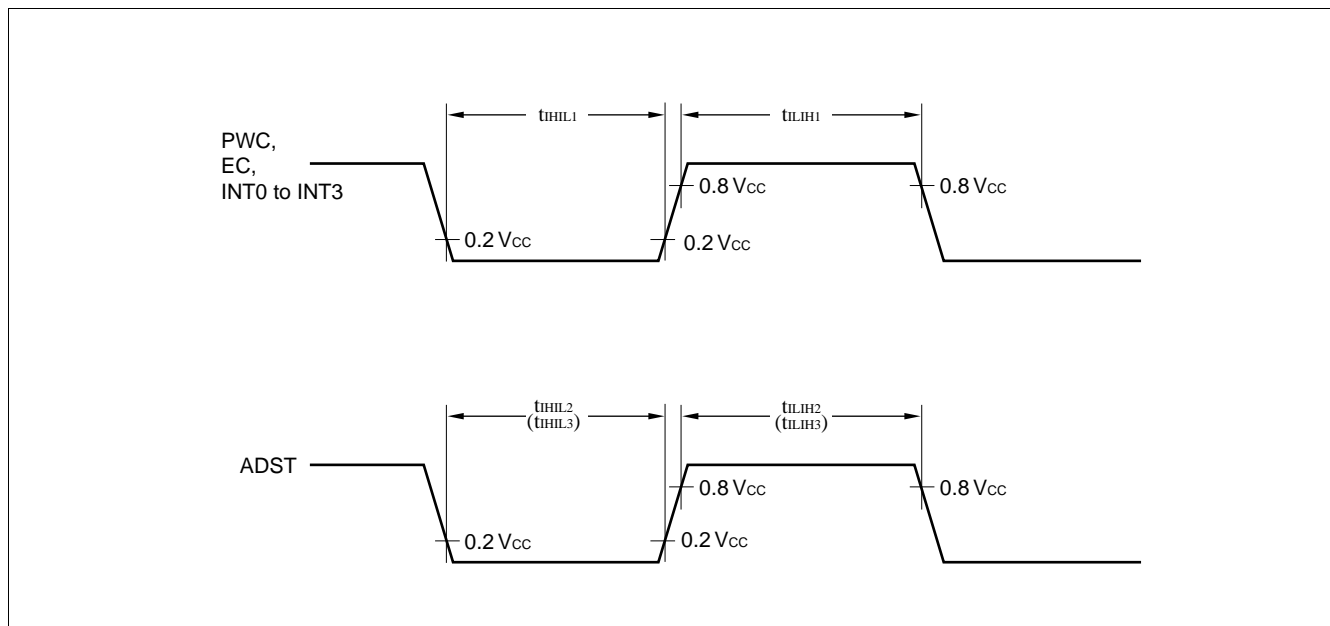


(10) Peripheral Input Timing

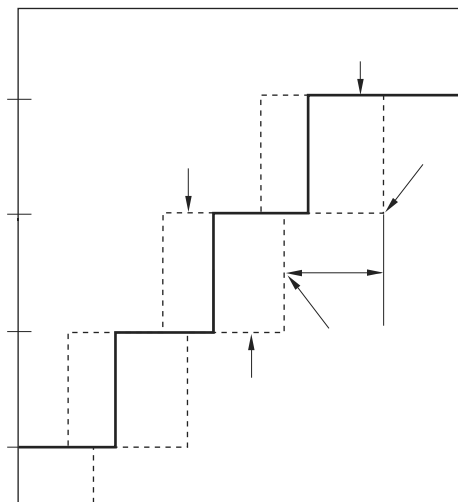
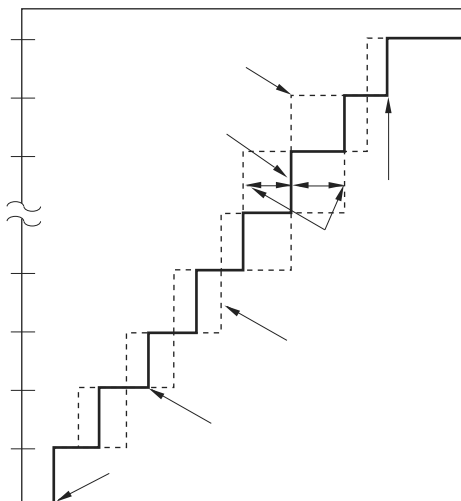
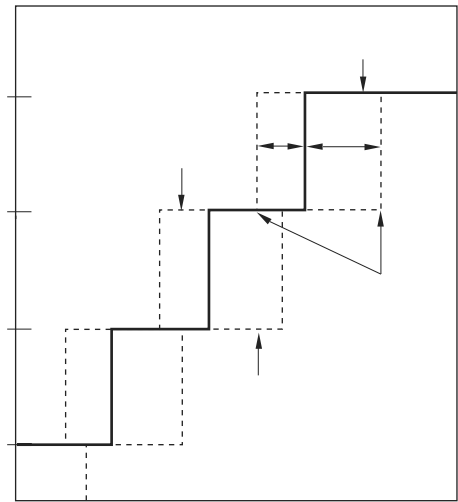
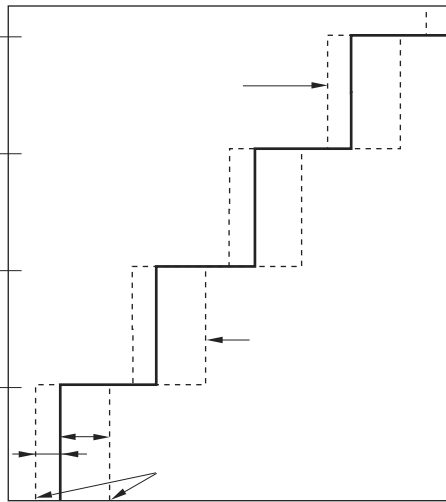
($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input "H" pulse width 1	t_{LIH1}	PWC, INT0 to INT3, EC	$2\ t_{inst}^*$	—	μs	
Peripheral input "L" pulse width 1	t_{HIL1}		$2\ t_{inst}^*$	—	μs	
Peripheral input "H" pulse width 2	t_{LIH2}	ADST	$2^8\ t_{inst}^*$	—	μs	A/D mode
Peripheral input "L" pulse width 2	t_{HIL2}		$2^8\ t_{inst}^*$	—	μs	A/D mode
Peripheral input "H" pulse width 3	t_{LIH3}	ADST	$2^8\ t_{inst}^*$	—	μs	Sense mode
Peripheral input "L" pulse width 3	t_{HIL3}		$2^8\ t_{inst}^*$	—	μs	Sense mode

* : For information on t_{inst} , see "(4) Instruction Cycle".



(Continued)



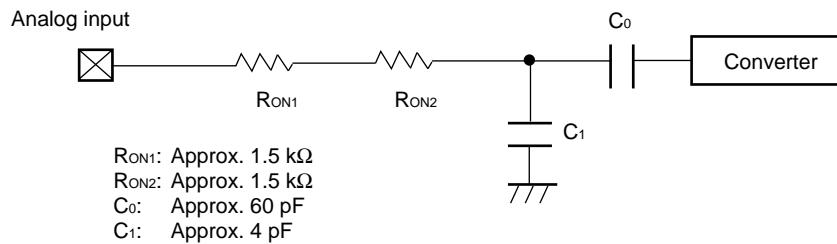
7. Notes on Using A/D Converter

• Input impedance of the analog input pins

The output impedance of the external circuit for the analog input must satisfy the following conditions.

If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 μ s at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 k Ω .

• Analog input circuit model

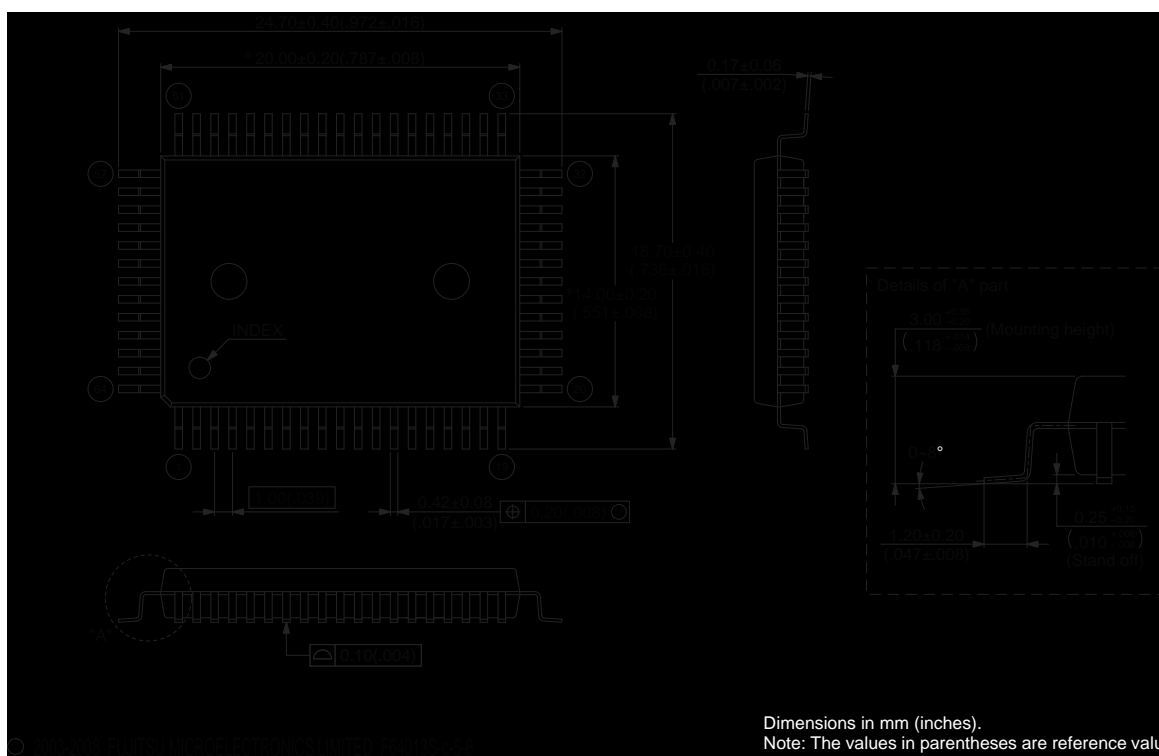
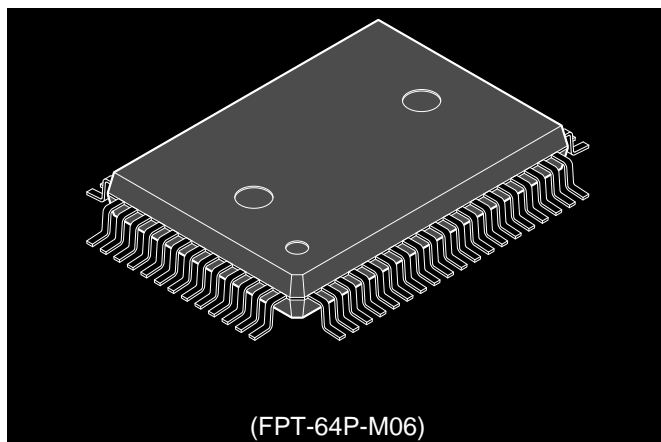


Note: The values mentioned here should be used as a guideline.

• Error

The smaller the $|AVR - AV_{ss}|$, the greater the error would become relatively.

MB89630R Series



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

MB89630R Series

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
49	■ MASK OPTIONS	Changed the explanation for "*" in "■ MASK OPTIONS".

The vertical lines marked in the left side of the page show the changes.

MEMO