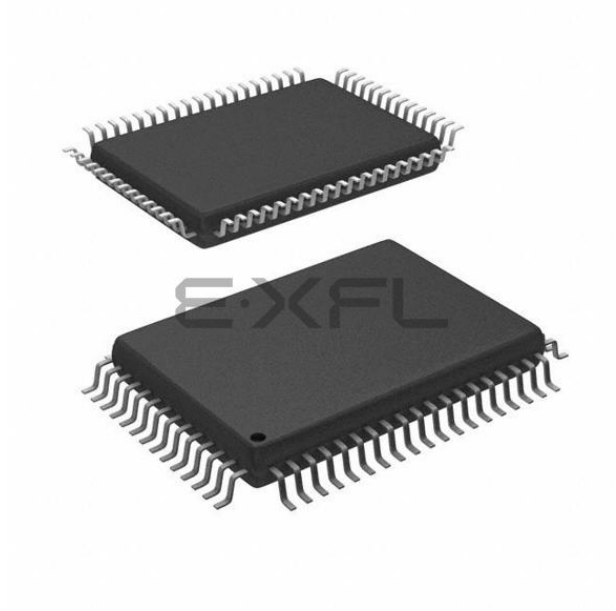


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1485

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12531-4E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89630R Series

MB89635R/636R/637R/P637/PV630

■ OUTLINE

The MB89630R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

* : F²MC is the abbreviation for Fujitsu Flexible Microcontroller.

■ FEATURES

- High-speed operating capability at low voltage
- Minimum execution time: 0.4 µs@3.5 V, 0.8 µs@2.7 V
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Five types of timers
  8-bit PWM timer: 2 channels (Also usable as a reload timer)
  8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
  16-bit timer/counter
  21-bit timebase timer

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2009.5

(Continued)

- UART
  CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  Start by an external input capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Bus interface function
  With hold and ready function

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P637, the program area starts from address 8007_H but on the MB89PV630 and MB89637R starts from 8000_H.

  (On the MB89P637, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637R, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637.)
- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM. However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics".)

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options".

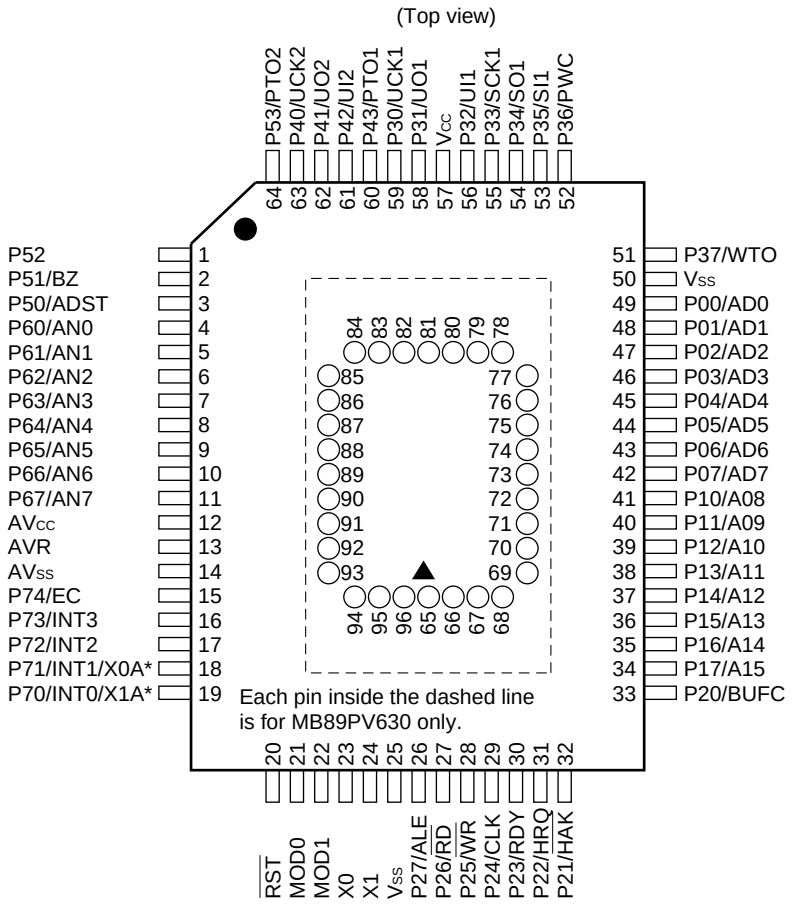
Take particular care on the following points:

- A pull-up resistor cannot be set for P50 to P53 on the MB89P637.
- Options are fixed on the MB89PV630.

4. Differences between the MB89630 and MB89630R Series

- Memory access area
  There are no difference between the access area of MB89635/MB89635R, and that of MB89637/MB89637R. The access area of MB89636 is different from that of the MB89636R when using in external bus mode.

Address	Memory area	
	MB89636	MB89636R
0000_H to $007F_H$	I/O area	I/O area
0080_H to $037F_H$	RAM area	RAM area
0380_H to $047F_H$	External area	Access prohibited
0480_H to $7FFF_H$		External area
8000_H to $9FFF_H$		Access prohibited
$A000_H$ to $FFFF_H$	ROM area	ROM area



(FPT-64P-M06)
(MQP-64C-P01)

*: When the dual-clock system is selected.

- **Pin assignment on package top (MB89PV630 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: Internally connected. Do not use.

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
33	25	26	P27/ALE	H	General-purpose output port When an external bus is used, this port functions as an address latch signal output.
2	58	59	P30/UCK1	G	General-purpose I/O port Also serves as the clock I/O 1 for the UART. This port is a hysteresis input type.
1	57	58	P31/UO1	F	General-purpose I/O port Also serves as the data output 1 for the UART.
63	55	56	P32/UI1	G	General-purpose I/O port Also serves as the data input 1 for the UART. This port is a hysteresis input type.
62	54	55	P33/SCK1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
61	53	54	P34/SO1	F	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O.
60	52	53	P35/SI1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
59	51	52	P36/PWC	G	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type.
58	50	51	P37/WTO	F	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter.
6	62	63	P40/UCK2	G	General-purpose I/O port Also serves as the clock I/O 2 for the UART. This port is a hysteresis input type.
5	61	62	P41/UO2	F	General-purpose I/O port Also serves as the data output 2 for the UART.
4	60	61	P42/UI2	G	General-purpose I/O port Also serves as the data input 2 for the UART. This port is a hysteresis input type.
3	59	60	P43/PTO1	F	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer.
10	2	3	P50/ADST	K	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.

*1: DIP-64P-M01
*2: MDP-64C-P02
*3: FPT-64P-M23
*4: FPT-64P-M06
*5: MQP-M64C-P01

(Continued)

- **External EPROM pins (MB89PV630 only)**

Pin no.		Pin name	I/O	Function
MDIP	MQFP			
65	66	V_{PP}	O	"H" level output pin
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
84	87	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
85	88	A10	O	Address output pin
86	89	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

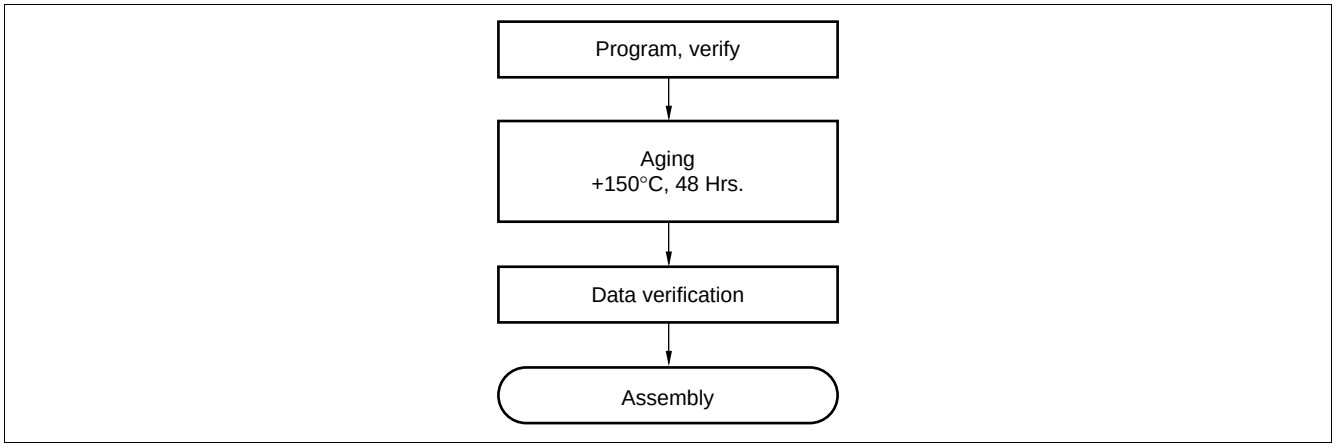
(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$. (Note that addresses 8000_H to $FFFF_H$ in the operating mode assign to 0000_H to $7FFF_H$ in EPROM mode).

(3) Load option data into addresses 0000_H to 0006_H of the EPROM programmer.
(For information about each corresponding option, see “8. OTPROM Option Bit Map”.)

(4) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

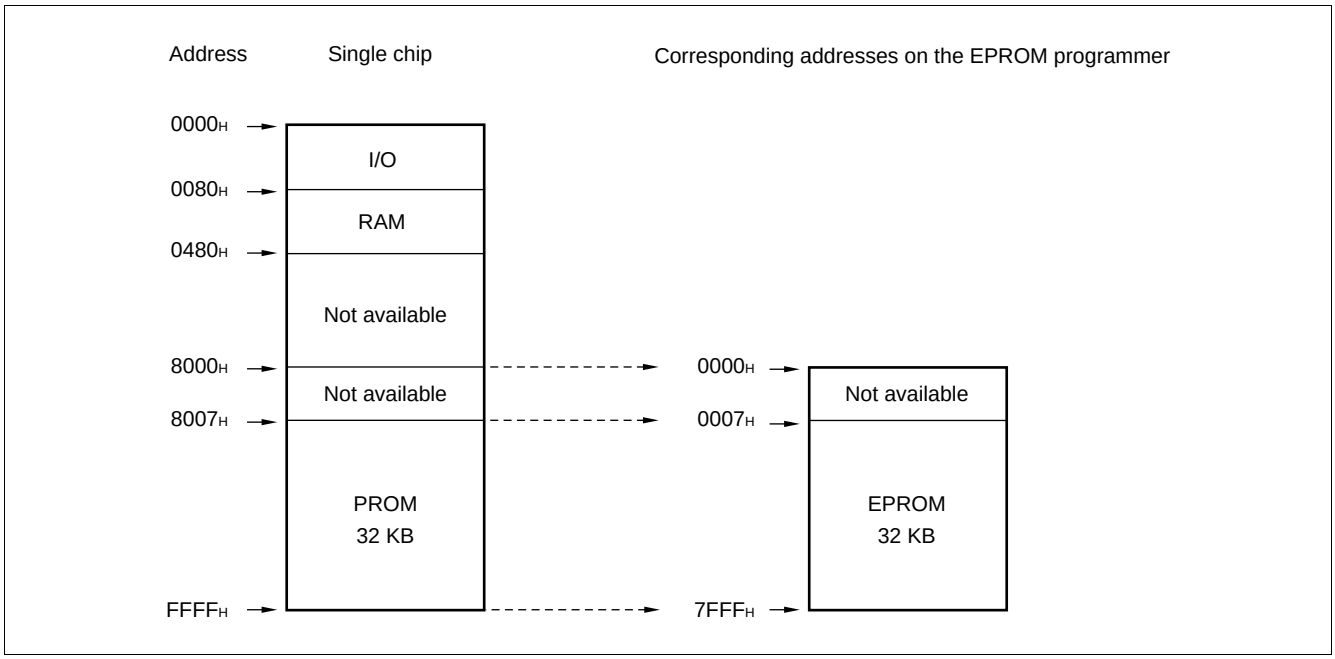
■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20CZ, MBM27C256A-20TV

2. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

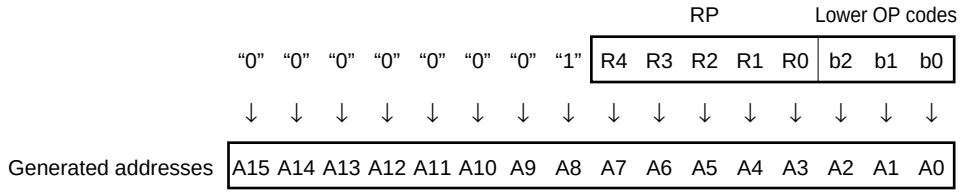
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• Rule for conversion of actual addresses of the general-purpose register area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

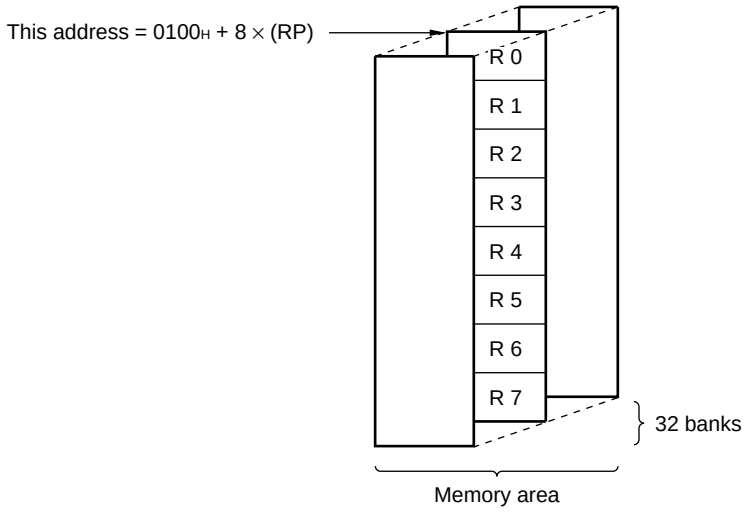
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).

• Register bank configuration



(Continued)

Address	Read/write	Register name	Register description
20H	(R/W)	ADC1	A/D converter control register 1
21H	(R/W)	ADC2	A/D converter control register 2
22H	(R/W)	ADDH	A/D converter data register (H)
23H	(R/W)	ADDL	A/D converter data register (L)
24H	(R/W)	EIC1	External interrupt control register 1
25H	(R/W)	EIC2	External interrupt control register 2
26H	Vacancy		
27H	Vacancy		
28H	(R/W)	CNTR1	PWM timer control register 1
29H	(R/W)	CNTR2	PWM timer control register 2
2AH	(R/W)	CNTR3	PWM timer control register 3
2BH	(W)	COMR1	PWM timer compare register 1
2CH	(W)	COMR2	PWM timer compare register 2
2DH	(R/W)	SMC	UART serial mode control register
2EH	(R/W)	SRC	UART serial rate control register
2FH	(R/W)	SSD	UART serial status/data register
30H	(R) (W)	SIDR SODR	UART serial input data control register UART serial output data control register
31H to 7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacancy		

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*
A/D converter reference input voltage	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AVR must not exceed "AV_{CC} + 0.3 V".
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P50 to P53
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P50 to P53
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P50 to P53
	V_{O2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P50 to P53
"L" level maximum output current	I_{OL}	—	20	mA	
"L" level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH}	—	–20	mA	
"H" level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	ΣI_{OH}	—	–50	mA	
"H" level total average output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89635R/ 636R/637R/ PV630
				—	1.5	2.5	mA	MB89P637
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89635R/ 636R/637R/ PV630
				—	500	700	µA	MB89P637
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	

(Continued)

(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 0.4 µs, operating at F_{CH} = 10 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs, operating at F_{CL} = 32.768 kHz

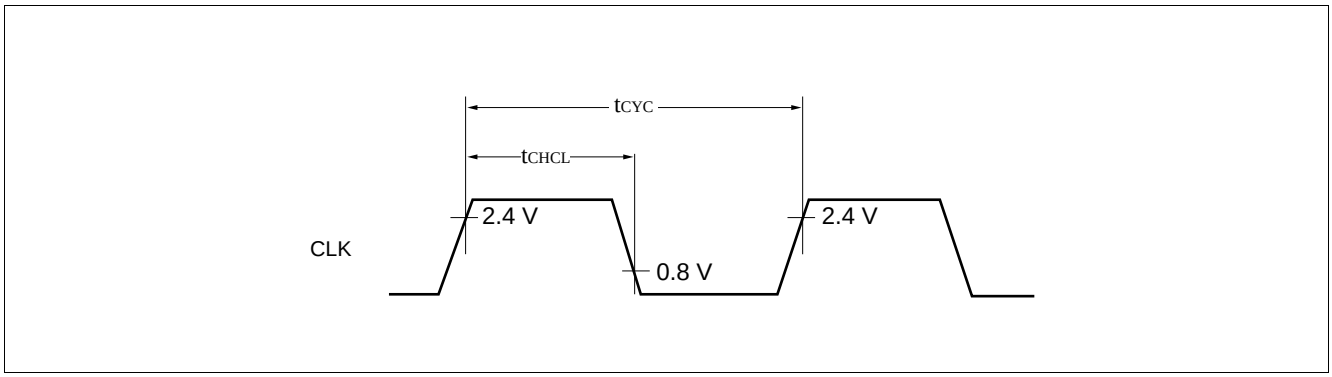
Note: Operating at 10 MHz, the cycle varies with the set execution time.

(5) Clock Output Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	1/2 t_{inst}*	—	µs	
CLK ↑ → CLK ↓	t_{CHCL}	CLK		1/4 t_{inst}* – 70 ns	1/4 t_{inst}*	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

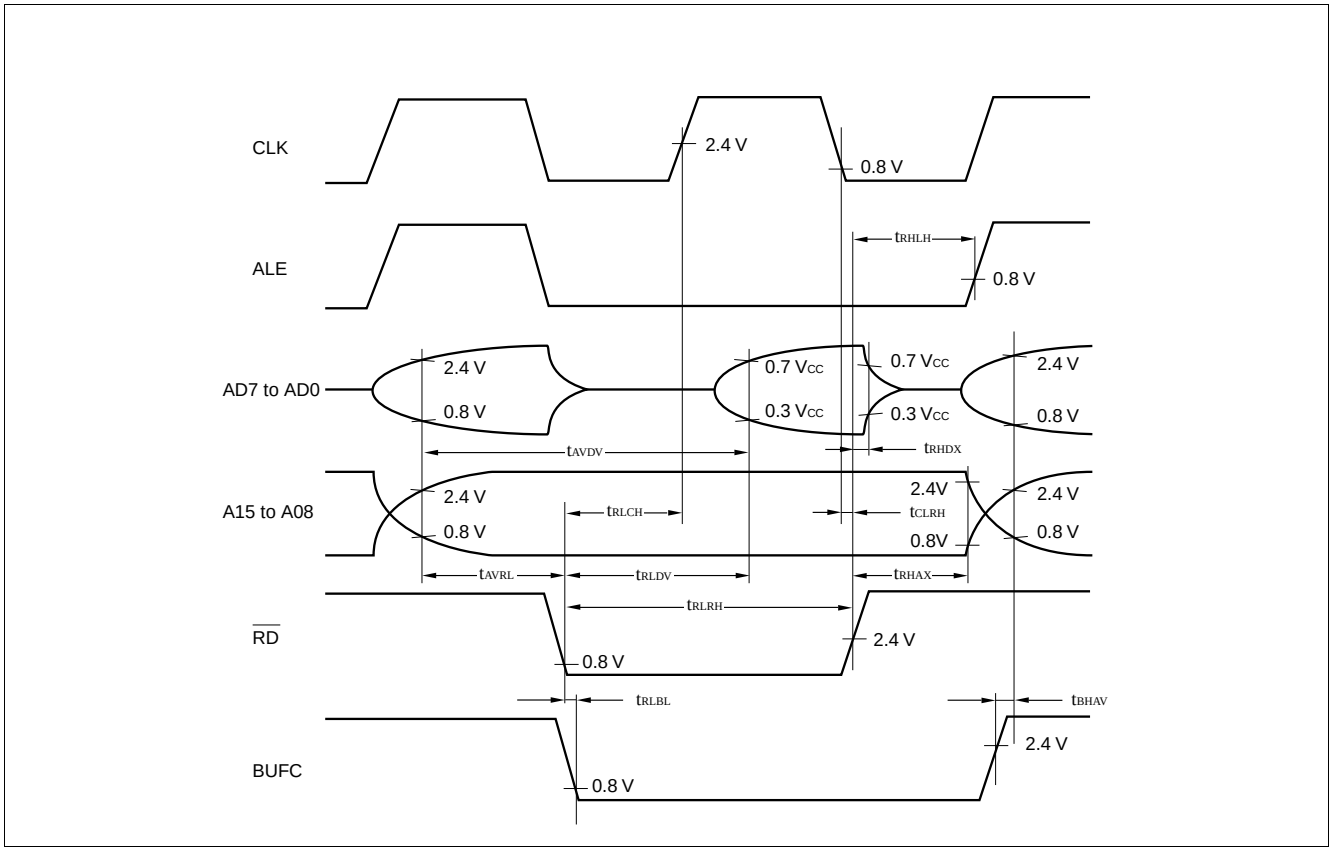


(6) Bus Read Timing

(V_{CC} = 5.0 V±10%, 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

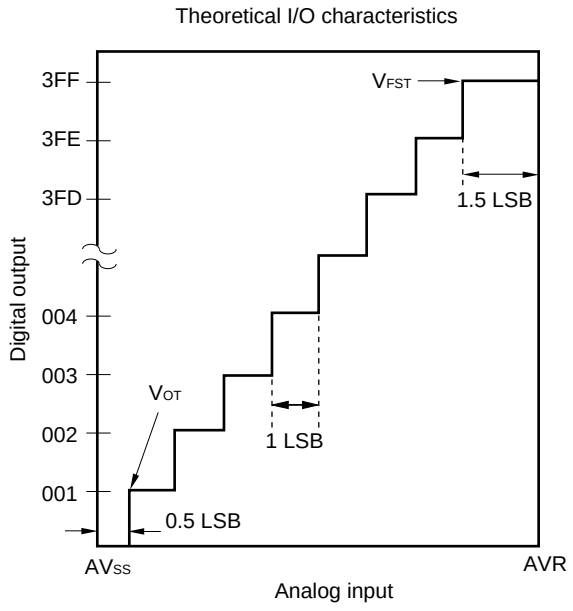
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to A08, AD7 to AD0	—	1/4 t_{inst}*– 64 ns	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst}*– 20 ns	—	µs	
Valid address → data read time	t_{AVDV}	AD7 to AD0, A15 to A08		1/2 t_{inst}*	200	µs	No wait
$\overline{RD}$ ↓ → data read time	t_{RLDV}	$\overline{RD}$, AD7 to AD0		1/2 t_{inst}*– 80 ns	120	µs	No wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to AD0, $\overline{RD}$		0	—	µs	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}*– 40 ns	—	µs	
$\overline{RD}$ ↑ → address loss time	t_{RHAX}	$\overline{RD}$, A15 to A08		1/4 t_{inst}*– 40 ns	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}*– 40 ns	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}			0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	µs	
BUFC ↑ → valid address time	t_{BHAV}	A15 to A08, AD7 to AD0, BUFC		5	—	µs	

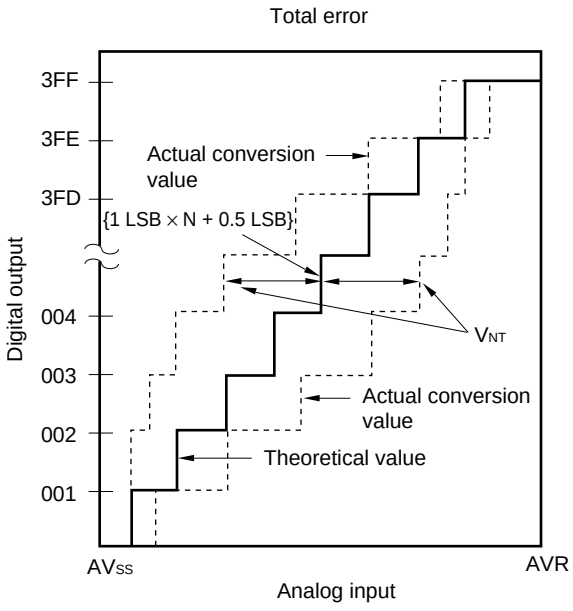
* : For information on t_{inst}, see “(4) Instruction Cycle”.



6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



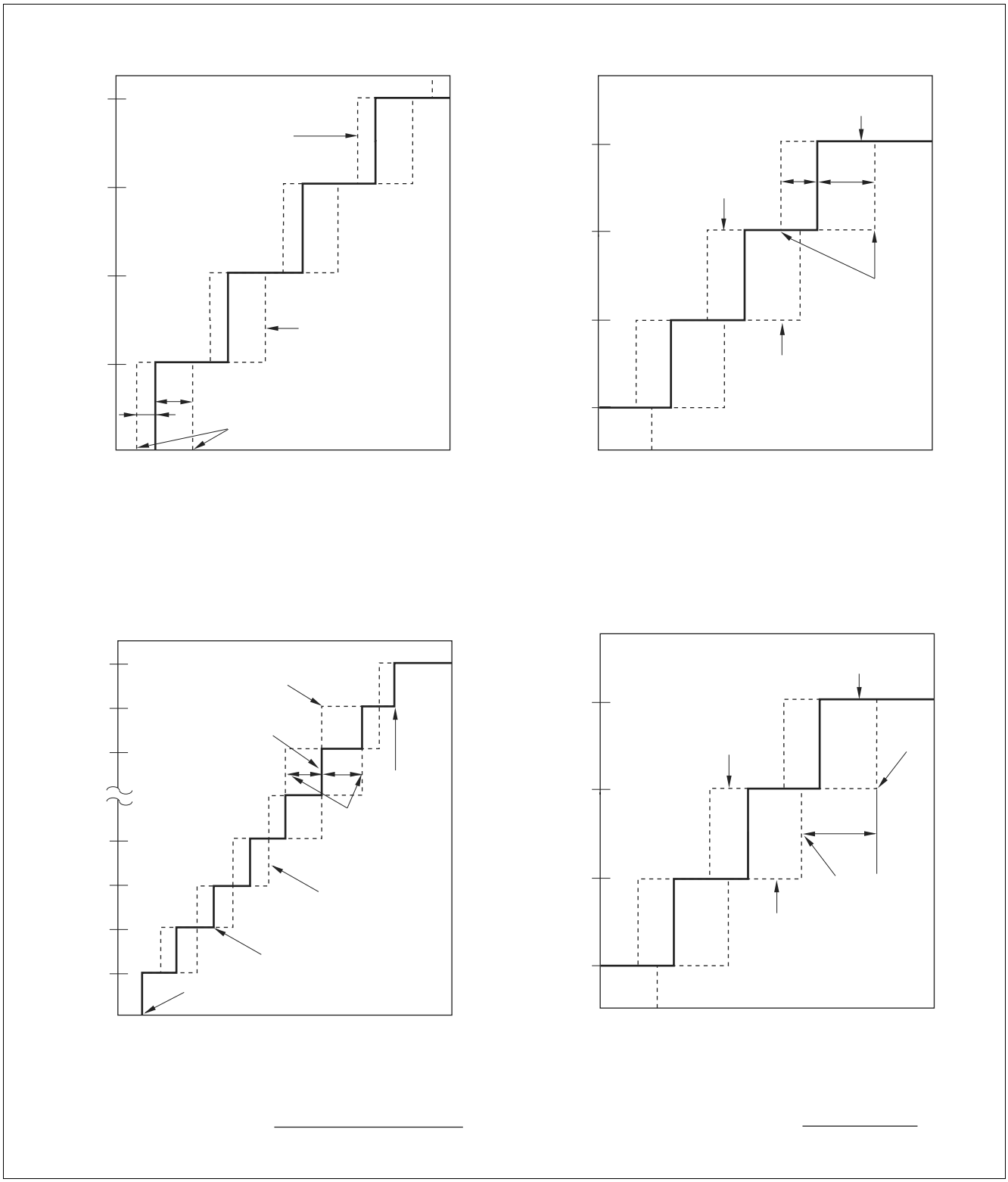


$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

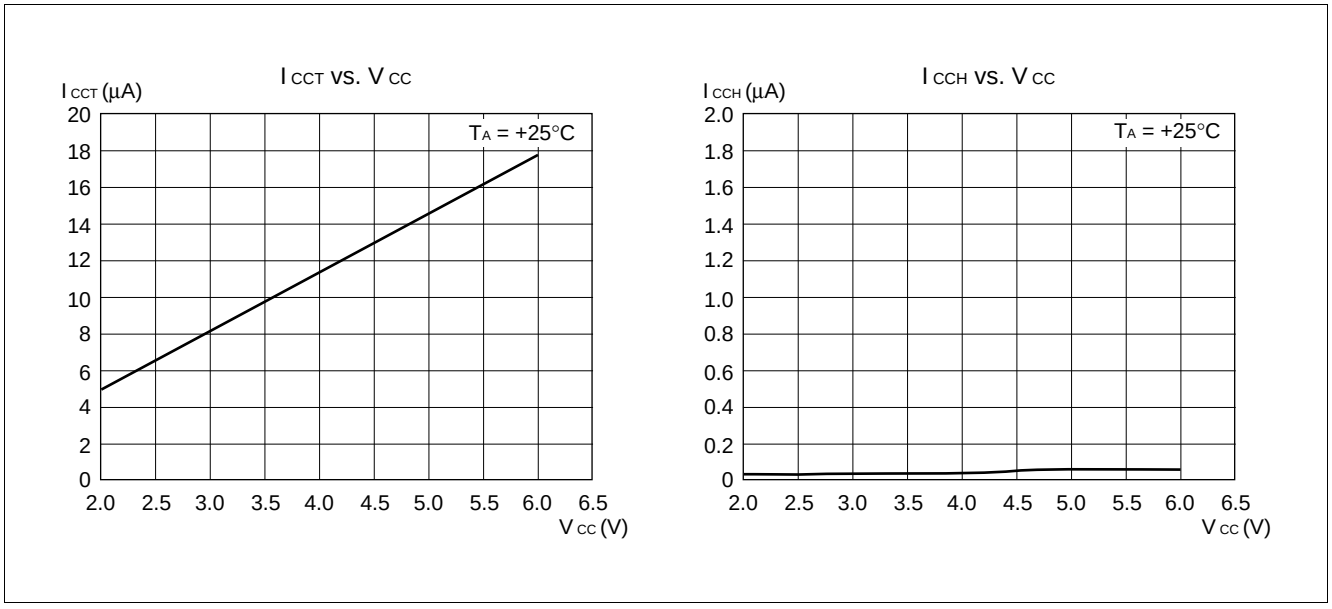
$$\text{Digital output N total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

(Continued)

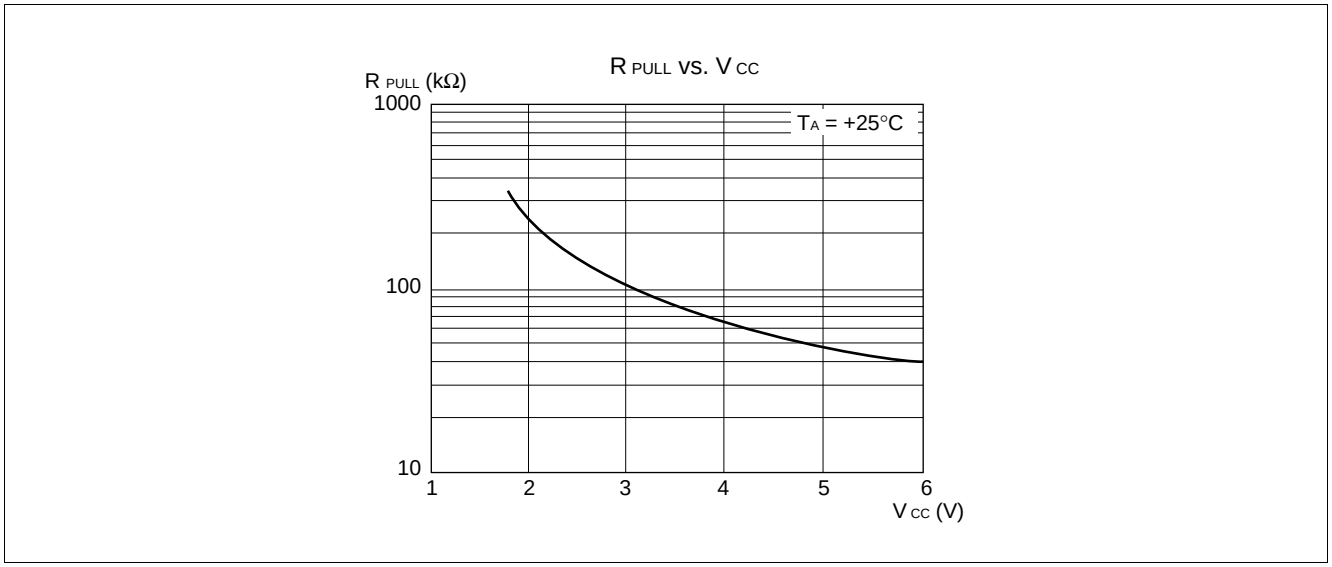
(Continued)

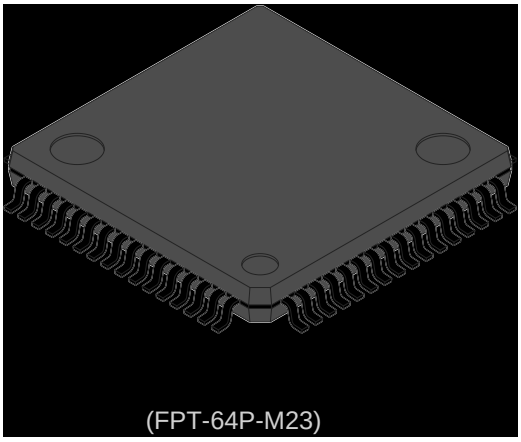


(Continued)

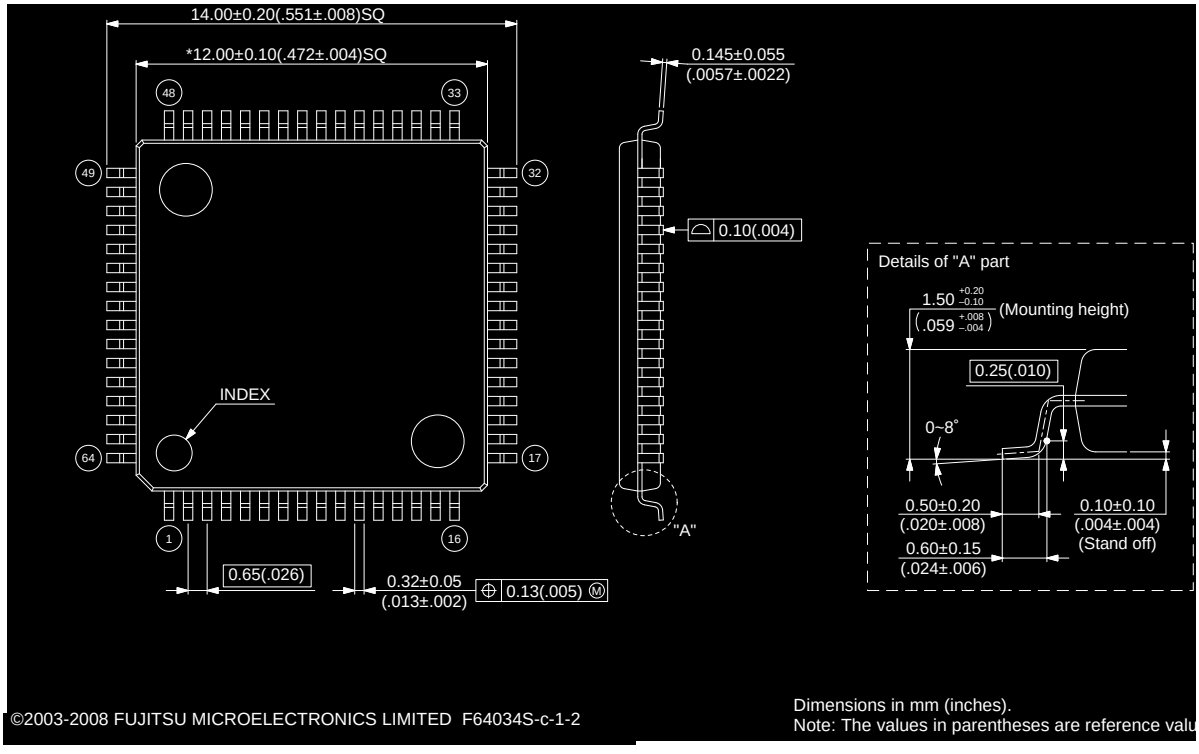


(6) Pull-up Resistance





(FPT-64P-M23)



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

(Continued)

MEMO