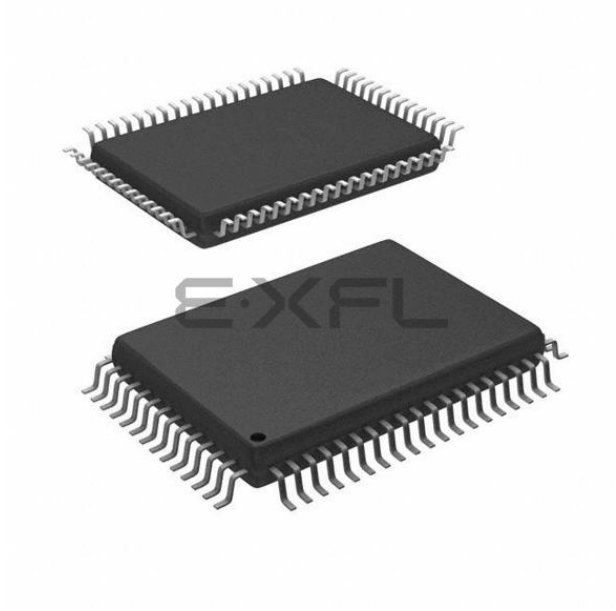

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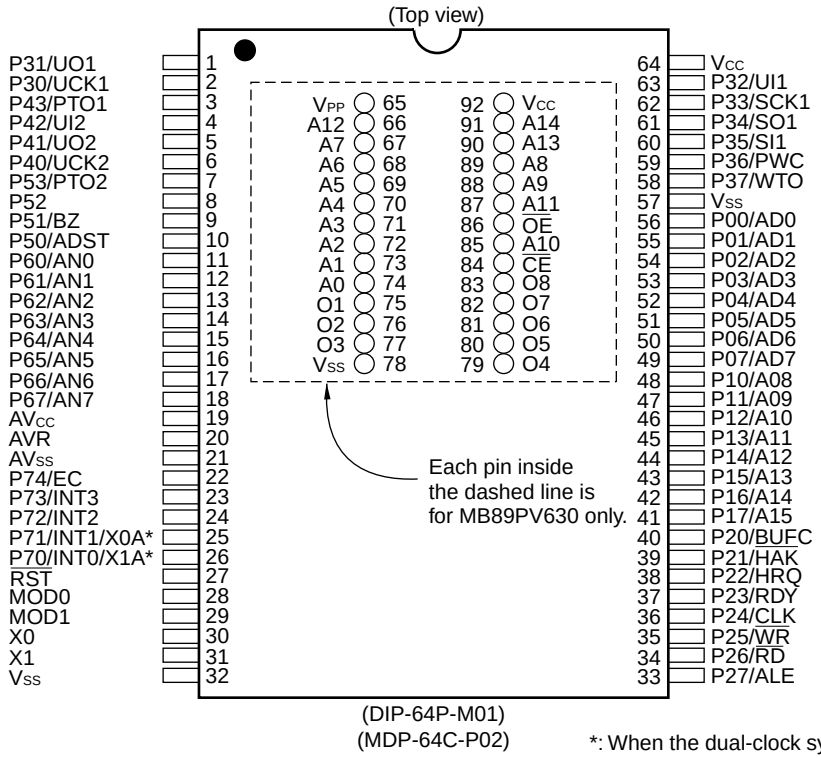
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

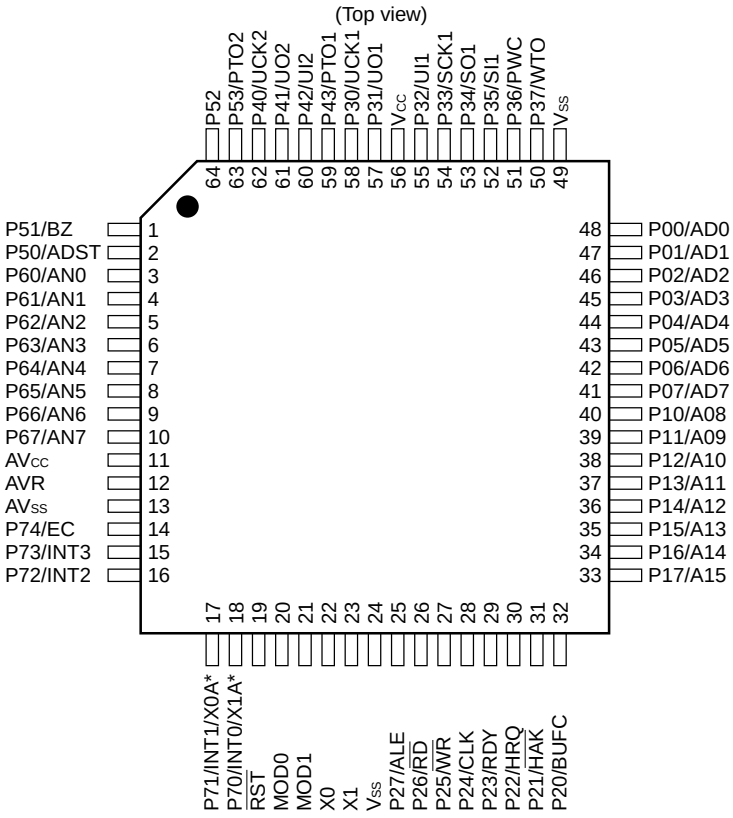
Details	
Product Status	Active
Core Processor	F²MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1486

■ PIN ASSIGNMENT



(DIP-64P-M01)
(MDP-64C-P02)

*: When the dual-clock system is selected.



(FPT-64P-M23)

*: When the dual-clock system is selected.

- **External EPROM pins (MB89PV630 only)**

Pin no.		Pin name	I/O	Function
MDIP	MQFP			
65	66	V_{PP}	O	"H" level output pin
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
84	87	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
85	88	A10	O	Address output pin
86	89	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.

6. OTPROM Option Bit Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single/dual-clock system 1: Dual clock 0: Single clock	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization ($/F_{CH}$) 11: $2^{18}/F_{CH}$ 01: $2^{17}/F_{CH}$ 10: $2^{14}/F_{CH}$ 00: $2^4/F_{CH}$	
0001_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0003_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0004_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0005_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	Vacancy Readable and writable	Vacancy Readable and writable
0006_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Reserved bit Readable and writable

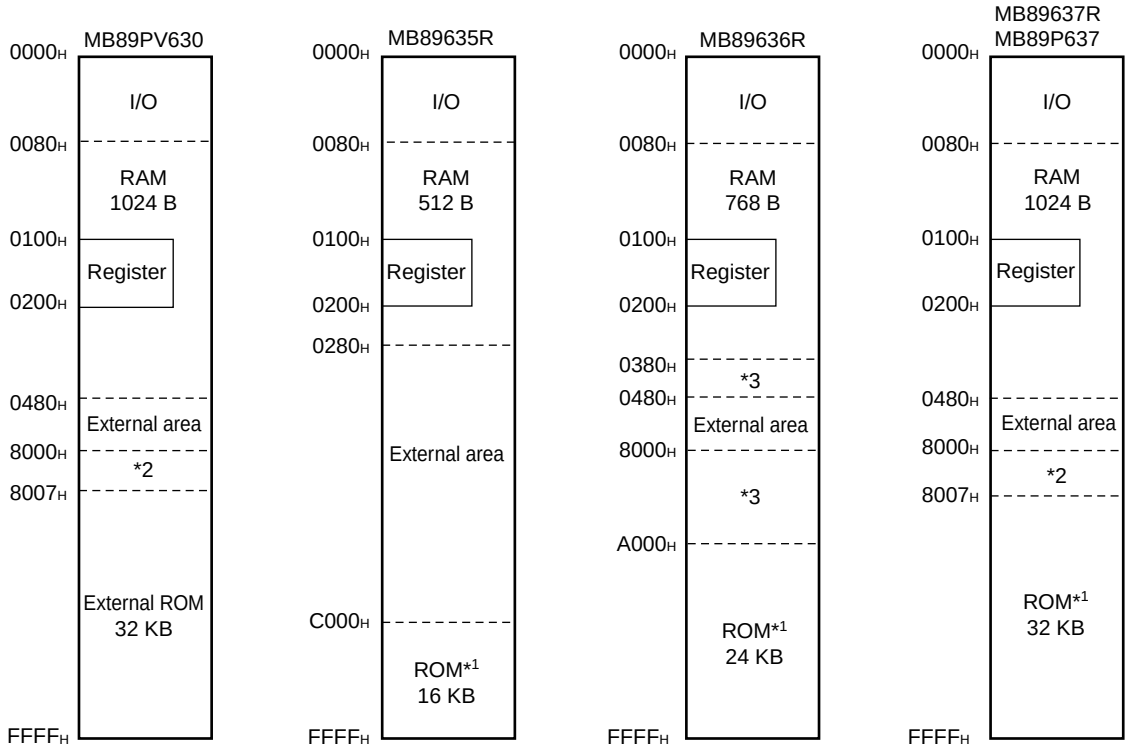
Note: Each bit is set to ‘1’ as the initialized value.

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89630R series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89630R series is structured as illustrated below.

• Memory space



*1: The ROM area is an external area depending on the mode.

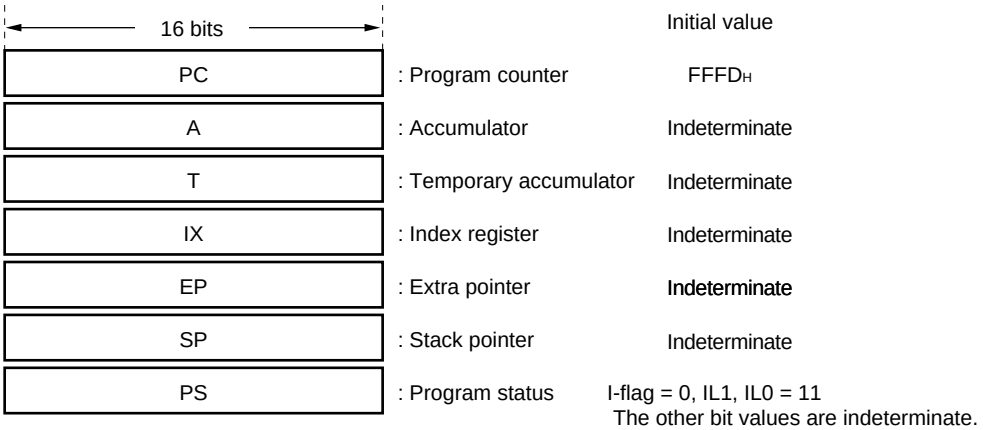
*2: Addresses 8000H to 8006H for the MB89P637 comprise an option area, do not use this area for the MB89PV630 and MB89637R.

*3: The access is forbidden in the external bus mode.

2. Registers

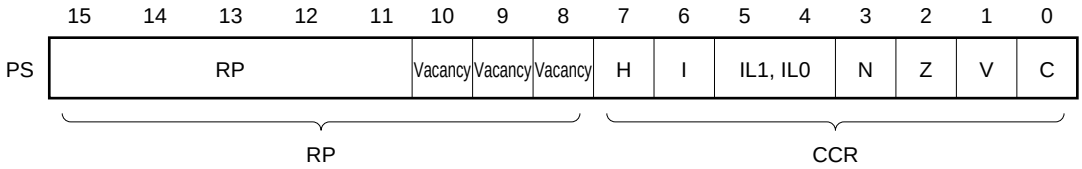
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A16-bit register for index modification
Extra pointer (EP):	A16-bit pointer for indicating a memory address
Stack pointer (SP):	A16-bit register for indicating a stack area
Program status (PS):	A16-bit register for storing a register pointer, a condition code



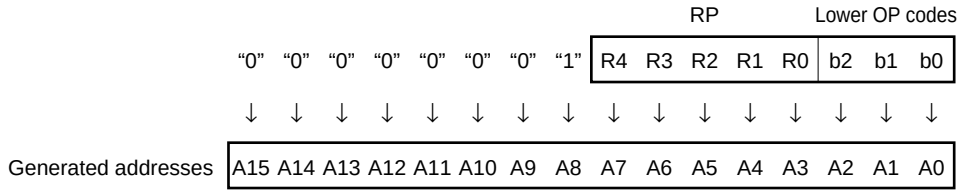
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the program status register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• Rule for conversion of actual addresses of the general-purpose register area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

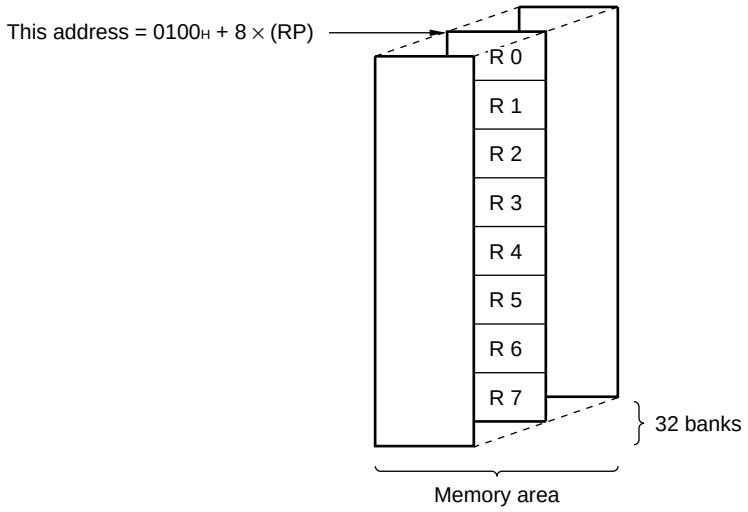
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).

• Register bank configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus pin control register
06H	Vacancy		
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	System clock control register
09H	(R/W)	WDTE	Watchdog timer control register
0AH	(R/W)	TBCR	Timebase timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	CHG3	Port 3 switching register
0DH	(R/W)	PDR3	Port 3 data register
0EH	(W)	DDR3	Port 3 data direction register
0FH	(R/W)	PDR4	Port 4 data register
10H	(W)	DDR4	Port 4 data direction register
11H	(R/W)	BUZR	Buzzer register
12H	(R/W)	PDR5	Port 5 data register
13H	(R/W)	PDR6	Port 6 data register
14H	(R)	PDR7	Port 7 data register
15H	(R/W)	PCR1	PWC pulse width control register 1
16H	(R/W)	PCR2	PWC pulse width control register 2
17H	(R/W)	RLBR	PWC reload buffer register
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH	Vacancy		
1CH	(R/W)	SMR1	Serial mode register
1DH	(R/W)	SDR1	Serial data register
1EH	Vacancy		
1FH	Vacancy		

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20H	(R/W)	ADC1	A/D converter control register 1
21H	(R/W)	ADC2	A/D converter control register 2
22H	(R/W)	ADDH	A/D converter data register (H)
23H	(R/W)	ADDL	A/D converter data register (L)
24H	(R/W)	EIC1	External interrupt control register 1
25H	(R/W)	EIC2	External interrupt control register 2
26H	Vacancy		
27H	Vacancy		
28H	(R/W)	CNTR1	PWM timer control register 1
29H	(R/W)	CNTR2	PWM timer control register 2
2AH	(R/W)	CNTR3	PWM timer control register 3
2BH	(W)	COMR1	PWM timer compare register 1
2CH	(W)	COMR2	PWM timer compare register 2
2DH	(R/W)	SMC	UART serial mode control register
2EH	(R/W)	SRC	UART serial rate control register
2FH	(R/W)	SSD	UART serial status/data register
30H	(R) (W)	SIDR SODR	UART serial input data control register UART serial output data control register
31H to 7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacancy		

Note: Do not use vacancies.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH1}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P51 to P53 with pull-up resistor
	V_{IH2}	P51 to P53		0.7 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42,P50, P72 to P74		0.8 V_{CC}	—	V_{CC} + 0.3	V	P50 with pull-up resistor
	V_{IHS2}	P50, P70, P71		0.8 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P30, P32, P33, P35, P36, P40, P42, P50 to P53, P70 to P74, $\overline{RST}$, MOD0, MOD1		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P50 to P53		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, P50 to P53, P60 to P67, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_A	AV_{CC}	F_{CH} = 10 MHz, when A/D conversion operates.	—	6	—	mA	
	I_{AH}		F_{CH} = 10 MHz, T_A = +25°C, when A/D conversion in a stop.	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not counted.

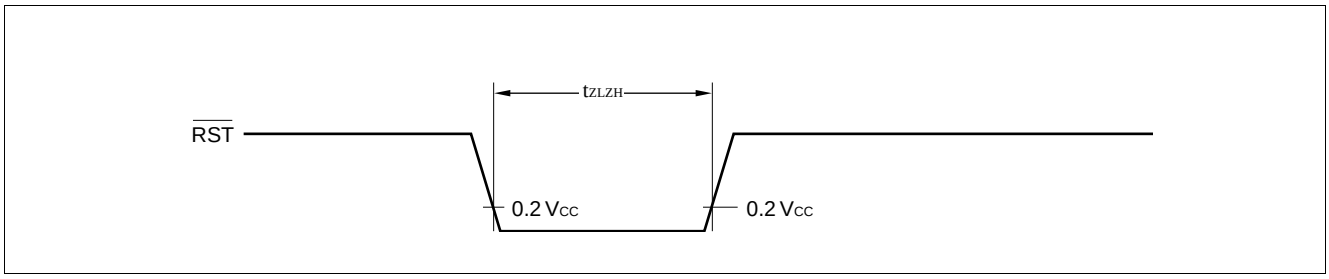
*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics”.

4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ “L” pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	



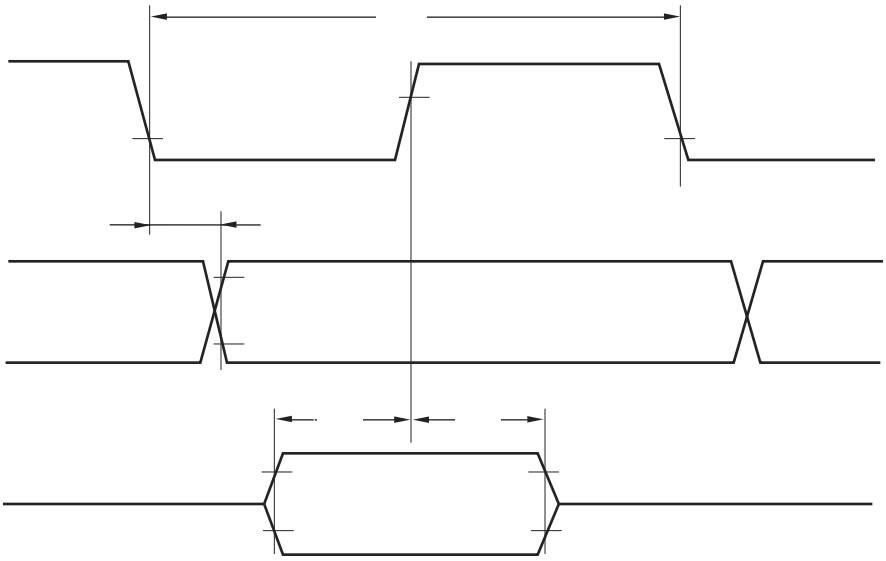
(9) Serial I/O Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

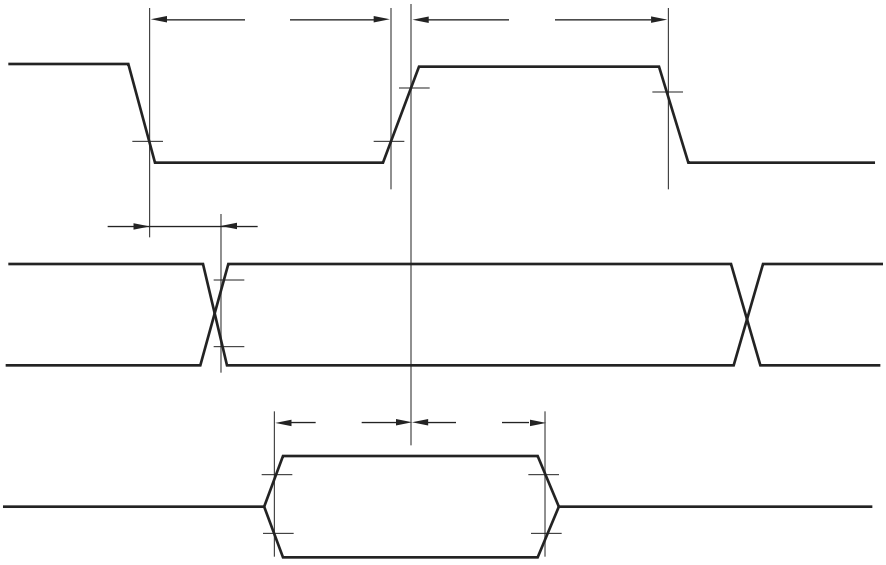
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, UCK1, UCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time UCK1 ↑ → valid UI1 hold time UCK2 ↑ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, UCK1, UCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, UCK1, UCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↓ → valid SI1 hold time UCK1 ↓ → valid UI1 hold time UCK2 ↓ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

• **Internal shift clock mode**

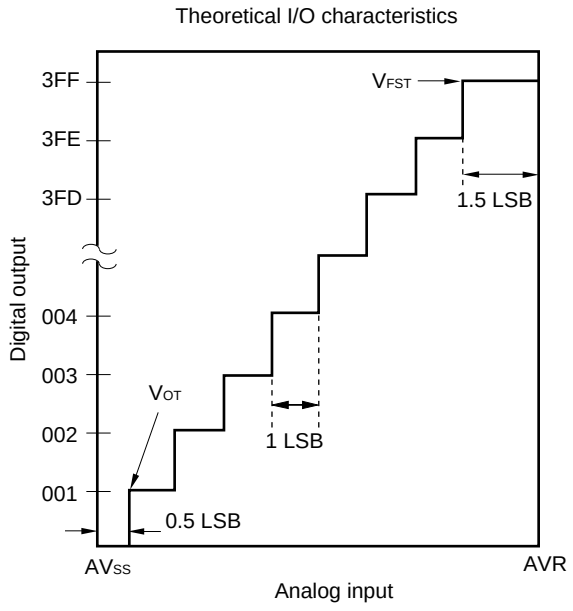


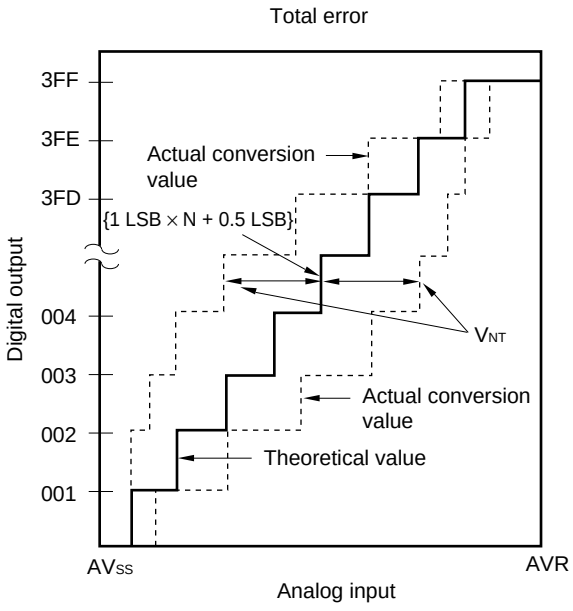
• **External shift clock mode**



6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise





$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

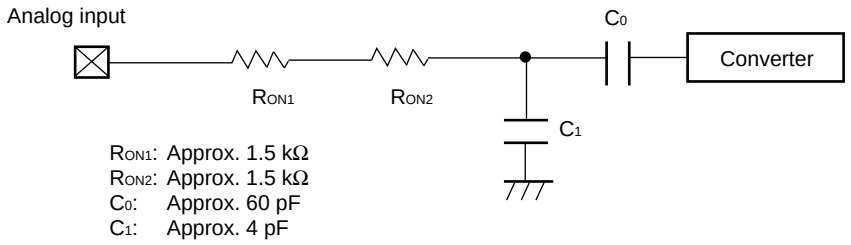
$$\text{Digital output N total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

(Continued)

7. Notes on Using A/D Converter

- **Input impedance of the analog input pins**
  The output impedance of the external circuit for the analog input must satisfy the following conditions.
  If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 kΩ.

- **Analog input circuit model**



R_{ON1}: Approx. 1.5 kΩ
R_{ON2}: Approx. 1.5 kΩ
C_0: Approx. 60 pF
C_1: Approx. 4 pF

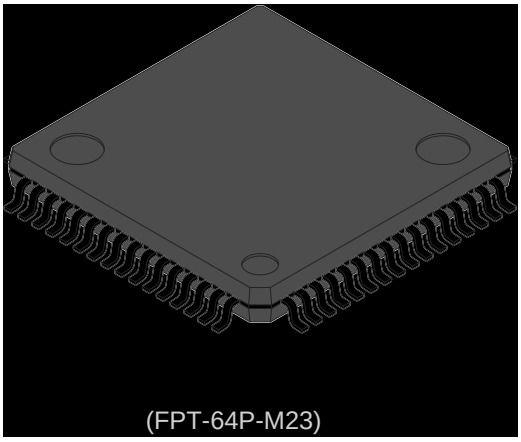
Note: The values mentioned here should be used as a guideline.

- **Error**
  The smaller the | AVR–AVss |, the greater the error would become relatively.

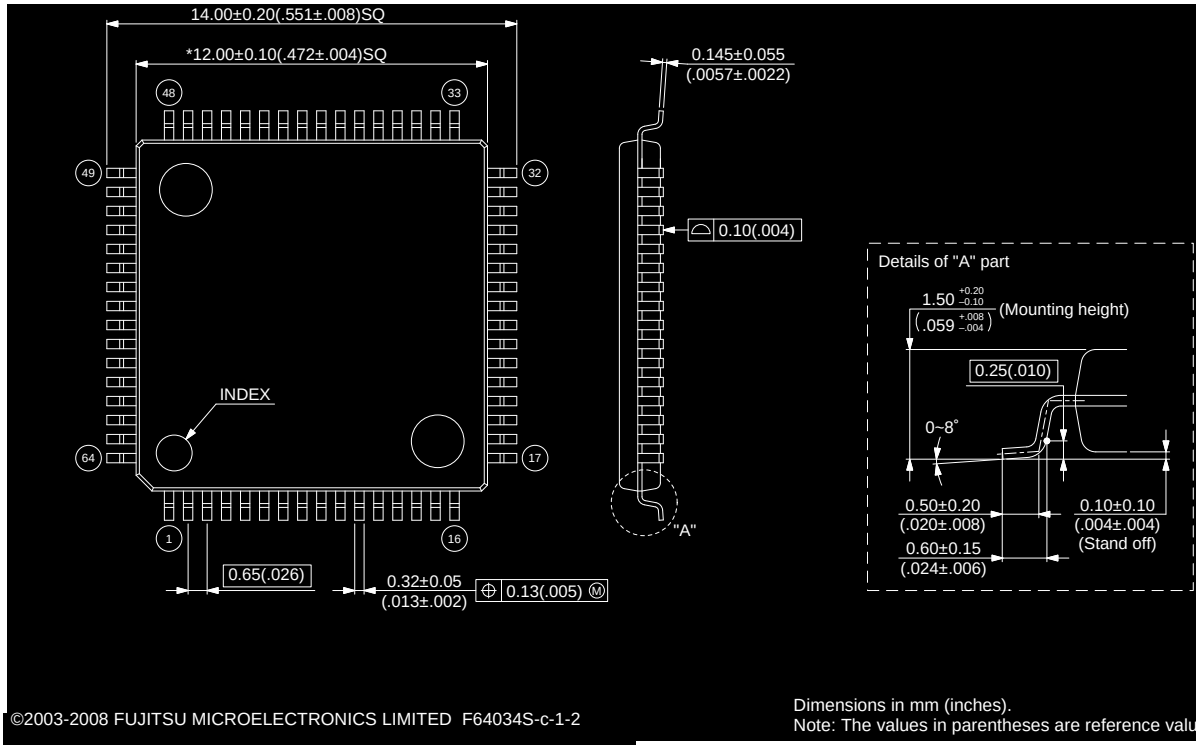
■ MASK OPTIONS

No.	Part number	MB89635R MB89636R MB89637R	MB89P637	MB89PV630
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors 〈 P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Selectable by pin	Can be set per pin*	Fixed to “without pull-up resistor”
2	Power-on reset selection 〈 With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to “with power-on reset”
3	Selection of the main clock oscillation stabilization time (at 10 MHz) 〈 $2^{18}/F_{CH}$ (Approx. 26.2 ms) $2^{17}/F_{CH}$ (Approx. 13.1 ms) $2^{14}/F_{CH}$ (Approx. 1.6 ms) $2^{4}/F_{CH}$ (Approx. 1.6 µs) F_{CH} : Main clock frequency	Selectable	Setting possible	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)
4	Reset pin output 〈 Reset output provided No reset output	Selectable	Setting possible	Fixed to “with reset output”
5	Single/dual-clock system option 〈 Single clock Dual clock	Selectable	Setting possible	MB89PV630-101 Single-clock system MB89PV630-102 Dual-clock systems

* : For P50 to P53, fixed to "Without pull-up resistor."



(FPT-64P-M23)



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

(Continued)

MEMO