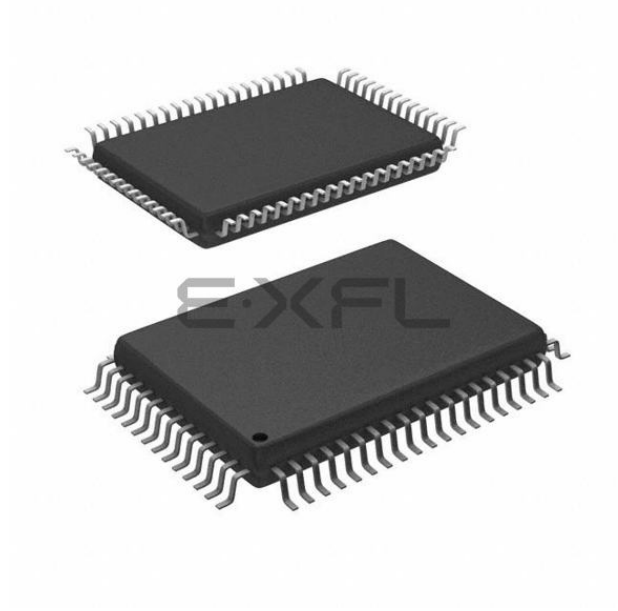

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1487e1

■ PRODUCT LINEUP

Part number / Item	MB89635R	MB89636R	MB89637R	MB89P637	MB89PV630
Classification	Mass-produced products (mask ROM products)			One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (Internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	512 × 8 bits	768 × 8 bits	1024 × 8 bits	1024 × 8 bits	1024 × 8 bits
CPU functions	The number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs/10 MHz, 61 µs@32.768 kHz Interrupt processing time: 3.6 to 57.6 µs/10 MHz, 562.5 µs@32.768 kHz				
Ports	Input ports: 5 (All also serve as peripherals.) Output ports (N-ch open-drain): 8 (All also serve as peripherals.) I/O ports (N-ch open-drain): 4 (All also serve as peripherals.) Output ports (CMOS): 8 (All also serve as bus control.) I/O ports (CMOS): 28 (27 ports also serve as bus pins and peripherals.) Total: 53				
Watch timer	21 bits × 1 (in main clock)/15 bits × 1 (at 32.768 kHz)				
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 3.3 ms) × 2 channels 7/8-bit resolution PWM operation (conversion cycle: 51.2 µs to 839 ms) × 2 channels				
8-bit pulse width count timer	8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 µs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 µs) 8-bit pulse width measurement operation (capable of continuous measurement, and measurement of "H" pulse width/ "L" pulse width/ from ↑ to ↑/from ↓ to ↓)				
16-bit timer/ counter	16-bit timer operation (operating clock cycle: 0.4 µs) 16-bit event counter operation (rising edge/falling edge/both edge selectable)				
8-bit serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)				
UART	Capable of switching two I/O systems by software Transfer data length (6, 7, and 8 bits) Transfer rate (300 to 62500 bps. at 10 MHz oscillation)				
10-bit A/D converter	10-bit resolution × 8 channels A/D conversion mode (conversion time: 13.2 µs) Sense mode (conversion time: 7.2 µs) Capable of continuous activation by an external activation or an internal timer				

(Continued)

- Other specifications
  Both MB89630 series and MB89635R/636R/637R is the same.
- Electrical specifications/electrical characteristics
  Electrical specifications of the MB89635R/636R/637R series are the same as that of the MB89630 series.
  Electrical characteristics of both the series are much the same.

■ CORRESPONDENCE BETWEEN THE MB89630 AND MB89630R SERIES

- The MB89630R series is the reduction version of the MB89630 series.
- The the MB89630 and MB89630R series consist of the following products:

MB89630 series	MB89635	MB89636	MB89637	MB89P637	MB89PV630
MB89630R series	MB89635R	MB89636R	MB89637R		

■ PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
30	22	23	X0	A	Main clock crystal oscillator pins
31	23	24	X1		
28	20	21	MOD0	D	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
29	21	22	MOD1		
27	19	20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
56 to 49	48 to 41	49 to 42	P00/AD0 to P07/AD7	F	General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.
48 to 41	40 to 33	41 to 34	P10/A08 to P17/A157	F	General-purpose I/O ports When an external bus is used, these ports function as an upper address output.
40	32	33	P20/BUFC	H	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	31	32	P21/$\overline{HAK}$	H	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.
38	30	31	P22/HRQ	F	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	29	30	P23/RDY	F	General-purpose output port When an external bus is used, this port functions as a ready input.
36	28	29	P24/CLK	H	General-purpose output port When an external bus is used, this port functions as a clock output.
35	27	28	P25/$\overline{WR}$	H	General-purpose output port When an external bus is used, this port functions as a write signal output.
34	26	27	P26/$\overline{RD}$	H	General-purpose output port When an external bus is used, this port functions as a read signal output.

*1: DIP-64P-M01
*2: MDP-64C-P02
*3: FPT-64P-M23
*4: FPT-64P-M06
*5: MQP-M64C-P01

(Continued)

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.

■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus pin control register
06H	Vacancy		
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	System clock control register
09H	(R/W)	WDTE	Watchdog timer control register
0AH	(R/W)	TBCR	Timebase timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	CHG3	Port 3 switching register
0DH	(R/W)	PDR3	Port 3 data register
0EH	(W)	DDR3	Port 3 data direction register
0FH	(R/W)	PDR4	Port 4 data register
10H	(W)	DDR4	Port 4 data direction register
11H	(R/W)	BUZR	Buzzer register
12H	(R/W)	PDR5	Port 5 data register
13H	(R/W)	PDR6	Port 6 data register
14H	(R)	PDR7	Port 7 data register
15H	(R/W)	PCR1	PWC pulse width control register 1
16H	(R/W)	PCR2	PWC pulse width control register 2
17H	(R/W)	RLBR	PWC reload buffer register
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH	Vacancy		
1CH	(R/W)	SMR1	Serial mode register
1DH	(R/W)	SDR1	Serial data register
1EH	Vacancy		
1FH	Vacancy		

(Continued)

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH1}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P51 to P53 with pull-up resistor
	V_{IH2}	P51 to P53		0.7 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42,P50, P72 to P74		0.8 V_{CC}	—	V_{CC} + 0.3	V	P50 with pull-up resistor
	V_{IHS2}	P50, P70, P71		0.8 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P30, P32, P33, P35, P36, P40, P42, P50 to P53, P70 to P74, $\overline{RST}$, MOD0, MOD1		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P50 to P53		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, P50 to P53, P60 to P67, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89635R/ 636R/637R/ PV630
				—	1.5	2.5	mA	MB89P637
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89635R/ 636R/637R/ PV630
				—	500	700	µA	MB89P637
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_A	AV_{CC}	F_{CH} = 10 MHz, when A/D conversion operates.	—	6	—	mA	
	I_{AH}		F_{CH} = 10 MHz, T_A = +25°C, when A/D conversion in a stop.	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not counted.

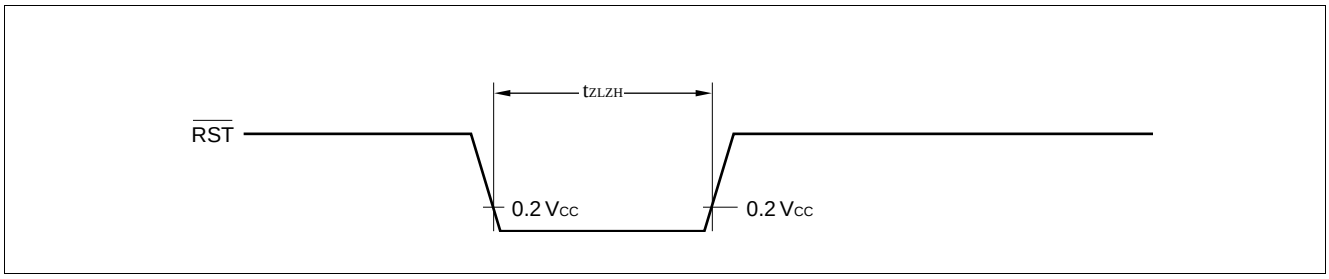
*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics”.

4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ “L” pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	



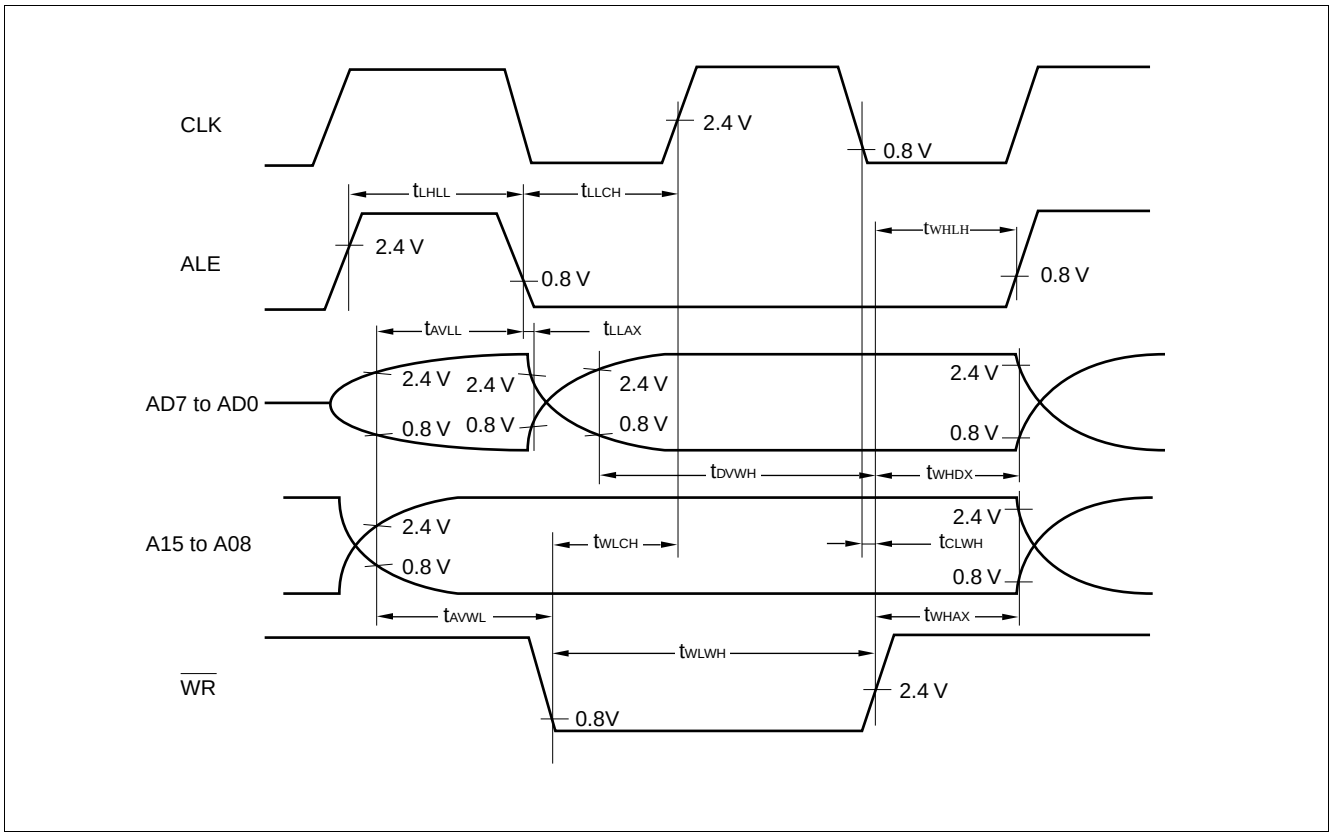
(7) Bus Write Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to AD0, ALE A15 to A08	—	1/4 t_{inst}*1 – 64 ns*2	—	µs	
ALE ↓ time → address loss time	t_{LLAX}			5	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 60 ns*2	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*1 – 20 ns*2	—	µs	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to AD0, $\overline{WR}$		1/2 t_{inst}*1 – 60 ns*2	—	µs	
$\overline{WR}$ ↑ → address loss time	t_{WHAX}	$\overline{WR}$, A15 to A08		1/4 t_{inst}*1 – 40 ns*2	—	µs	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to AD0, $\overline{WR}$		1/4 t_{inst}*1 – 40 ns*2	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 40 ns*2	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*1 – 40 ns*2	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}			0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*1 – 35 ns*2	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE,CLK		1/4 t_{inst}*1 – 30 ns*2	—	µs	

*1: For information on t_{inst}, see “(4) Instruction Cycle”.

*2: This characteristics are also applicable to the bus read timing.

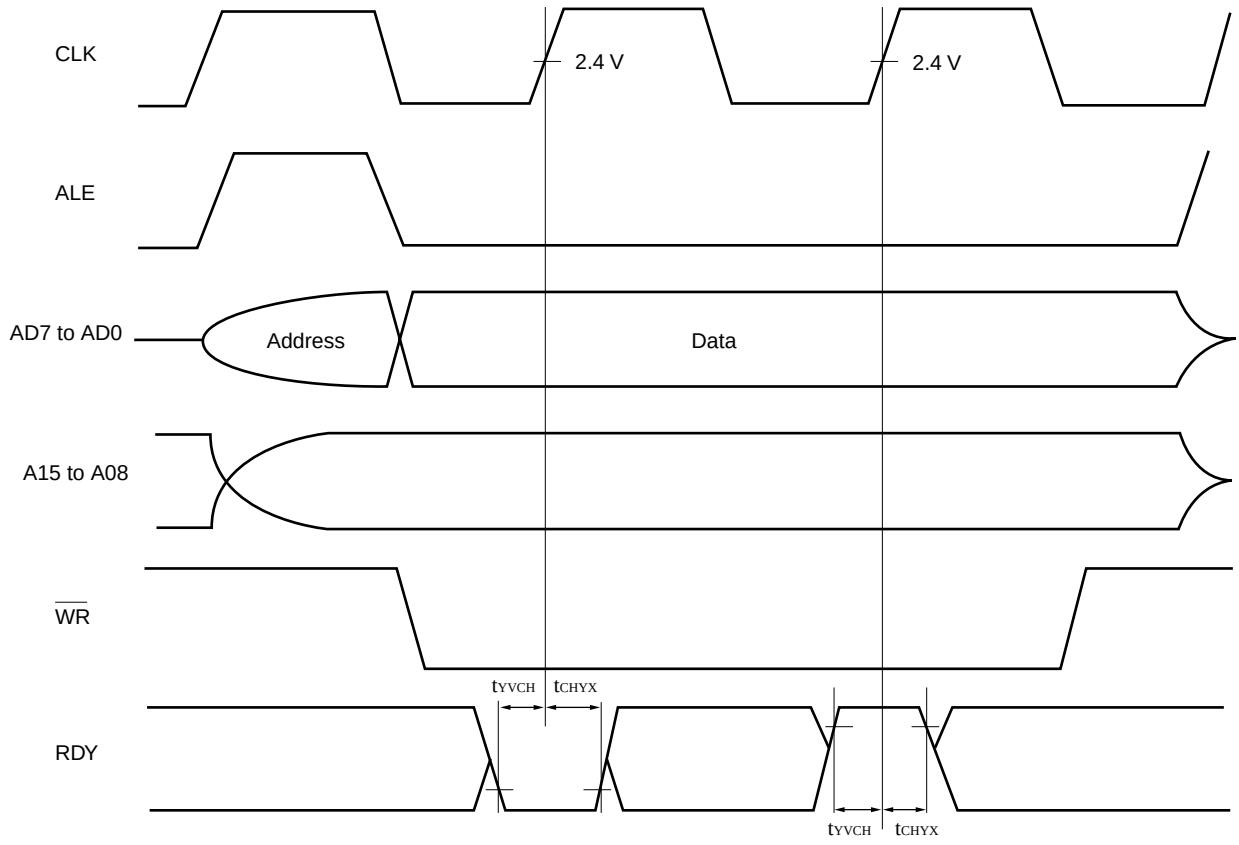


(8) Ready Input Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY loss time	t_{CHYX}			0	—	ns	*

* : This characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

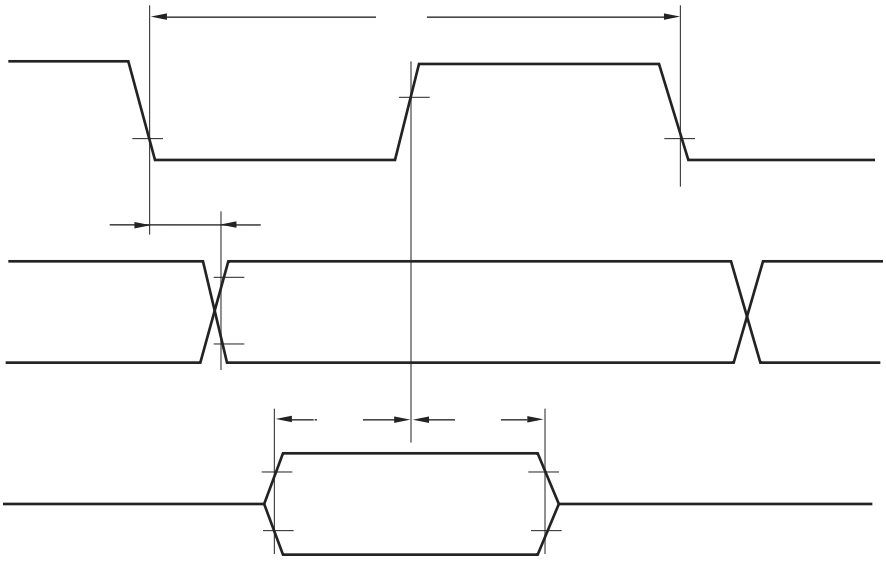
(9) Serial I/O Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

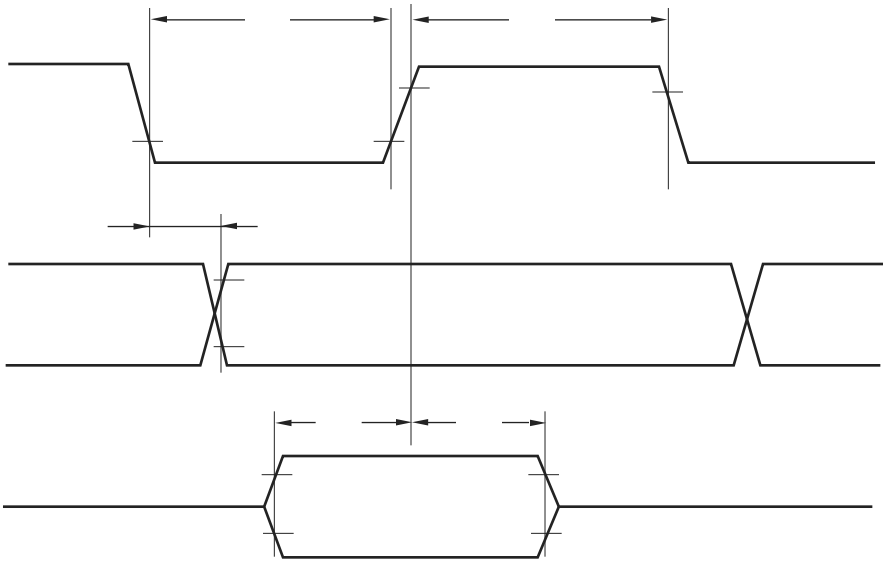
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, UCK1, UCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time UCK1 ↑ → valid UI1 hold time UCK2 ↑ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, UCK1, UCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, UCK1, UCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↓ → valid SI1 hold time UCK1 ↓ → valid UI1 hold time UCK2 ↓ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

• **Internal shift clock mode**

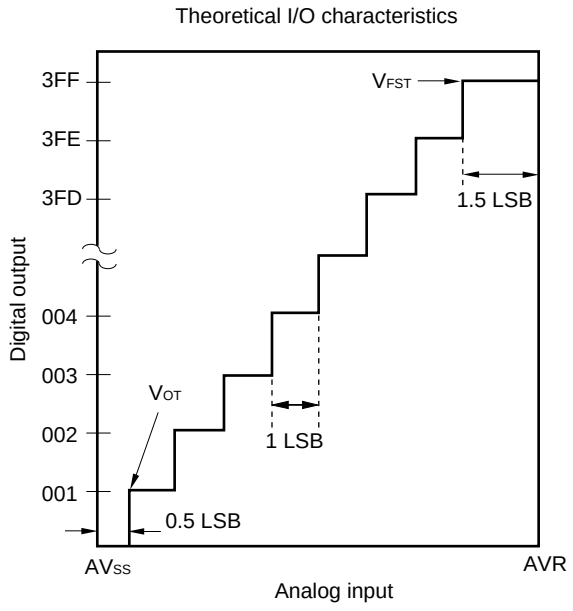


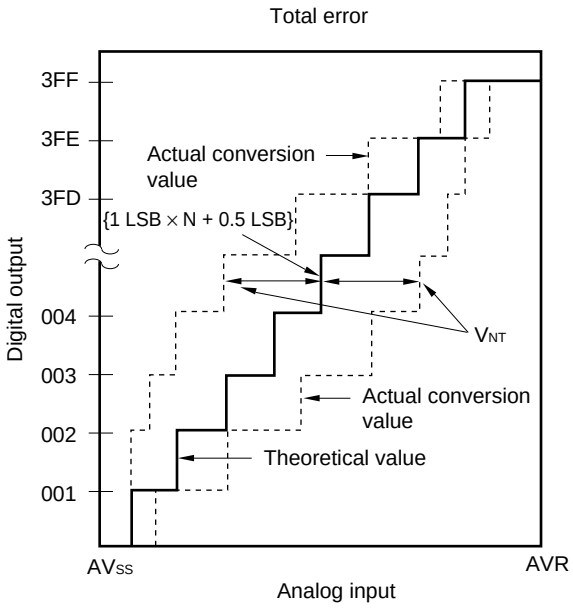
• **External shift clock mode**



6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise





$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

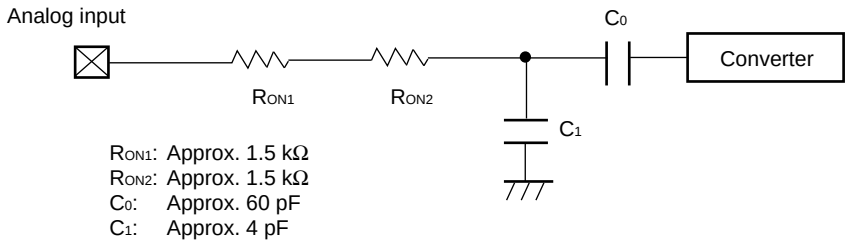
$$\text{Digital output N total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

(Continued)

7. Notes on Using A/D Converter

- **Input impedance of the analog input pins**
  The output impedance of the external circuit for the analog input must satisfy the following conditions.
  If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 kΩ.

- **Analog input circuit model**



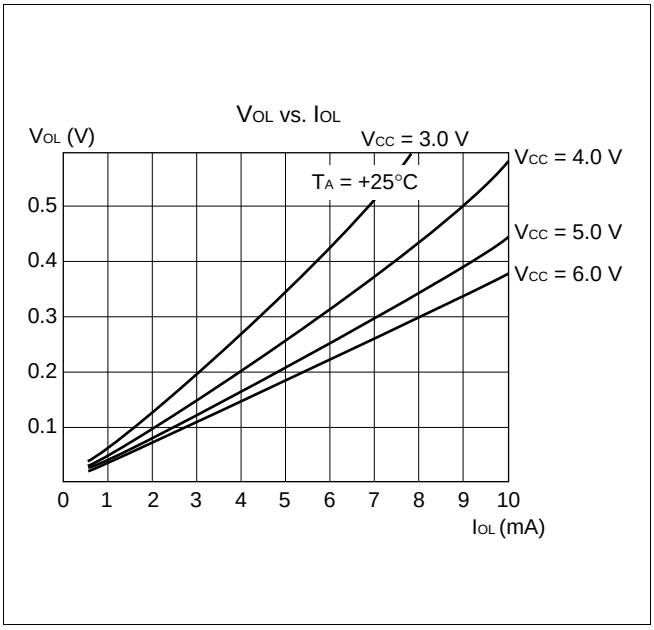
R_{ON1}: Approx. 1.5 kΩ
R_{ON2}: Approx. 1.5 kΩ
C_0: Approx. 60 pF
C_1: Approx. 4 pF

Note: The values mentioned here should be used as a guideline.

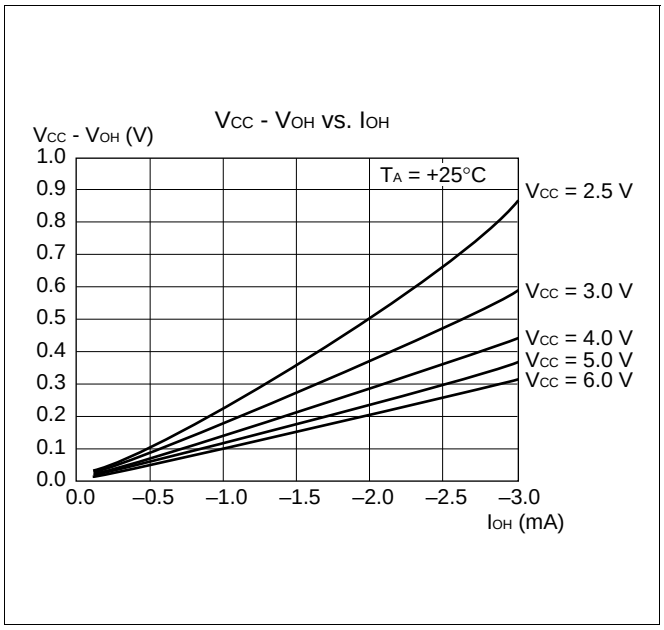
- **Error**
  The smaller the | AVR–AVss |, the greater the error would become relatively.

■ CHARACTERISTICS EXAMPLE

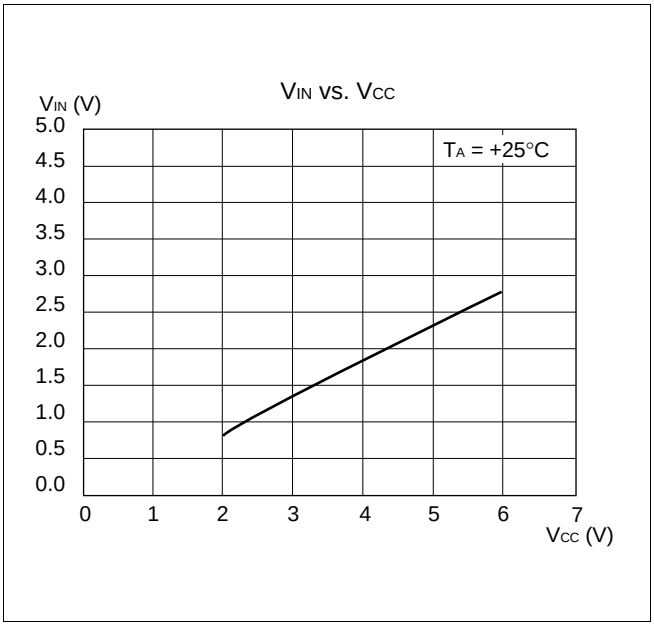
(1) “L” Level Output Voltage



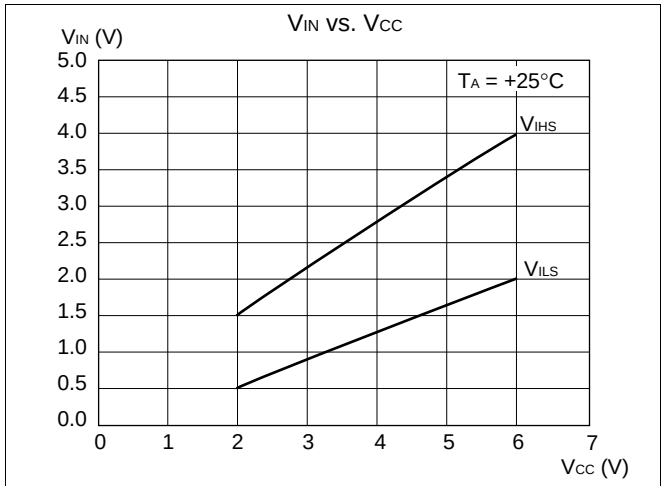
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



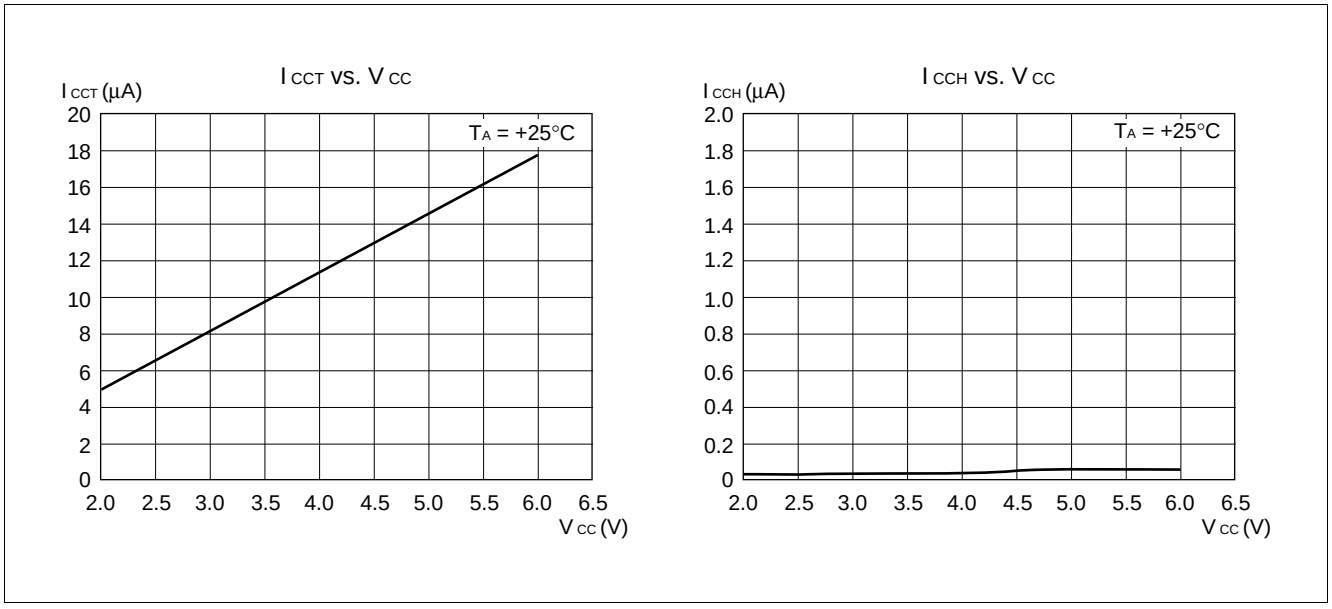
(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)



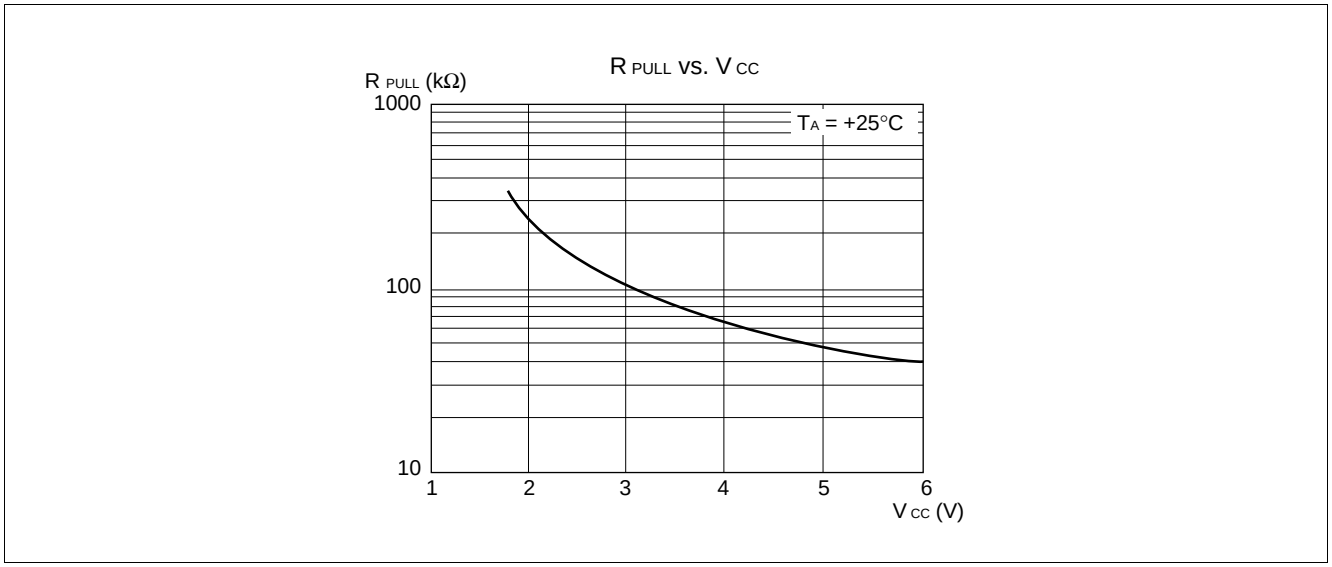
V_{IHS}: Threshold as the input voltage in hysteresis characteristics is set to “H” level

V_{ILS}: Threshold as the input voltage in hysteresis characteristics is set to “L” level

(Continued)



(6) Pull-up Resistance

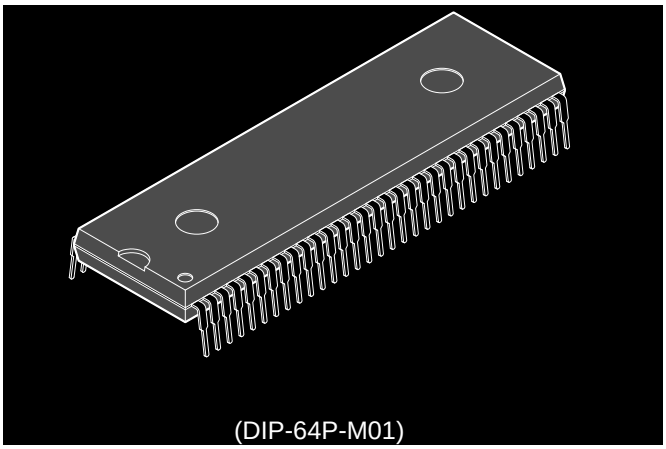


■ MASK OPTIONS

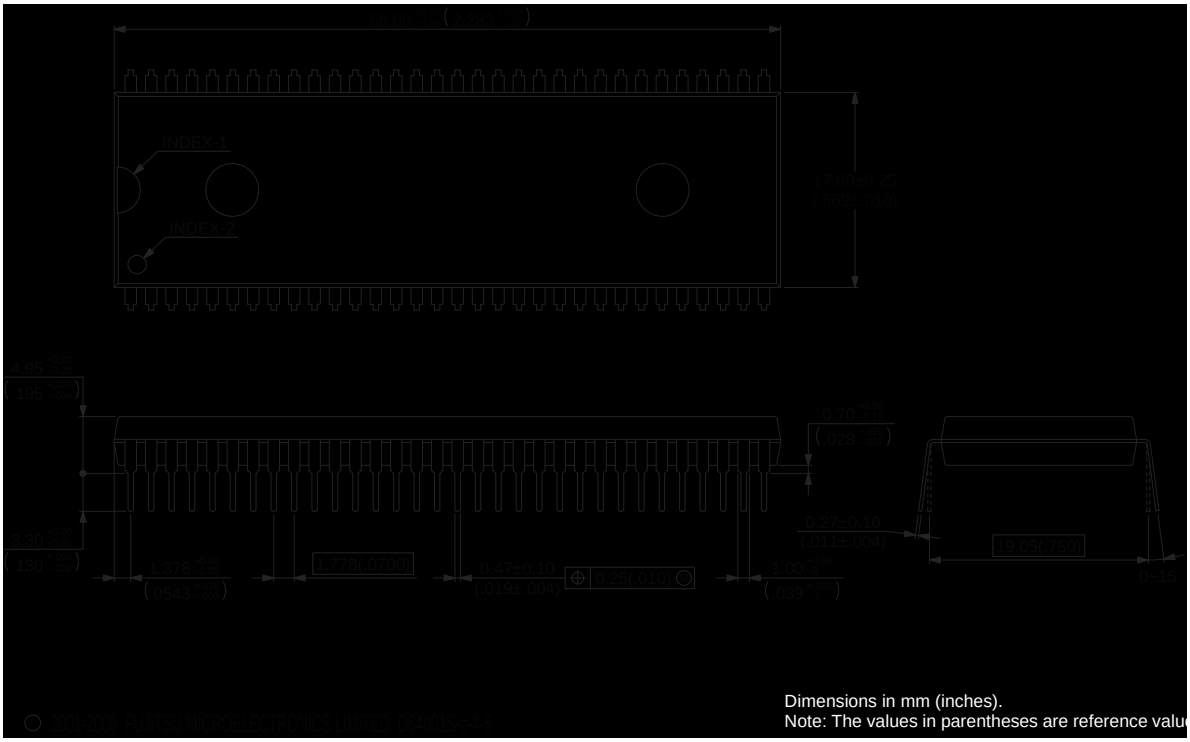
No.	Part number	MB89635R MB89636R MB89637R	MB89P637	MB89PV630
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors 〈 P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Selectable by pin	Can be set per pin*	Fixed to “without pull-up resistor”
2	Power-on reset selection 〈 With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to “with power-on reset”
3	Selection of the main clock oscillation stabilization time (at 10 MHz) 〈 $2^{18}/F_{CH}$ (Approx. 26.2 ms) $2^{17}/F_{CH}$ (Approx. 13.1 ms) $2^{14}/F_{CH}$ (Approx. 1.6 ms) $2^{4}/F_{CH}$ (Approx. 1.6 µs) F_{CH} : Main clock frequency	Selectable	Setting possible	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)
4	Reset pin output 〈 Reset output provided No reset output	Selectable	Setting possible	Fixed to “with reset output”
5	Single/dual-clock system option 〈 Single clock Dual clock	Selectable	Setting possible	MB89PV630-101 Single-clock system MB89PV630-102 Dual-clock systems

* : For P50 to P53, fixed to "Without pull-up resistor."

■ PACKAGE DIMENSIONS



(DIP-64P-M01)



Dimensions in mm (inches).
Note: The values in parentheses are reference valu

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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MEMO

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