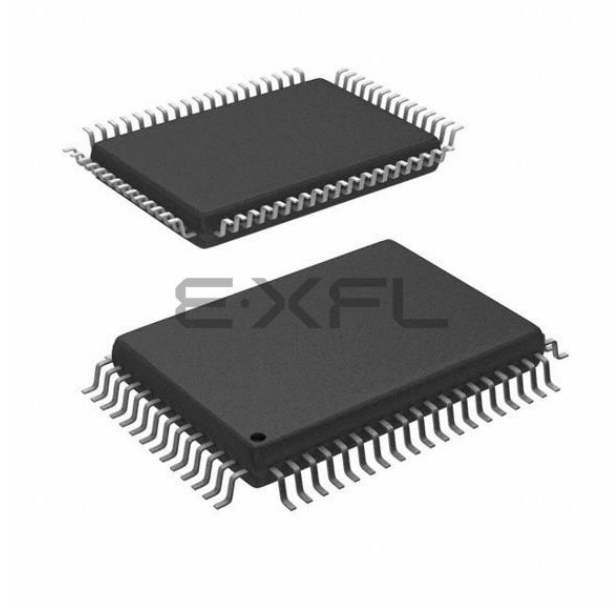
Infineon Technologies - MB89635RPF-G-1489E1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8L
Core Size	8-Bit
Speed	10MHz
Connectivity	EBI/EMI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	16KB (16K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb89635rpf-g-1489e1

(Continued)

- UART
  CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  Start by an external input capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Bus interface function
  With hold and ready function

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P637, the program area starts from address 8007_H but on the MB89PV630 and MB89637R starts from 8000_H.

  (On the MB89P637, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637R, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637.)
- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM. However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics".)

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options".

Take particular care on the following points:

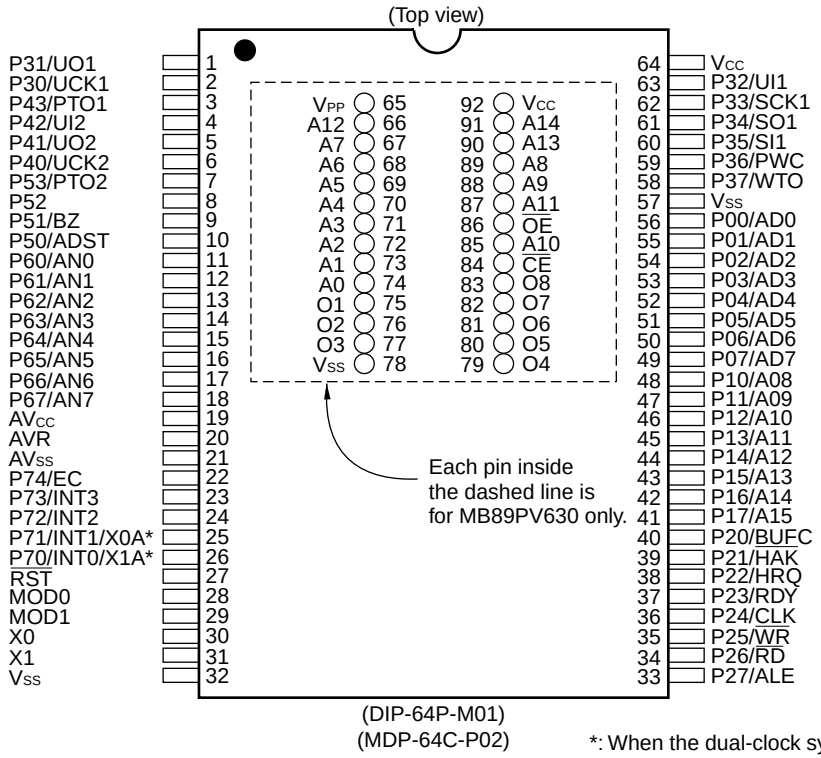
- A pull-up resistor cannot be set for P50 to P53 on the MB89P637.
- Options are fixed on the MB89PV630.

4. Differences between the MB89630 and MB89630R Series

- Memory access area
  There are no difference between the access area of MB89635/MB89635R, and that of MB89637/MB89637R. The access area of MB89636 is different from that of the MB89636R when using in external bus mode.

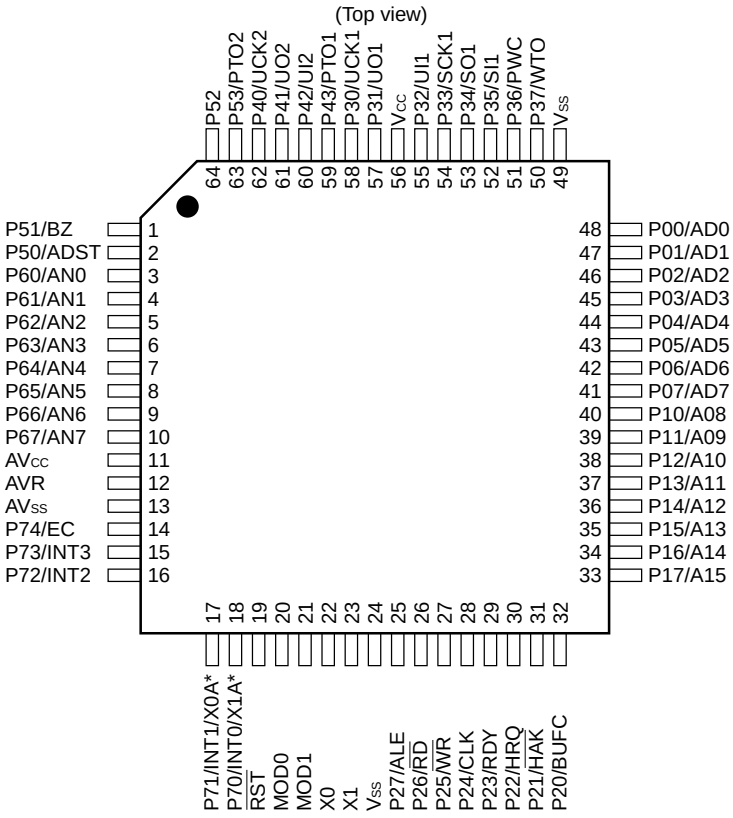
Address	Memory area	
	MB89636	MB89636R
0000_H to $007F_H$	I/O area	I/O area
0080_H to $037F_H$	RAM area	RAM area
0380_H to $047F_H$	External area	Access prohibited
0480_H to $7FFF_H$		External area
8000_H to $9FFF_H$		Access prohibited
$A000_H$ to $FFFF_H$	ROM area	ROM area

■ PIN ASSIGNMENT



(DIP-64P-M01)
(MDP-64C-P02)

*: When the dual-clock system is selected.



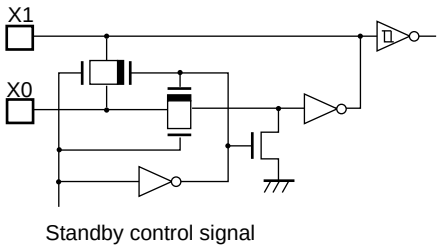
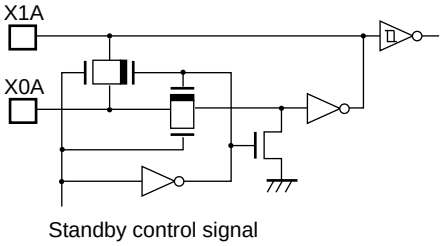
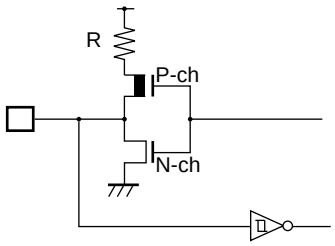
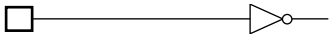
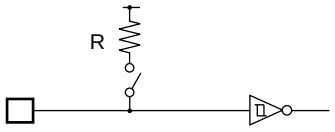
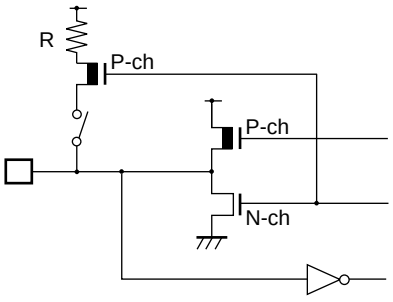
(FPT-64P-M23)

*: When the dual-clock system is selected.

- **External EPROM pins (MB89PV630 only)**

Pin no.		Pin name	I/O	Function
MDIP	MQFP			
65	66	V_{PP}	O	"H" level output pin
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
84	87	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
85	88	A10	O	Address output pin
86	89	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) External clock input selection versions of MB89PV630, MB89P637, MB89635R, MB89636R, and MB89637R At an oscillation feedback resistor of approximately 1 MΩ@5.0 V
B		• Crystal or ceramic oscillation type (subclock) MB89PV630, MB89P637, MB89635R, MB89636R, and MB89637R with dual-clock system At an oscillation feedback resistor of approximately 4.5 MΩ@5.0 V
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ@5.0 V • Hysteresis input
D		
E		• Hysteresis input • Pull-up resistor optional (except P70 and P71)
F		• CMOS output • CMOS input • Pull-up resistor optional (except P22 and P23)

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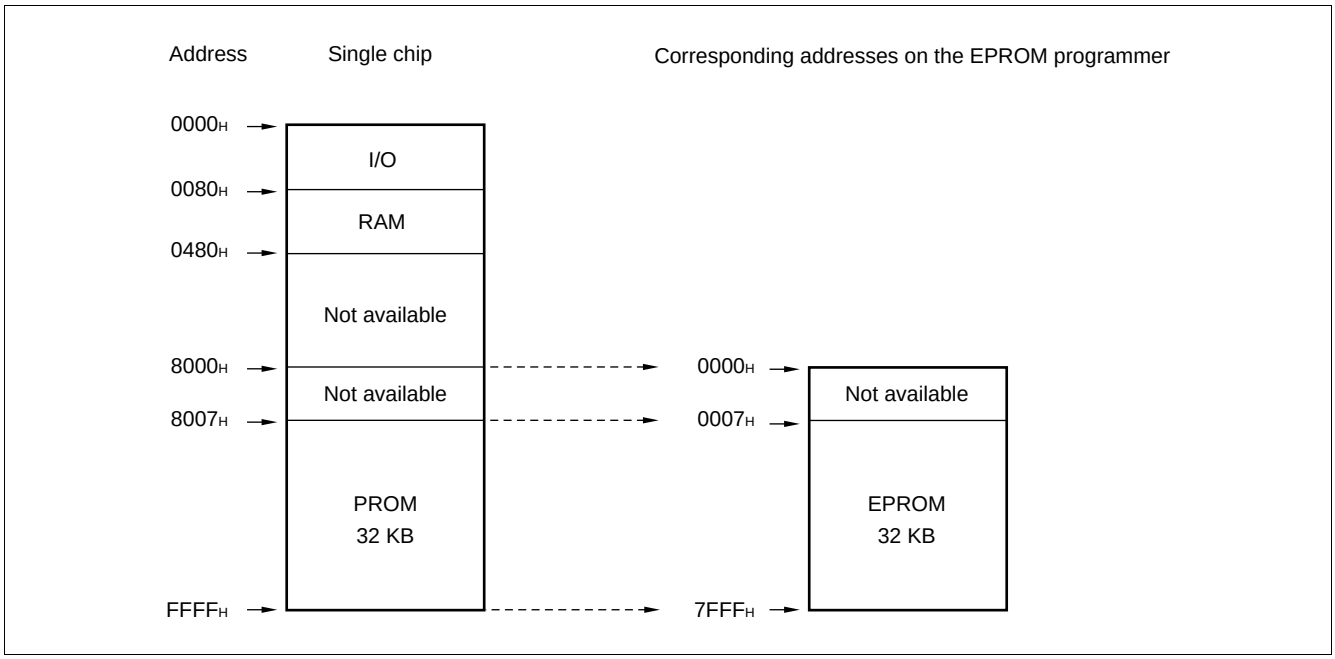
■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20CZ, MBM27C256A-20TV

2. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

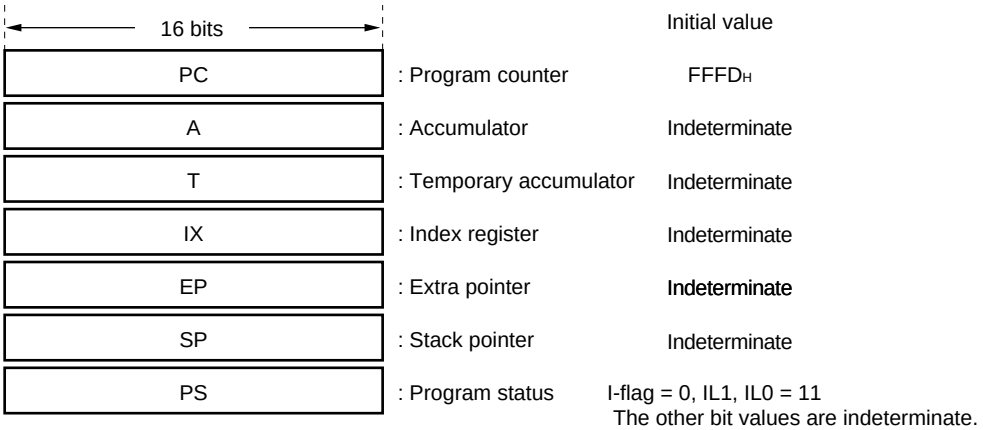
(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

2. Registers

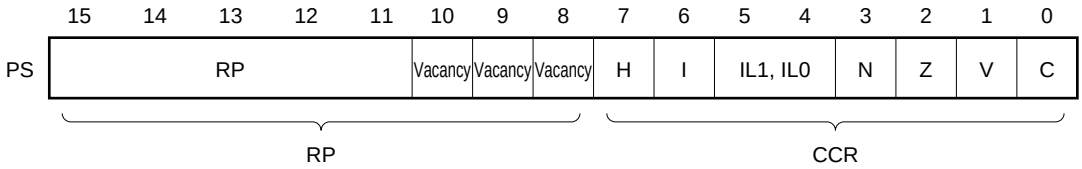
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A16-bit register for index modification
Extra pointer (EP):	A16-bit pointer for indicating a memory address
Stack pointer (SP):	A16-bit register for indicating a stack area
Program status (PS):	A16-bit register for storing a register pointer, a condition code



The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the program status register



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus pin control register
06H	Vacancy		
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	System clock control register
09H	(R/W)	WDTE	Watchdog timer control register
0AH	(R/W)	TBCR	Timebase timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	CHG3	Port 3 switching register
0DH	(R/W)	PDR3	Port 3 data register
0EH	(W)	DDR3	Port 3 data direction register
0FH	(R/W)	PDR4	Port 4 data register
10H	(W)	DDR4	Port 4 data direction register
11H	(R/W)	BUZR	Buzzer register
12H	(R/W)	PDR5	Port 5 data register
13H	(R/W)	PDR6	Port 6 data register
14H	(R)	PDR7	Port 7 data register
15H	(R/W)	PCR1	PWC pulse width control register 1
16H	(R/W)	PCR2	PWC pulse width control register 2
17H	(R/W)	RLBR	PWC reload buffer register
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH	Vacancy		
1CH	(R/W)	SMR1	Serial mode register
1DH	(R/W)	SDR1	Serial data register
1EH	Vacancy		
1FH	Vacancy		

(Continued)

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Address	Read/write	Register name	Register description
20H	(R/W)	ADC1	A/D converter control register 1
21H	(R/W)	ADC2	A/D converter control register 2
22H	(R/W)	ADDH	A/D converter data register (H)
23H	(R/W)	ADDL	A/D converter data register (L)
24H	(R/W)	EIC1	External interrupt control register 1
25H	(R/W)	EIC2	External interrupt control register 2
26H	Vacancy		
27H	Vacancy		
28H	(R/W)	CNTR1	PWM timer control register 1
29H	(R/W)	CNTR2	PWM timer control register 2
2AH	(R/W)	CNTR3	PWM timer control register 3
2BH	(W)	COMR1	PWM timer compare register 1
2CH	(W)	COMR2	PWM timer compare register 2
2DH	(R/W)	SMC	UART serial mode control register
2EH	(R/W)	SRC	UART serial rate control register
2FH	(R/W)	SSD	UART serial status/data register
30H	(R) (W)	SIDR SODR	UART serial input data control register UART serial output data control register
31H to 7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacancy		

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*
A/D converter reference input voltage	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AVR must not exceed "AV_{CC} + 0.3 V".
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P50 to P53
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P50 to P53
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P50 to P53
	V_{O2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P50 to P53
"L" level maximum output current	I_{OL}	—	20	mA	
"L" level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH}	—	–20	mA	
"H" level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	ΣI_{OH}	—	–50	mA	
"H" level total average output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

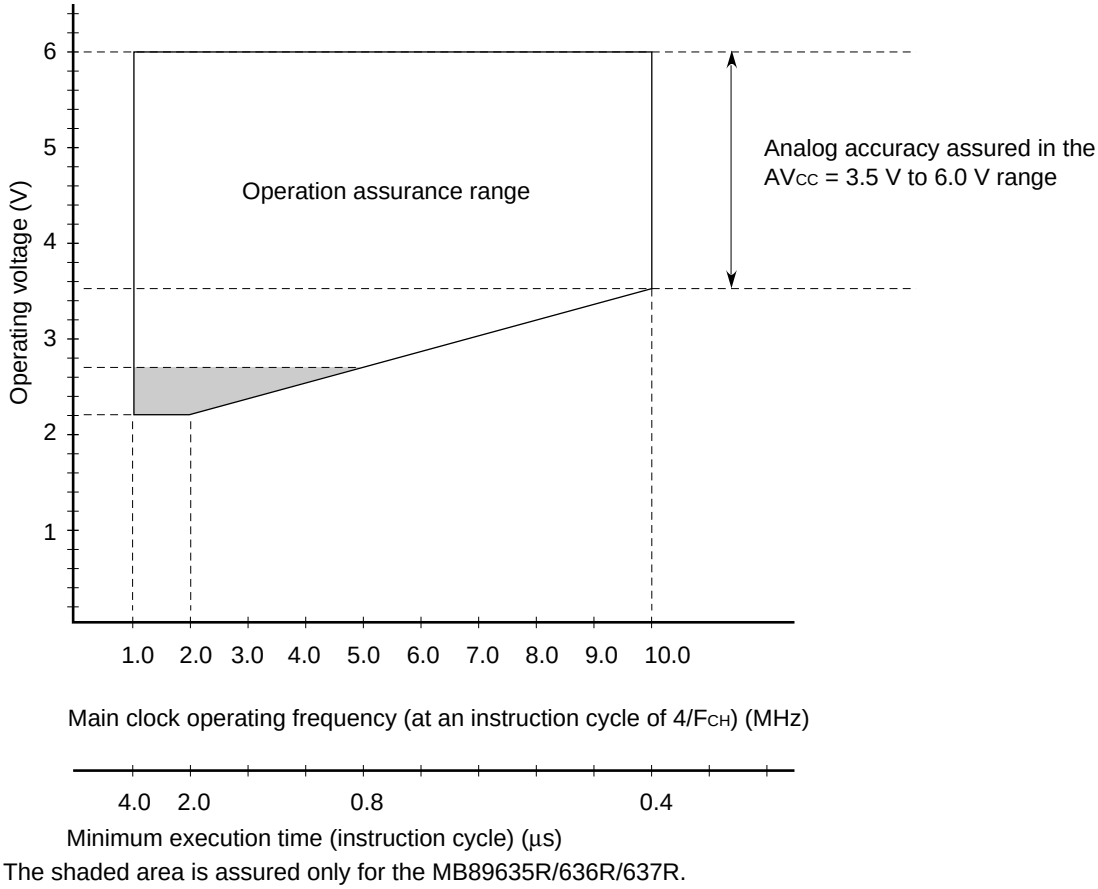
2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89635R/636R/637R
		2.7*	6.0*	V	Normal operation assurance range* MB89PV630/P637
	AV_{CC}	1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	3.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and “5. A/D Converter Electrical Characteristics”.

Figure 1 Operating Voltage vs. Main Clock Operating Frequency



Note: The shaded area is assured only for the MB89635R/636R/637R.

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_{CH}.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH1}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P51 to P53 with pull-up resistor
	V_{IH2}	P51 to P53		0.7 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42,P50, P72 to P74		0.8 V_{CC}	—	V_{CC} + 0.3	V	P50 with pull-up resistor
	V_{IHS2}	P50, P70, P71		0.8 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P30, P32, P33, P35, P36, P40, P42, P50 to P53, P70 to P74, $\overline{RST}$, MOD0, MOD1		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P50 to P53		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, P50 to P53, P60 to P67, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89635R/ 636R/637R/ PV630
				—	1.5	2.5	mA	MB89P637
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89635R/ 636R/637R/ PV630
				—	500	700	µA	MB89P637
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	

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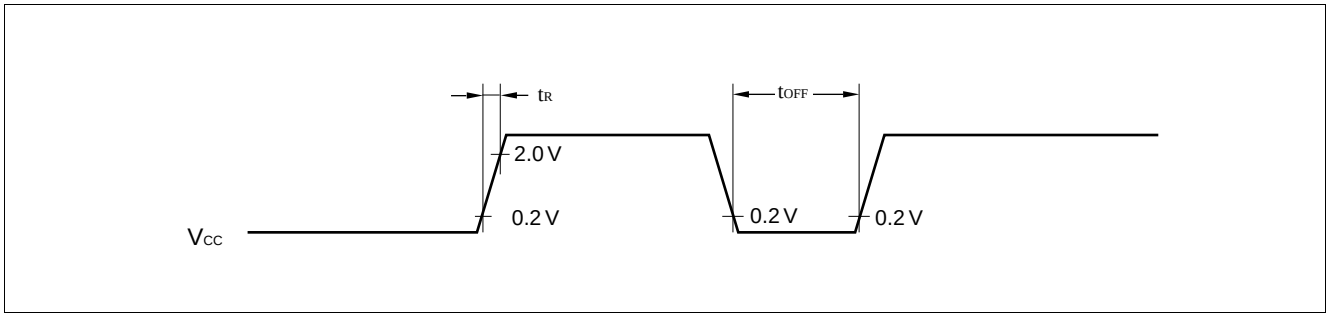
(2) Specification for Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Min. interval time for the next power-on reset

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



(3) Clock Timing

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

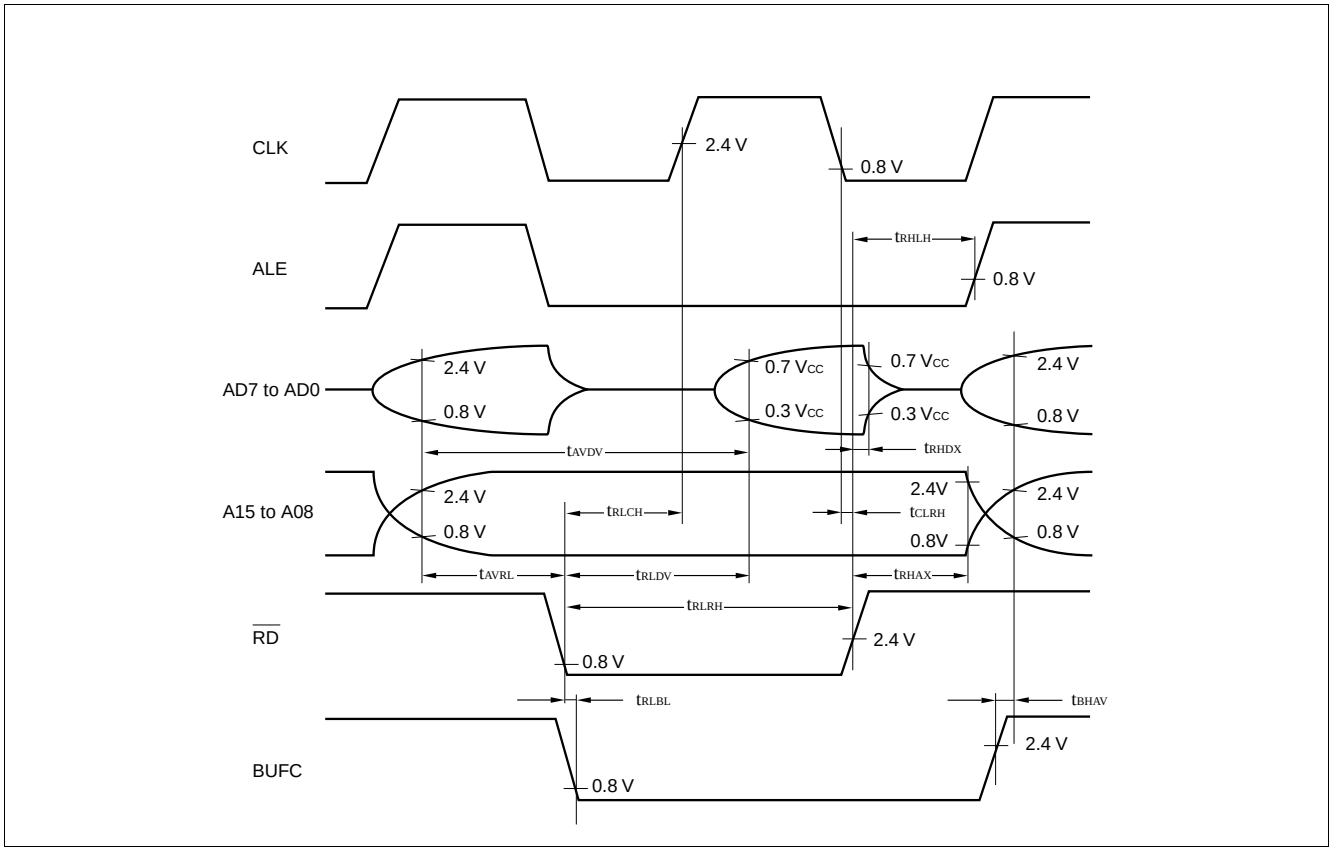
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	External clock
Input clock rising/ falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

(6) Bus Read Timing

(V_{CC} = 5.0 V±10%, 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to A08, AD7 to AD0	—	1/4 t_{inst}*– 64 ns	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst}*– 20 ns	—	µs	
Valid address → data read time	t_{AVDV}	AD7 to AD0, A15 to A08		1/2 t_{inst}*	200	µs	No wait
$\overline{RD}$ ↓ → data read time	t_{RLDV}	$\overline{RD}$, AD7 to AD0		1/2 t_{inst}*– 80 ns	120	µs	No wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to AD0, $\overline{RD}$		0	—	µs	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}*– 40 ns	—	µs	
$\overline{RD}$ ↑ → address loss time	t_{RHAX}	$\overline{RD}$, A15 to A08		1/4 t_{inst}*– 40 ns	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}*– 40 ns	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}			0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	µs	
BUFC ↑ → valid address time	t_{BHAV}	A15 to A08, AD7 to AD0, BUFC		5	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

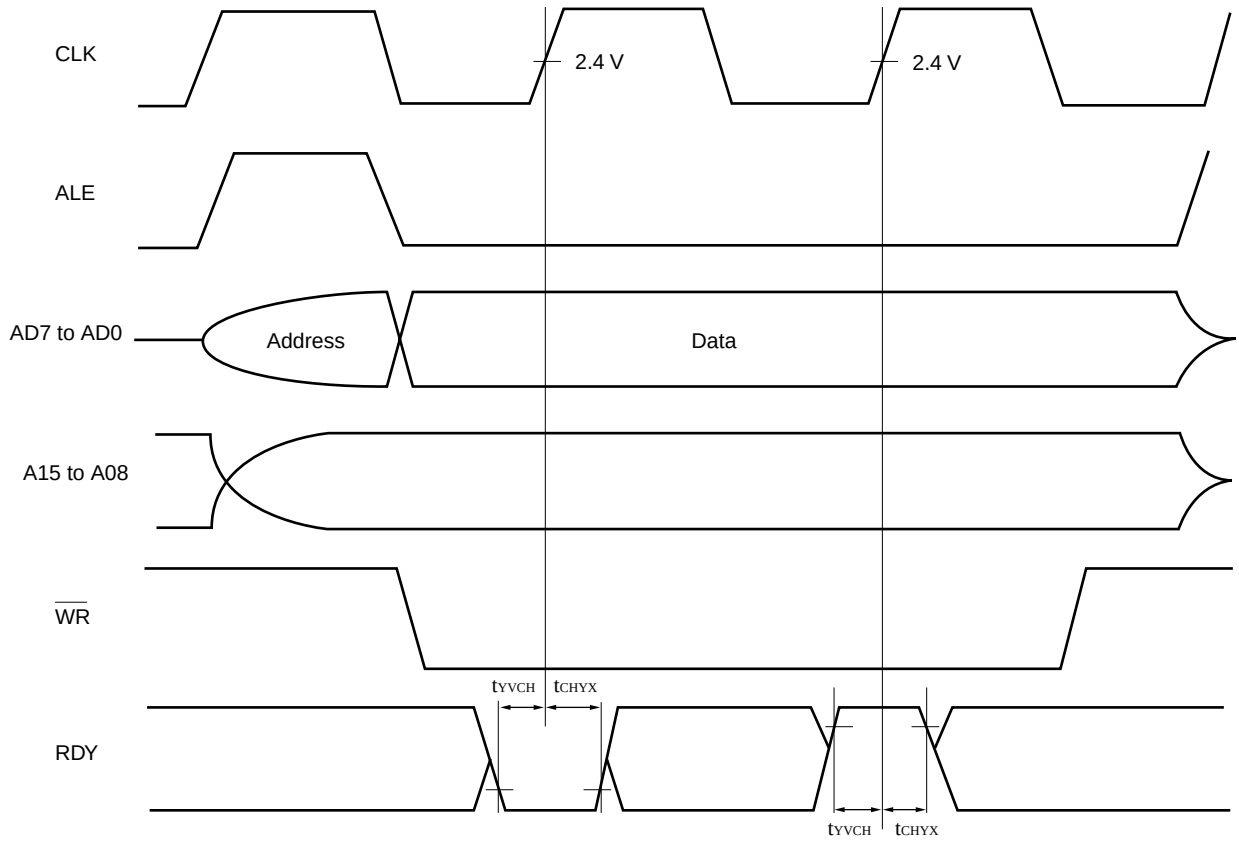


(8) Ready Input Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY loss time	t_{CHYX}			0	—	ns	*

* : This characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

(9) Serial I/O Timing

(V_{CC} = 5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, UCK1, UCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time UCK1 ↑ → valid UI1 hold time UCK2 ↑ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, UCK1, UCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, UCK1, UCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↓ → valid SI1 hold time UCK1 ↓ → valid UI1 hold time UCK2 ↓ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	

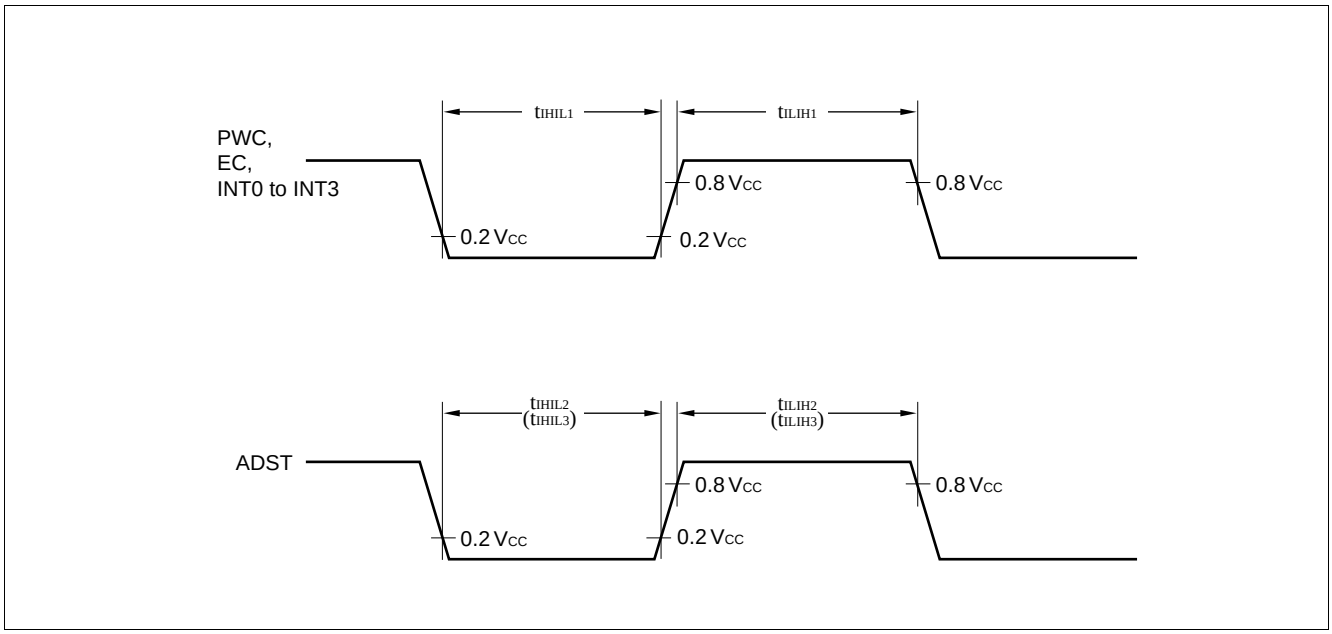
* : For information on t_{inst}, see “(4) Instruction Cycle”.

(10) Peripheral Input Timing

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	PWC, INT0 to INT3,EC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	ADST	2^8 t_{inst}*	—	µs	A/D mode
Peripheral input “L” pulse width 2	t_{IHIL2}		2^8 t_{inst}*	—	µs	A/D mode
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	2^8 t_{inst}*	—	µs	Sense mode
Peripheral input “L” pulse width 3	t_{IHIL3}		2^8 t_{inst}*	—	µs	Sense mode

* : For information on t_{inst}, see “(4) Instruction Cycle”.



5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC}$ = 3.5 V to 6.0 V, F_{CH} = 10 MHz, $AV_{SS} = V_{SS}$ = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	At $AV_{CC} = V_{CC}$
Linearity error			—	—	±2.0	LSB	
Differential linearity error			—	—	±1.5	LSB	
Total error			—	—	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	V	
Interchannel disparity	—	—	—	—	4	LSB	
A/D mode conversion time			—	13.2	—	µs	At 10 MHz oscillation
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	—		0.0	—	AVR	V	
Reference voltage		—	0.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		—	200	—	µA	AVR = 5.0 V

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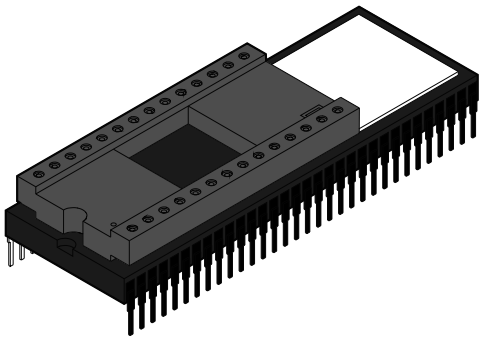

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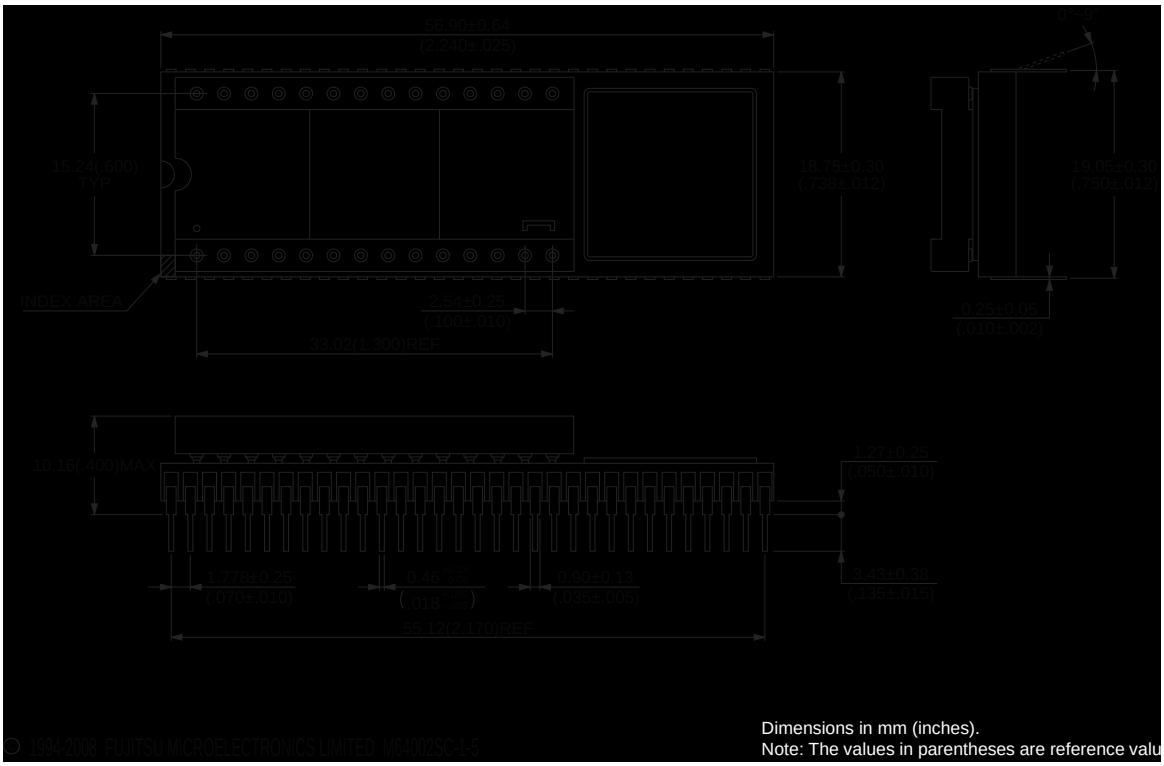

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